QDC Technology Engine Service Manual

Software Version 16 and above

Part Number: DRAFT DDRM100-A

Document Number: 1

THE BENCHMARK IN DIGITAL AUDIO

Introduction

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Contents

Certificates & Compliances

CC Emission Control

This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to Part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications.

The Merlin Console and Engine conform to the EMC directives :-

EN 55022:1998 Class A - Emissions

EN 55024:1998 Class 3 - Susceptibility

The Merlin Console and Engine also conform to the Safety directives :-

UL 1419 - Professional Video & Audio Equipment

IEC 60950 - Information Technology Equipment

For further information on EMC procedures please refer to the following titles:-

Noise Reduction Techniques In Electronic Systems by Henry W Ott

EMC by Tim Williams

Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense. Changes or modifications not expressly approved by Fairlight ESP can affect emission compliance and could void the user's authority to operate this equipment.

CHARACTERISTICS	DESCRIPTION
Equipment Type	Supplemented Data: Information Technology
Equipment Class	Supplmental Data: Class 1 - Grounded equipment
Installation Catergory	Requirment Category 2 - Local level appliances, portable equipment etc.
Pollution Degree	Requirment: Level 2 operating enviorment - Normally only non-conductive pollution occurs. Occasionally there may be a temporary conductivity caused by condensation.

Mains Plugs & Mains Power Cords

The following lists the recommended Mains Plugs and Leads for use in various countries throughout the world.

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Standards applicable for Mains Plugs	**Rating**	**Country**
ASTA BS1363 1984	10A @ 250VAC	UK
BS546, 1950	10A @ 250VAC	India, Kenya, Nigeria, Kuwait, Parts of Asia and the Far East
IEC695-2-1 & NF-USE	10A @ 250VAC	France & Belgium
DIN49441 & CEE 7 Sheet VII	10A @ 250VAC	Europe
SEV	10A @ 250VAC	Switzerland
CEI23-16	10A @ 250VAC	Italy
NEMA5-15P & NEMA6-15P	10A @ 250VAC	USA
Mains Power Leads		
Standards applicable for Mains Leads	**Rating**	**Country**
CSA22.2 No.42 & UL498	10A @ 250VAC	Canada & Japan
ASE 1011 (1959)	10A @ 250VAC	Switzerland
CEI 2316	10A @ 250VAC	Italy
SRAF 1962	10A @ 250VAC	Denmark
AS3112-1990, NZSS198-1967	10A @ 250VAC	Australia, New Zealand, Fiji, Papua New Guinea, Republic of China
UL498 & SJT 10A minimum rating with IEC60320-1 coupler	10A @ 250VAC	USA

Pre-Installation & Cabling Considerations

The following information is presented to ensure a smooth and timely installation and commissioning of the Fairlight QDC Technology Engine.

Pre-Installation Checklist

- Is all relevant building work completed ie. timber, concrete, plaster, brickwork? Building work is a source of dust and moisture, both which can seriously affect system operation and reliability.

- Is the flooring complete, ie. carpeting, tiling, ducting? All work generating vibration, moisture or dust, must be completed before the installation can be considered. The warranty may be invalidated, and the system mean time before failure may be reduced, if this is not strictly adhered to.

- Have all mains cables and breakers been installed, in both the machine room and studio? It is recommended that the same power source be used for both the mainframe and the console. This can be achieved by installing a power run from the machine room mains to the studio (or wherever the console will be located), as the power source for the console.

- Have you received the pre-install connector kit? The installation manual contains all pinout information required to allow cable assembly.

- Is the studio and machine room wiring installation complete?

- Are all cables terminated and is all cable ducting accessible?

- Has the studio earthing been installed, are all earthing cables identifiable?

- Are all signal cables earthed at one end only? To avoid earth loops it is recommended that all signal cable shields be connected to ground at one end only.

- Has the air conditioning system been running for one to two days prior to installation? Air conditioning must be operating prior to installation in order to purge dust from the rooms and air conditioning ducts.

- Has the loading placed on the air conditioning by the system installation been considered? A clean, dust free and low humidity environment with an ambient temperature of 19° C or lower is recommended.

- Will all external system interfacing have been completed? All Multitrack sends and returns, audio and video tie lines, sync sources and video distribution cabling should be completed.

- Are all audio and video tape machines installed and tested?

- Are all video monitors installed and tested?

Section 1 - Introduction

The aim of this manual is to familiarize service personnel with the new Fairlight QDC Technology Engine and provide technical information which will allow troubleshooting and diagnosis of the following Fairlight Products :-

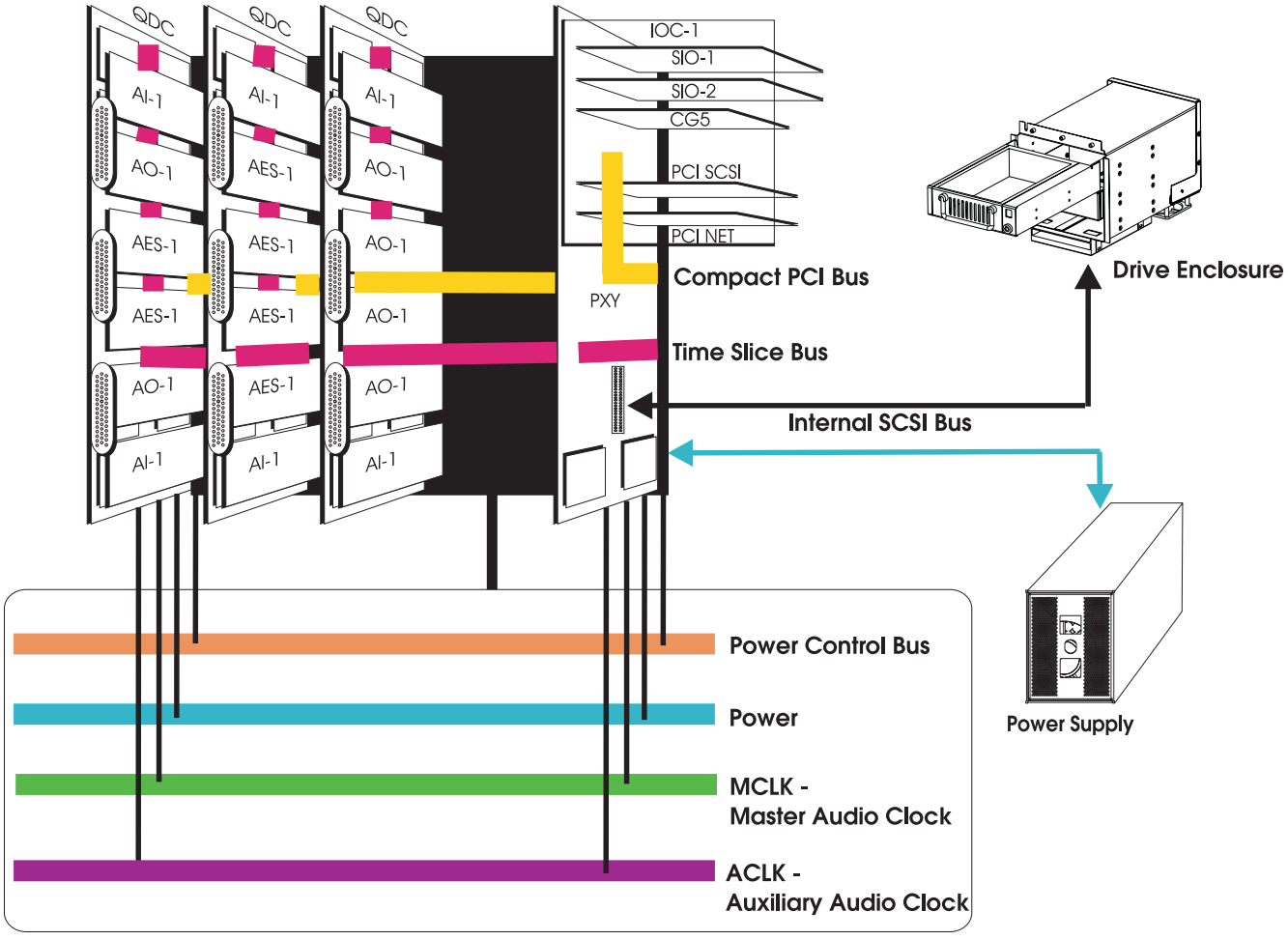
- Merlin
- FAME 2
- Prodigy 2
- MFX3.48

The manual provides installation and configuration instructions through including the Merlin Installation Manual.

The manual also provides detailed functional descriptions and schematics. of the internal boards which make up the Engine.

1.1 QDC Engine Overview

QDC Engine



QDC Technology Backplane

2.1 QDC - Technology Explanation

2.2 System Buses

2.2.1 PCI

Used as the backplane for the whole system. Allows exceptionally fast transfers between disk and audio channel cards.

2.2.2 TSB

Connects all DSP chips via a 600-slot "patchbay". Allows any DSP to exchange a sample with any other in every sample period. The corresponding bus in MFX3plus had 50 slots.

2.2.3 MCLCK

Master clock for driving the internal sample rate.

2.2.4 ACLCK

Auxiliary clock for driving the I/O sample rate. This allows there to be a different sample rate at the inputs and outputs from that in the DSP engine, so we can work with asynchronous digital signals (requires sample rate conversion).

2.2.5 Power Control

Allows ordered shutdown without damage to files.

2.3 Circuit Boards

2.3.1 PXY

Combines all elements of the following MFX3plus boards:

- WX
- TSCSI
- PCI
- SYNC

2.3.2 QDC

Includes 8 SHARC DSP chips (same as whole of MFX3plus), with 128 meg of waveform RAM. This allows longer record queues, more graphical waveform coverage of the screen, more track bandwidth.

The QDC is also used to support the I/O cards, and it will allow up to 32 inputs (up to 16 of them analog) and 32 outputs to be fitted to each card. In some situations the requirement for I/O will cause an extra QDC to be added to the system, even though its DSP processing power is not needed.

2.3.3 SIO-1

Processes external sync signals AES, WCLCK, Video, LTC. Also 9-pin Master and Slave.

Uses VCXO technology for ultra-low jitter.

2.3.4 SIO-2

Processes second 9-pin port and GPIOs (8 now, expandable with external circuitry to 64).

2.3.5 CG5

New graphics card. Provides 3 extra scrolling planes (8 times as many colours) and hi-res graphic output (3 times as many pixels as before).

2.4.6 IOC-1

Carries connectors for sync and graphics signals. Allows the Engine to be almost cable-free internally.

2.4.7 AI-1

8 analog inputs.

2.4.8 AO-1

8 analog outputs.

2.4.9 AES-1

8 digital I/Os.

For more detailed explanations of the QDC Engine please see futher sections within this manual.

Installation Manual

Software Version 16.2

Part Number: DMER201-C

Document Number: 146

Manual by: Owen P Walker

Important Notice

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SAFETY SYMBOLS

The lightning flash with arrowhead symbol, within an equilateral triangle, is intended to alert the user to the presence of un-insulated "dangerous voltage" within the product's enclosure; that may be of sufficient magnitude to constitute a risk of electric shock to persons.

L'eclair, dans une triangle, est destiné à alerter l'utilisateur de la présence de haute tension dangereuse non isolée dans l'enclosure du produit, qui peut être d'un voltage suffisant pour constituer un risque d'électrocution.

Das dreieckige Schild mit Blitzsymbol soll den Benutzer vor unisolierten Hochspannungen innerhalb des Gerätes warnen. Es besteht Lebensgefahr durch elektrischen Schlag!

El simbolo del rayo dentro de un triángulo equilátero, es usado para indicar la presencia de un voltage peligroso en el interior del aparato, de suficiente intensidad, como para constituir riesgo de electrocución a las personas.

"三角形内加上闪电似的箭号"表示机件/机器内部有"暴露的高电压"，可能造成触电的危险。

The exclamation point within an equilateral triangle is intended to alert the user to the presence of important operating and maintenance instructions in the literature accompanying the appliance.

Le point d'exclamation dans une triangle est destiné à alerter l'utilisateur de la présence d'instructions importantes de fonctionnement et d'entretien dans la littérature accompagnant l'appareil.

Das dreieckige Schild mit Ausrufungszeichen soll den Benutzer auf wichtige Bedienungs- und Wartungshinweise in der Bedienungsanleitung hinweisen.

El simbolo de exclamación dentro de un triángulo equilátero avisa al usuario de la presencia de instrucciones importantes acerca del funcionamiento y mantención del aparato en los documentos que se

"三角形内加上感叹号"表示提醒使用者查阅附上的"重要操作和维修指南"。

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UL498 & SJT 10A minimum rating with IEC60320-1 coupler	10A @ 250VAC	USA

OBTAINING TECHNICAL SUPPORT

Users requiring technical support should contact their local Fairlight office or distributor.

Information can also be found on the world wide web at :-

http://www.fairlightesp.com.au

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France	**USA – East Coast**
Fairlight France 41-43 Rue des Peupliers 92100 Boulogne-Billancourt Paris France Tel: +33 1 4610 9292 Fax: +33 1 4610 9295	Fairlight USA 2 West 45th Street, Suite 605 New York, NY 10036 USA Tel: +1 212 819 1289 Fax: +1 212 819 0376
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Asia - Pacific	
Fairlight ESP Pty.limited Unit 2, 1 Skyline Place, Frenchs Forest NSW 2086 Australia Tel: +61 2 8977 9999 Fax: +61 2 8977 9900	

Section 1 - Introduction

1.1 Product Description

Merlin is the first of a new generation of disk based multitrack recorders from Fairlight. The system marries together the MFX user interface with the technology of the latest generation of digital audio workstation in a combination that has a significant impact on productivity and efficiency.

The Merlin interface incorporates a dedicated editing Console, a unique graphical user interface and powerful database capabilities. These tools allow the operator to work quickly and efficiently without impeding the creativity of the recording and editing process, and can now be fully utilized in the professional audio suite. The Merlin offers a number of unique benefits through its adaptation of DSP and proprietary technology to the audio environment.

For a more detailed explanation of the Merlin, please refer to the *Merlin User Manual.*

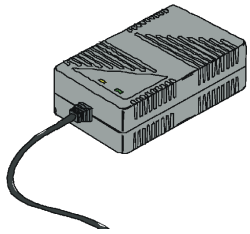
1.2 Manual Summary

The purpose of this manual is to provide all the technical information required to design a suitable installation for the Merlin system and to fit and connect the units. It is assumed that the installer is familiar with both analogue and digital audio signals. For full operational instructions please refer to the *Merlin User Manual.*

1.3 System Overview

The Merlin is made up of four interconnecting components, the Merlin Console and external power supply, a Flat Screen Display Monitor and a Engine rack mounted unit which contains all the electronic circuitry, disk drives and audio I/O necessary to run the system.

Merlin Console & Flat Screen Monitor



Console Power Supply Unit

Engine

Audio Mixer

1.4 Unpacking

It is advisable that before any installation work is attempted that the system be unpacked and the contents verified. A sizeable area approximately 3 meters square should be suitable. Using the basic packing list attached record the items you have received. This will both help you when you have to make an enquiry, by having the relevant details logged in your Installation Manual, in the event of a packing omission. At this stage do not power up the system, nor remove electronic modules from the system, as damage may occur if not handled correctly.

1.5 Equipment Supplied

EQUIPMENT SUPPLIED	QUANTITY	CHECK LIST
Mainframe	**1**	
Merlin Console	**1**	
Merlin External Power Supply Unit	**1**	
Mouse	**1**	
9 Pin Cable	**1**	
Merlin Installation Manual	**1**	
Merlin User Manual	**1**	
Merlin Console Controller Cable	**1**	
VGA Cable	**1**	
IEC Mains Cable	**2**	
Keyboard	**1**	

1.6 Static Precautions

Please take note that all Fairlight manufactured electronic modules are static sensitive and should be handled under anti static conditions. When working on a system always ensure that you have an anti static lead connected and that the system is connected to ground through an earth lead.

Never work on the system while powered up unless you are authorized by Fairlight to do so. As a matter of practice always touch the external chassis of the system before opening the front panel. If cards are not handled under anti static procedures your machine may sustain damage which could either cause a complete failure or may cause intermittent crashes and subsequential system failure.

When handling cards please ensure that they are placed in anti static bags when not in the system. For shipment purposes electronic modules should be placed in an anti static bag and then suitably surrounded with loose packaging materials in a solid card board box. Cards shipped to Fairlight without the correct anti static packaging will have their warranty voided. If you have any enquiries on this matter please feel free to contact your local Fairlight office or distributor.

1.7 Environment

The system is designed to be operated in a clean air-conditioned environment. Generally, an area comfortable for people (20°C - 21°C) should be suitable. The rack mounted units and disk drives, use fans for ventilation. Users may find it desirable to install these units away from the operator/console location. Note that cable lengths, as detailed in *Section 2.5 - External Cable Length Considerations*, should be taken into account when planning the installation.

Make sure that the rack units can access cool air through the opening on the front of the Engine and expel warm air from the back. As with all computer systems, the Fairlight will operate more reliably if static generating floor coverings are avoided.

Do not fit the Engine into a closed environment except where ducted cool air is forced through the Rack. Do not run the Engine whilst it is on the ground as it will accumulate dust, which may eventually cause a failure.

The Engine unit is normally installed in a suitable 19" rack which is at least 600 mm deep, or has an open back section. It is recommended that external hard drives be mounted on a rack tray, above or below the Engine, using the shortest possible cables to prevent SCSI bus corruption.

Please Avoid:

- Fitting the Engine where air circulation will be restricted.
- Installing Engine close to heat sources.
- Installing in dusty or damp area.
- Installing in area subject to vibration.
- Installing in area with strong magnetic or electric fields

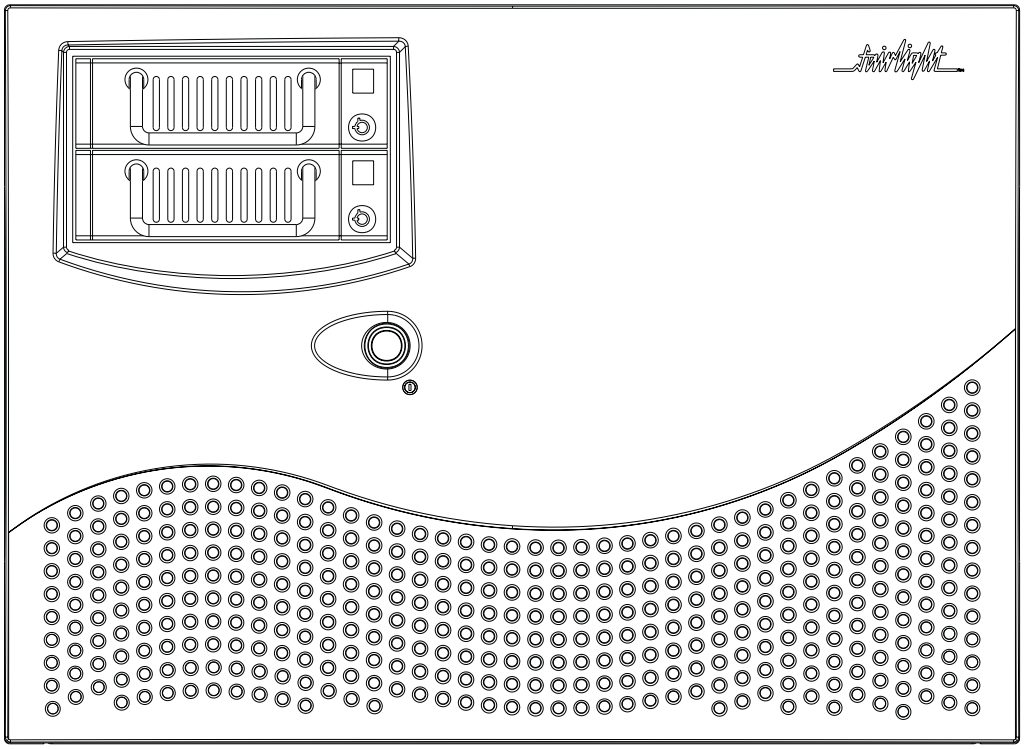
SECTION 2 - ENGINE PHYSICAL INSTALLATION

2.1 MECHANICAL INSTALLATION

The Engine unit, takes up 8 RU, when fitted into a 19" rack. It operates from either 100-120v or 200-250v, 50-60Hz with the mains inputs being auto- switching, as such there are no switches to be set. At least two people are required to fit the Engine into a 19" rack as the unit is quite heavy. If available it is suggested that a third person be made available for the initial installation into the rack, such that a person can guide the Engine into the rack, from the rear.

The Engine should be fitted so that there is no restrictions to the ventilation, at the rear of the unit. If external SCSI devices are to be connected it is recommended that these be placed on a rack tray above or below the Engine.

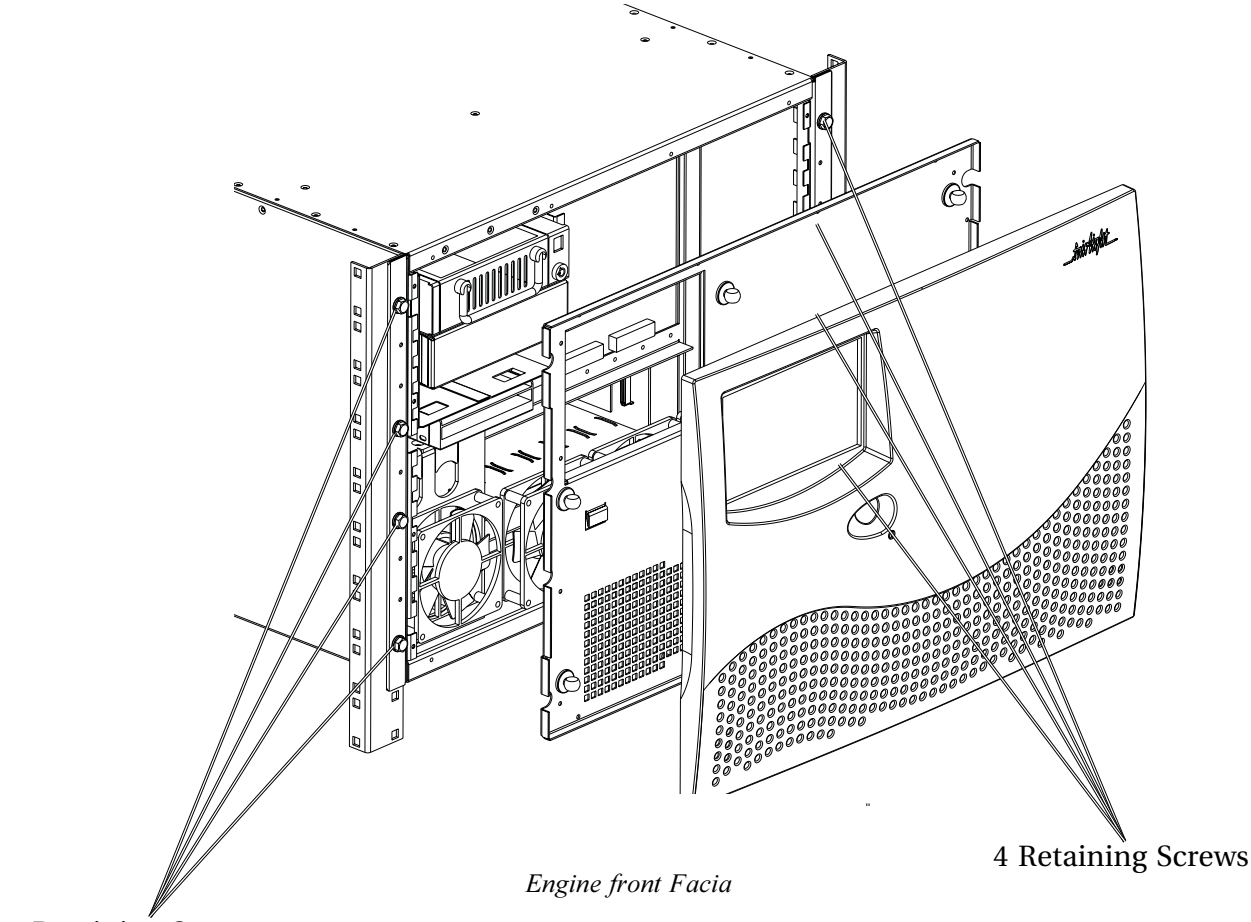
It should be noted that typically the Engine unit is fitted with a boot drive with SCSI I.D. " 0 "(although the boot drive can be at any ID). The Engine uses fans for its forced ventilation system, these generate an amount of ambient noise. As stated before the Engine should be located in an air conditioned machine room away from the studio and other heat generating equipment.



Engine Front Panel

1 Install the Engine into a 19" Rack unit. Once this is done, the front facia of the Engine must be removed to allow 8 retaining screws to be fitted.

2 To mount the Engine into the rack, remove the front dress panel and insert 4 retaining screws on to both the left and right rack mounts. Once this is done reattach the front dress panel.



Engine front Facia

2.2 Electrical Installation

The Engine is designed to run from a single phase power source with one of its current carrying conductors at or near ground earth ground potential (the neutral conductor). Only the line (live) conductor is fused for over-current protection. Systems that have both current carrying conductors live with respect to ground , such as phase-to-phase in multi-phase systems are not recommended as power sources.

It is recommended that both the Engine and Console are connected to the same electrical supply or ring main which ideally should be regulated and smoothed. If the power source is likely to be unexpectedly cut then both the units should be fed from a backed up power source such as a UPS.

For Power Requirements, see Appendix A21 at the back of this Manual.

Mains connections should be fitted with the appropriate type of plug. See Section *"Mains Plugs & Power Cords"* at the front of this Manual.

2.3 Engine Rear Panel Connections

The Engine rear is split into two distinct sections; the System I/O Panel, located to the right and the Audio I/O section, located to the left.

The System I/O Panel contains all the synchronization needed to allow communication with external devices including RS-422, Midi, LTC, AES Sync, Serial and GPIO.

To allow communication with other Fairlight products including Fame and Prodigy, a Mixer port is provided.

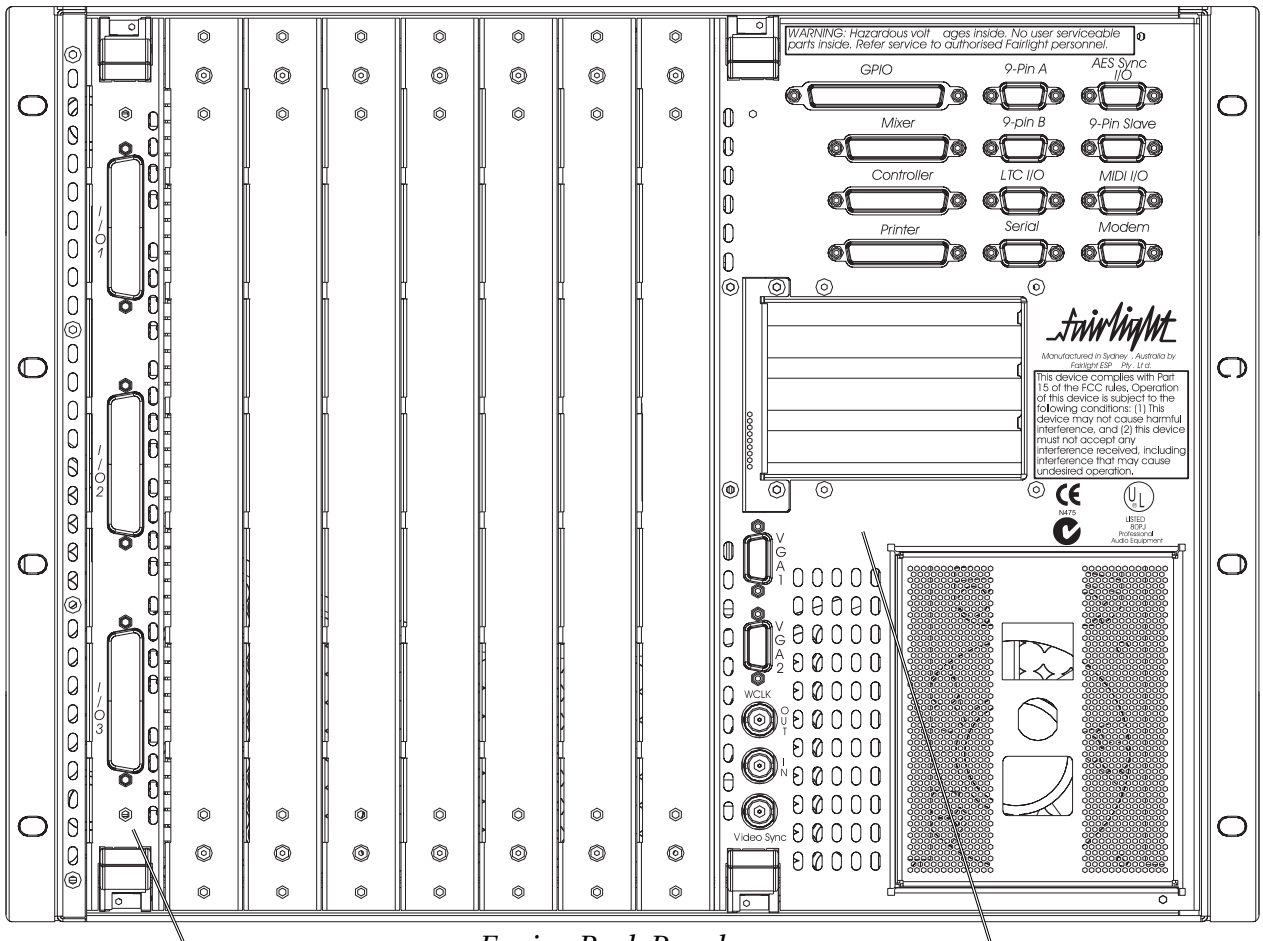
To allow comunication with the Merlin Console, a Controller port is provided.

The System I/O Panel also contains the VGA Output, Word Clock and Video sync In connectors.

The Audio I/O Section can contain up to a maximum of 4 QDC cards, which perform all analog ue and digital I/O Connections and Processing. Each QDC card can contain a maximum of 16 analogue inputs and 32 analogue outputs or a maximum of 32 digital inputs / outputs and 16 analogue inputs.

Depending on what configuration is ordered, the system can allow for more QDC cards to be configured. Please contact your local Fairlight office or distributor for further information regarding the maximum inputs and outputs which can be configured within the system.

Please refer to the Appendix page 36 for further details on the Audio I/O and System I/O Panels.



2.4 Cabling

Once the mechanical installation of the Engine is complete, a number of cables must be connected. Some of these connect various components together and may have been supplied with the Merlin system, others provide connection to the rest of the environment.

The interconnecting cables suppled as standard may not be long enough for your installation, in which case you must provide longer cables. The following information gives specific wiring details and highlights any special requirements, however as with all equipment not supplied with the Merlin system, it is the installer's responsibility to ensure that these cables comply fully with the applicable safety and EMC regulations.

2.5 External Cable Length Considerations

Poor cabling can be the bane of a good system. Earth loops, floating inputs and outputs and extended runs are just some of the issues to be addressed when planning an installation.

2.5.1 Merlin Control Cable

The Merlin Control Cable connects the Merlin Console to the Engine. The cable carries RS232, RS422 and MIDI signals and is limited to a maximum length of 30 meters, providing correct attention is paid to signal pairing using twisted pair cable. Ensure sufficient slack is left at the Console end to ensure movement of the Console does not cause undue stress on the connector, or cause the connector to partially disconnect, which can damage the serial drivers. When fitting or reconnecting the cable ensure that power is off at either the Engine or the Console.

2.5.2 Sony 9-Pin Cable

The 9-Pin cable connects the Engine to a Sony 9-pin protocol machine. The recommended maximum length for this cable is 30 meters. The Engine is supplied with a 5 meter cable. Again it is recommended that the power be switched off at one end when connecting to protect the drivers.

2.5.3 VGA Cable

The Video cable connects the VGA output from the Engine to the attached Monitor. It is a 15-way shielded 50 Ohm cable with high density D-type connectors at each end. A maximum length of 20 meters is typical. The Fairlight Engine is supplied with a 10 meter cable which has been found to be suitable for the majority of monitors.

2.5.4 Audio Cable

Standard shielded audio cable is suitable.

2.5.6 Digital Audio Cables

Digital cables connected to the Engine system must be of the correct 110 Ohm impedence.

2.6 Connecting The Various System Components

1 Once cabling issues have been dealt with the various system connections need to be made.

2 Connect an IEC Power lead to the back of the Engine.

3 Connect the 15 way D connector of the Video cable to VGA 1 connector on the System I/O Panel on the rear of the Engine.

4 Connect the Console Controller cable to the connector on the System I/O panel located on the rear of the Engine.

5 Connect any external SCSI drives to the external SCSI card (if fitted) and ensure that the last device is terminated. Ensure that the SCSI I.D.'s are not in conflict with each other.

6 Connect all Synchronization cables such as LTC, Word clock, Video Black burst etc.

7 Connect all audio input and output cables to the QDC cards located on the rear of the Engine.

Section 3 - Merlin Console Physical Installation

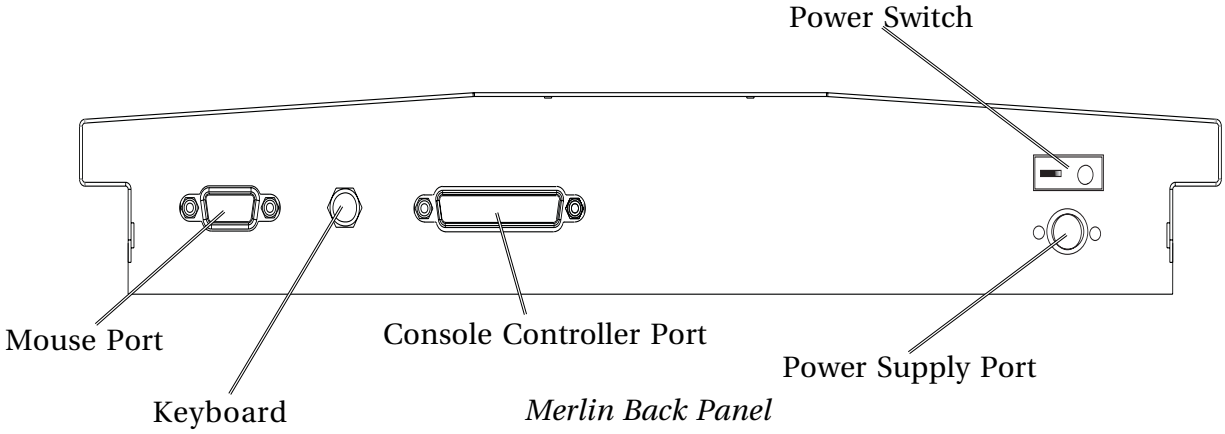
3.1 Introduction

The Merlin Console provides a control surface to allow the engineer to work quickly and efficiently. The Console has a number of user definable macros and keystrokes. For more information regarding the operational use of the console please refer to the *Merlin User manual.*

Merlin Console

3.2 Mechanical Installation

The Merlin Console should be sat on a level horizontal surface.

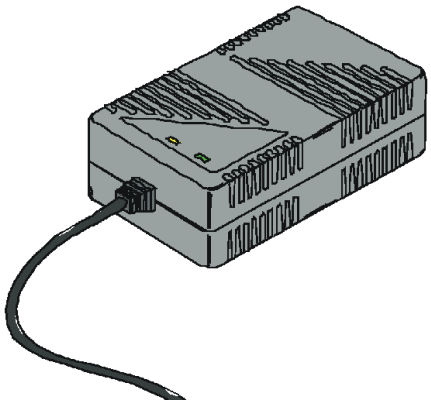


Merlin Back Panel

3.3 Electrical Installation

The Power Supply unit is an auto ranging unit which will take any input voltage from 100 to 250VAC using a standard IEC mains cable. As there are no mains switches on the power supply it should be plugged into a switched mains outlet. The output from the PSU is 12DV, fed to the console via an 8 pin mini DIN connector. As the output lead is fairly short, the PSU should be located close to the close.

A small LED indicator illuminates when the supply is on.



CAUTION : 1. DO NOT USE ANY OTHER POWER SUPPLY TO POWER THE CONSOLE.
2. DO NOT CONNECT THE POWER SUPPLY TO THE CONSOLE WITH THE MAINS POWER TURNED ON.

3.3.1 Merlin Control Cable

The Merlin Control Cable connects the Merlin Console to the Engine unit. The cable carries RS232, RS422 and MIDI signals and is limited to a maximum length of 30 meters, providing correct attention is paid to signal pairing using twisted pair cable. Ensure sufficient slack is left at the Console end to ensure movement of the Console, does not cause undue stress on the connector, or cause the connector to partially disconnect, which can damage the serial drivers. When fitting or reconnecting the cable ensure that power is off at either the Engine or the Console.

3.4 Interconnecting The Console And Engine

1 Place the Console at a suitable location close to the mixing desk.

2 Connect the Console Controller cable to the 37 Pin D connector on the rear of the Console.

3 Connect the mouse to the 9 Pin D connector on the rear of the Console.

4 Connect the Console power supply cable to the Merlin Console and then connect the mains power to the Merlin Console power supply unit.

5 Connect the Keyboard cable to the Keyboard socket on the back of the Merlin Console.

6 Once all connections have been made to the Console, it can be powered up safely, by pressing the switch located on the back panel.

3.6 Internal and External SCSI Devices

The Engine unit has been designed to accept two 3.5 Inch drives and 2 5.5” drive bays internally which can take either Kingston Technology drive enclosures or an Exabyte enclosure. The system typically comes configured with one system disk which contains the O/S9 Operating System and Merlin software. This allows for 3 media drives to be fitted internally in the system.

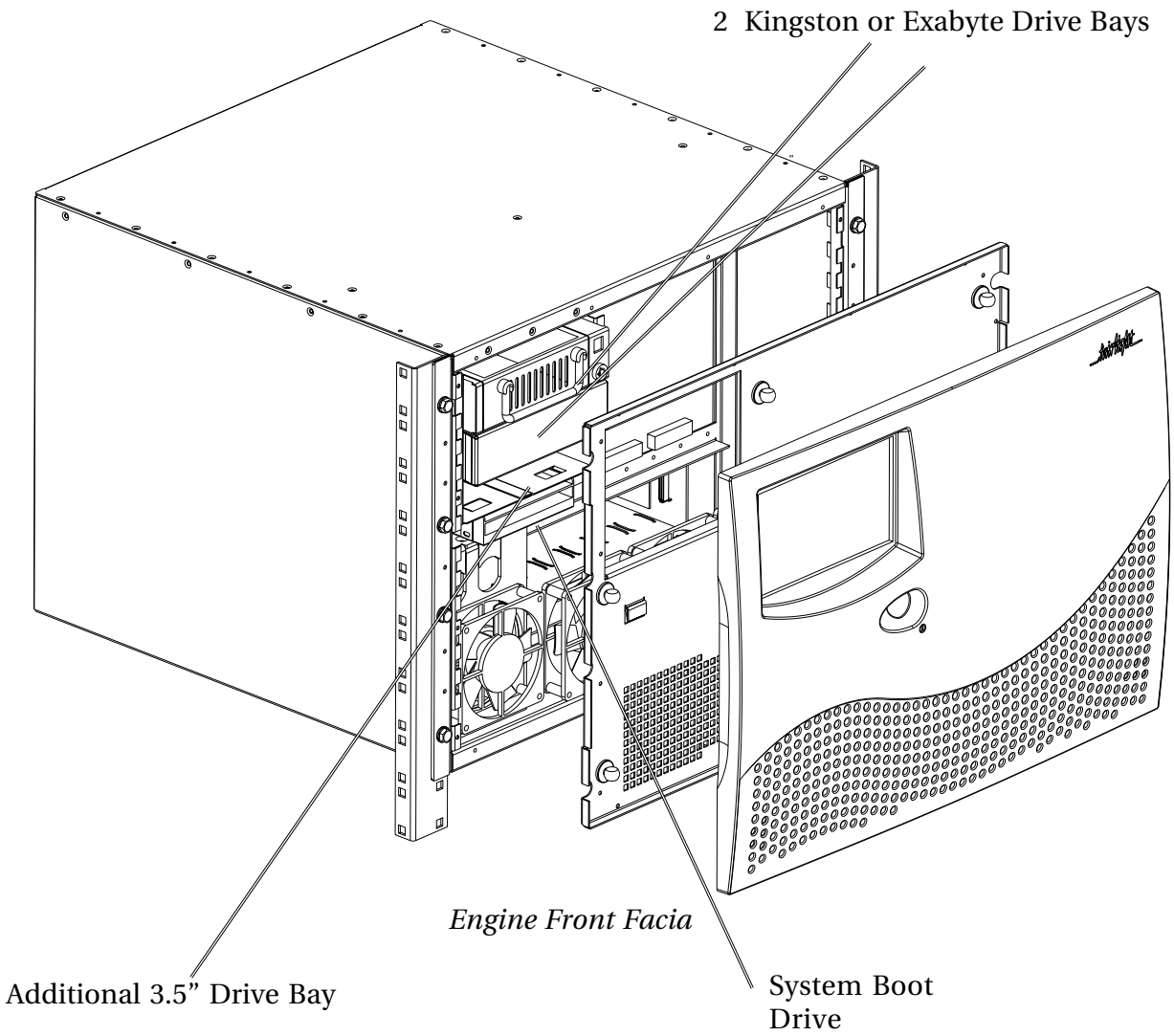
With a second SCSI Controller installed within the Engine an additional 4 SCSI devices can be attached externally.

Typically Exabyte drives should be set to ID “5” when connected on either SCSI Buss.

Optical based devices should be set to ID “3”. When connected on either SCSI bus.

It is recommended that a rack tray be fitted either above or below the Engine to hold external SCSI devices. The last device on the chain should be terminated with all other devices being looped through. The cables should be the shortest length possible to avoid SCSI bus corruption.

See Section 5 - *Adding SCSI drives Internally and Externally.*



Section 4 - System Configuration

4.1 Introduction

The following describes the procedure for powering on the Console and Engine.

CAUTION : NEVER ATTEMPT TO ATTACH SCSI BASED DISK DRIVES OR OTHER CABLING WHILE THE SYSTEM IS RUNNING AS THIS MAY CAUSE FILE CORRUPTION. ALWAYS POWER OFF BEFORE CONFIGURING ANY CABLES.

4.2 Switching on the Equipment

4.2.1 Console

Once the mouse and cables have been connected, the Merlin Console can be powered up.

1. Turn on the power switch, at the power source, and on the back of the Console. The Console will then boot up.

2. The green LC display on the Console should display zero's on the top screen and on the lower screen the software revision.

4.2.2 Engine

1. Ensure all SCSI cables and terminators are connected.

2. Power up all SCSI devices.

3. Verify monitor cable is connected and then power up the monitor.

4. Ensure all Sync Input/Output cables are connected and secure.

5. Turn down the master faders on the mixing console.

6. Ensure all digital and analog Input / Output cables are connected and secure.

7. Ensure Merlin Console cable is connected and secure.

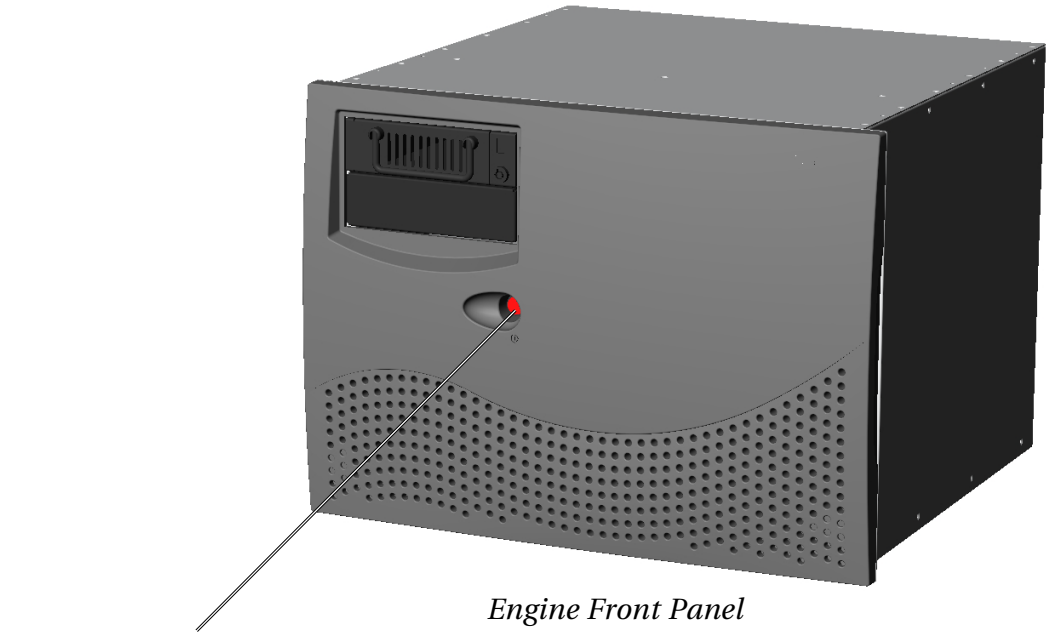
8. Ensure 9 pin control cable is connected and secure.

9. Power up the Engine via the switch on the back panel then press the switch on the front panel.

10. Power up the Merlin Console, if not already powered up.

At this point the system should be booting up if all has gone to plan. Initially you will observe a gray and blue text screen, containing system configuration information. The system will continue booting until the program is loaded.

Engine Back Panel



Engine Front Panel

4.3 Boot up screen

At this point the system should be booting up and the following text should be seen on the graphical interface.

1. Take note of the SCSI devices being found in case a problem is encountered.

```
+-----------[  Fairlight ESP - MFX Mainframe - Flashware v1.00 [16.1.07b] ]---+
|                     Backplane: Yes (9)              Compile Date: Feb 21 2000|
|                       SIO [1]: No                   Compile Time: 12:05:16   |
|                       SIO [2]: No                 IntGlue Xilinx: 34         |
|      Colour Graphics Card [A]: No                     TSB Xilinx: 7          |
|      Colour Graphics Card [B]: No                     Machine ID: 061C207A   |
+--------------[  Non Volatile RAM Options ]-----------------------------------+
|     SCSI Controller Boot Slot: 0                ROM Debug Level: OFF         |
|              SCSI Initiator ID: 7                   IOPACK Mode: 46 Lines    |
|               Synchronous SCSI: Yes                                          |
|             Disconnecting SCSI: Yes                                          |
|                      Wide SCSI: Yes                                          |
+--------------[  DIP Switch Settings ]-----------------------------------------+
|    Enable System Debugger #A1: No        Boot ROM Select (0) #B1: No         |
|          Disable PCI BIOS #A2: No        Boot ROM Select (1) #B2: No         |
|               Disable MMU #A3: No           HIRES CG5 Enable #B3: No         |
|     Disable IOPACK Output #A4: Yes                DipSwitch #B4: No          |
|         Change CCB to CWT #A5: No                 DipSwitch #B5: No          |
|               QDC Disable #A6: No                 DipSwitch #B6: No          |
|     QDC Order left->right #A7: No                 DipSwitch #B7: No          |
|                 DipSwitch #A8: No                 DipSwitch #B8: No          |
+--------------[  PCI Buss Status ]-----------------------------------------+
|                 On Board SCSI: Installed   Symbios 53c875   [1000:000F:#91]  |
|                       Slot #1:  Vacant                                       |
|                       Slot #2:  Vacant                                       |
|                       Slot #3: Installed     Intel i82557   [8086:1229:#90]  |
+------------------------------------------------------------------------------+
OS-9/68040 System Bootstrap [Dynamic RAM Version]

Press Key to Display Boot Menu ... 4 3 2 1 Autobooting

Scanning On Board PCI SCSI Controller
ID -    DEVICE TYPE    VENDOR   PRODUCT          FIRM CAPACITY SECT    MB
-------------------------------------------------------------------------
01 -     Fixed Disk    IBM      DRVS09V          0270 011191F9  512  8754
-------------------------------------------------------------------------
Attempting to Boot to Target #1 on the Onboard Controller
Detected an RBF Formatted Disk.
A valid OS-9 bootfile was found.
-nt
Setting Lines Per Page to 48 - [TERM=xterm] ....................................
Loading Resident Modules .......................................................
Starting Resident Fairlight Extension Modules ..................................

flight: v3.09 - Fairlight OS9 Extensions
ESP Messages Version 1.10

Initialising MMU ...............................................................
Starting RAM Resident IOPACK ...................................................
Saving Last TVT Image (/dd/tvtlog.txt) .........................................
Press Any Key to Edit System Configuration ..................... 4 3 2 1
Starting Network ...............................................................
Creating primary (MASTER) network interface "/ie0" for [Web]
    HOSTNAME   = mfx_232
    IP_ADDRESS   = 192.100.105.232
    NET_MASK   = 255.255.0.0
    DOMAINNAME   = MFX
    INNET=ffff0000 BDCST=ffffffff
Creating device descriptor "ie0" "if82557" "ifman"
Creating socket: Devices "/lo0 /ie0" for host "mfx_232"
Starting Network
Starting TVT Drivers (TCP/IP Port 2700) ........................................
```

2. If the Merlin system has been configured to be part of a network, check that the Engine is attaching to the network. For further details on connecting to an Local Area Network, please the network administrator.

```
Starting MFX Console ..........................................................
================================================================================
                    System Identification
        Machine #:061c0283      Site:Fairlight ESP Pty Ltd
        MERLIN
        9-Pin:YES
        MFX
        Multi-Out:YES           Printing:YES            Time-FX:YES       Audiobase:TWO
        Tracks:48               A-In:48                 A-Out:48            D-In-Out:48
        Preview:YES             Connect:YES             MediaLink:YES
        Varispeed:YES           CD-Write:YES
================================================================================
Creating Temporary Directory (/dd/TMP) ........................................
Starting File Gopher, DFN Server, FFS, ANETD and NODED ........................
Starting SCSI Caching Sub-System and Media Daemon .............................
Initialising Audio Hardware ...................................................
jtag v2.06:
qdcinit v3.06
Resetting all QDCs
QDC 1 Slot 7 OK
DSP Resources
    1  QDC cards
    4  DCC sections
    8  DSP processors
I/O Resources:
    2  AIN cards
    2  AOUT cards
    2  DIO cards
    16 Analog Inputs
    16 Analog Outputs
    16 Digital Inputs
    16 Digital Outputs
Checking Versions of Modules, ROMS and Hardware ...............................

Starting Session ..............................................................
1 devices online
OS-9/68K V3.0.3   MFX/PX-DYNAMIC '/term' online 00/25/06 at 19:04:31
User name?: mfx

Process #32 logged on    02/01/06 19:04:52
Welcome!

MFX:
```

3. As the boot up process continues check that the Merlin Console is being seen.

4. If a problem is encounter with audio I/O check that the system is logging the QDC card or cards within the system.

5. If problems persist please contact a local Fairlight office or distributor.

4.4 System Fails To Boot From A Hard Drive

If your system fails to boot from a hard drive which you believe has software on it, the following procedure may be of assistance.

1. Reboot the system and press the < Space Bar > as soon as it is possible.

2. You should see a small menu with the following prompt;

" Select a boot method from the above menu: "

3. Type "SCAN" then press < Return >

4. Check that the drive you are attempting to boot from is detected.

5. If detected there is probably a boot sector problem on the Drive or the Drive may not have software installed.

6. If not detected, then check all SCSI connections and that the drive is powered up.

7. Check that each disk drive does not share any SCSI ID's on the same buss.

4.5 System Stops At Merlin Picture

If after powering up your new system it appears to stop at the point where the Merlin picture is displayed the following should correct the problem.

1. Type "QUIT" < Return >

2. Answer "Y" to the question.

3. Type "MFXLOAD" < Return >

4. Allow the Engine to load software into the Merlin Console. The Console will reset itself when finished.

5. Reboot the system by typing "RESTART" < Return >

6. The system should now boot through to the Disk Recorder.

7. If not, re-boot. At the second countdown, press any key. Check the network setup file is correct. Edit the file if changes need to be made. Then hold down the <blue> keyand press Z.

If the above procedure fails please press the < Blue > key and then the < ESC > key.

Contact your local Distributor or Fairlight office for further assistance.

4.6 Software Installation

From time to time software will need to be installed onto the Merlin system. The following describes the steps which need to be taken to install software.

4.6.1 Installing Software From Exabyte

To update software from the Exabyte whe no release files are available.

1. Ensure that an Exabyte drive is connected and set to ID 5.

2. Power up the Exabyte drive.

3. Place the Exabyte software tape in the drive.

4. Power up the Engine.

5. Press the < Space Bar > immediately on powering up the system. You may need to press the < Space Bar > a few times. The aim is to stop the system booting from a hard drive if one is connected.

6. The displayed prompt is " Select a boot method from above menu: ".

7. Type " ROM " < Return > to boot to from Rom.

8. Type " Upgrade -T " < Return>. This tells the system to boot from the Exabyte at ID 5.

Follow the procedure as appears on the screen. You will be asked if you want to reformat the drive. Answer NO to this if there are projects you require on the drive.

Section 5 - Drive Installations

5.1 Introduction

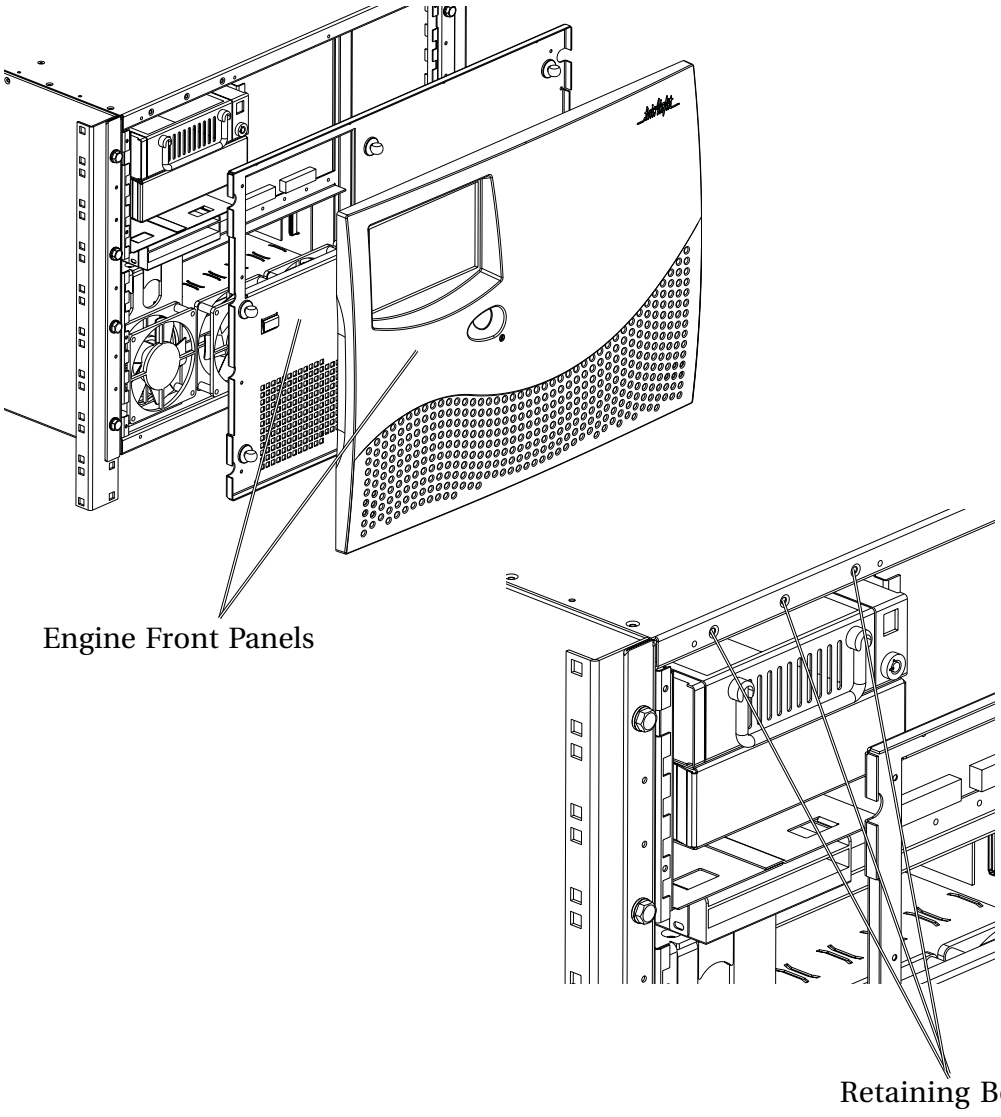
The following section deals with installing internal and external SCSI based media devices and configuring them for use with Merlin. For information regarding approved SCSI drives please refer to a local Fairlight office or distributor.

5.2 Installing Internal Hard Disk Drives

The Engine unit has been designed to accept two fixed 3.5” disk drives and 2 removable 5.25” drive enclosures fitted on to an internal drive bracket. The system comes configured with one system disk which contains the O/S9 Operating System and Merlin software. This allows for 3 media drives to be fitted internally. The two removable drive carriers have been designed to provide durable and reliable mounting for 3.5” SCSI drives within 5.25” half height peripheral slots.

The Internal SCSI buss is connected via a SCSI loom directly to the motherboard. The SCSI buss is based on the Ultra Wide, 68 Pin configuration

1 To install a hard drive within the Engine, first remove the dress panel.



2. Next, unscrew the eight screws holding the front panel in place, gently pull the front panel away from the Engine, being careful to note the three cables connected to the back of the panel from the power supply and the back plane within the Engine.

3. Disconnect the fan power loom from the connector labeled F1 on the back plane.

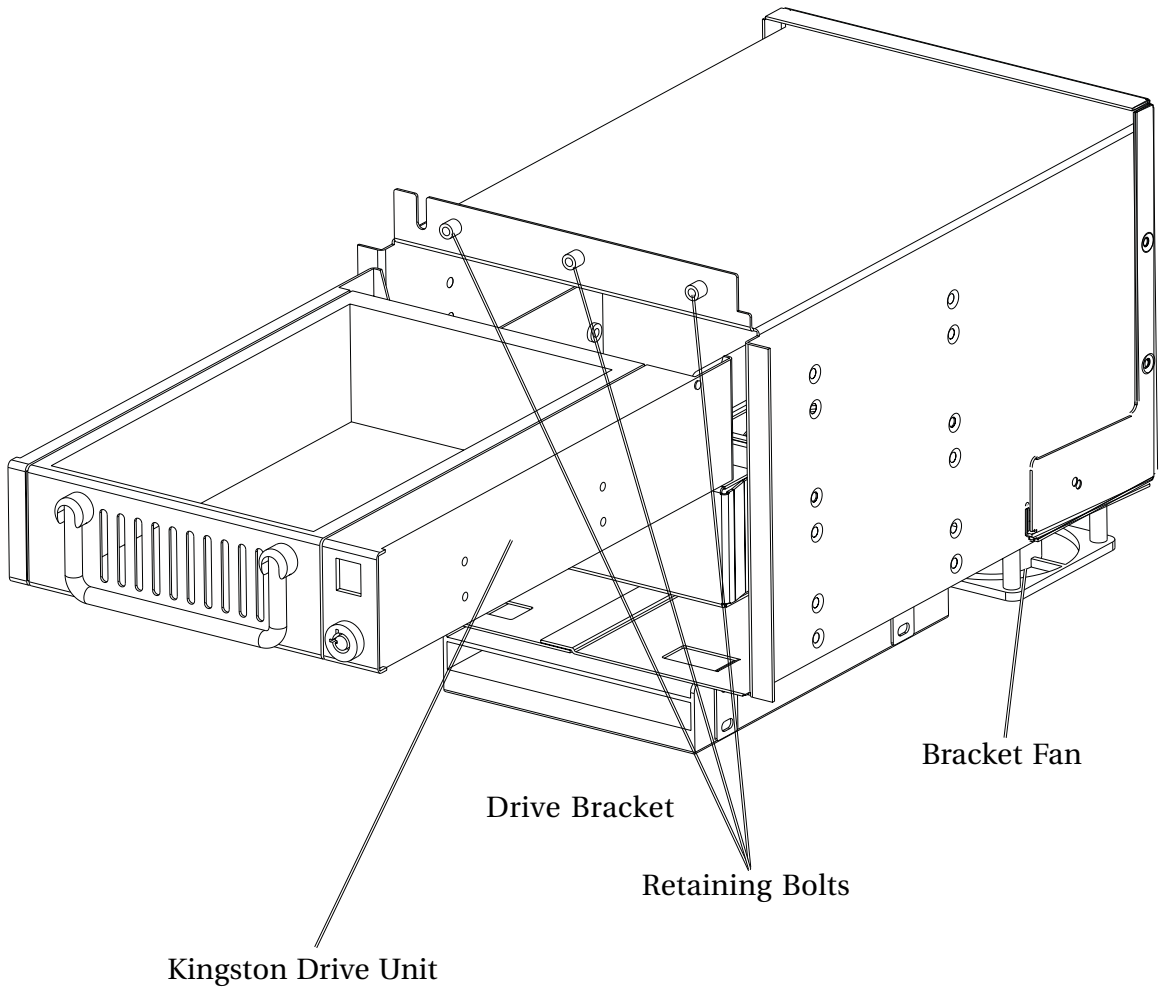
4. Using a small flat headed screwdriver, turn the red screw (anti-clockwise) on the power switch connector on the rear of the front panel.

5. Disconnect the power connector, leading from the Power On switch to the F2 connector on the back plane (and leading to the Power Supply).

6. Disconnect the SCSI extender cable from the internal SCSI cable, mounted on the right side of the power supply.

7. The front panel can now be removed fully from the front of the Engine and placed on a suitable surface until reinstallation.

8. Next remove the three bolts holding the drive mount bracket in place.



9. Pull out the bracket from the Engine being careful to disconnect the power cable for the fan attached.

10. Remove termination blocks and set a unique SCSI ID on the drive. Refer to the SCSI drives manufacturers User Manual for details.

11. Insert the drive or cradle into one of the appropriate sections of the enclosure.

12. Mount four screws to the two sides of the drive bracket to allow the device to remain securely fastened. Note - These screws should be supplied with the drive.

13. Connect the Drive Bracket SCSI extender cable to the internal SCSI cable connector.

14. Connect the power loom on to the back of the cradle or disk drive.

15. Insert the drive bracket back into the Engine and attach the three bolts and fan power cable again.

16. Reattach the front panel, remembering to attach the fan power loom to the F1 connector on the backplane and connect the two power connectors onto the back of the Power On switch.

5.3 Installing External Hard Disk Drives

An additional SCSI controller can be added to the system and fitted in one of three PCI slots on the PXY Main Processor Board. With thecontroller physically installed an additional 4 SCSI devices can be connected to the system bringing the available devices allowed to 7.

All cabling to SCSI devices must be kept as short as possible and the Buss must be terminated using an active SCSI terminator plugged into the last drive in the chain. SCSI I.D.'s can be 0 through to 6. SCSI I.D. 7 is reserved for the internal SCSI controller.

Some disks have SCSI terminating resistors in place and this should be checked and resistors removed when extra disks are being added to the system. Lower transfer rates and SCSI errors will result if the buss is not correctly terminated.

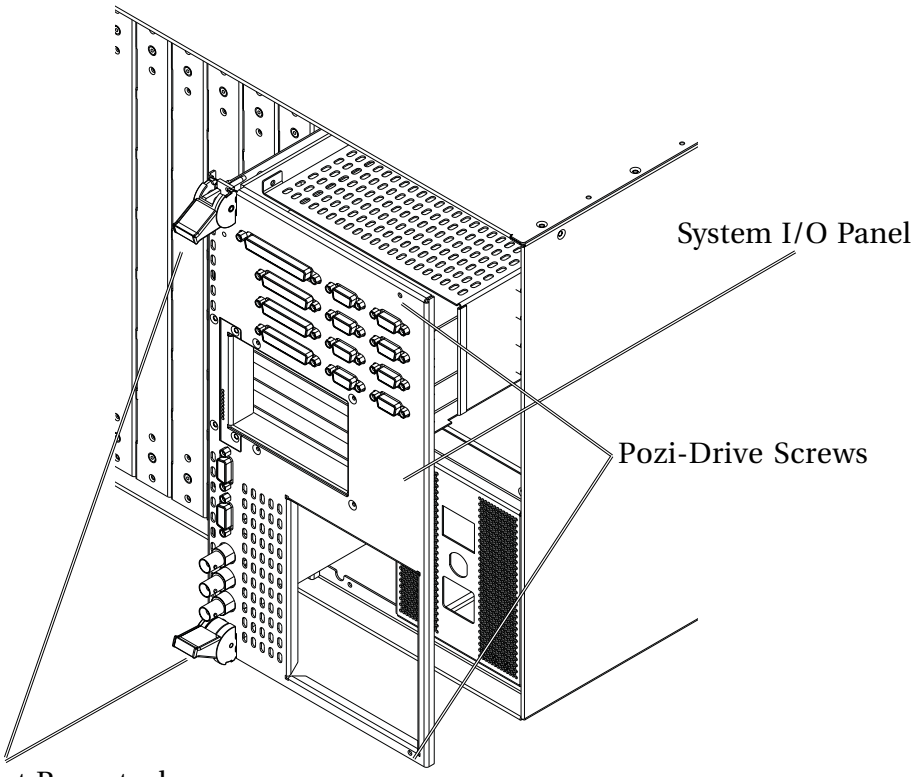
5.3.1 Adding An Additional SCSI Card

1. Remove the pozi-drive screws using a posi-drive screwdriver.

2. The System I/O Panel must be removed from the Engine. Pull outwards the two compact PCI receptacle holders and slowly pull the panel out from the back of the Engine.

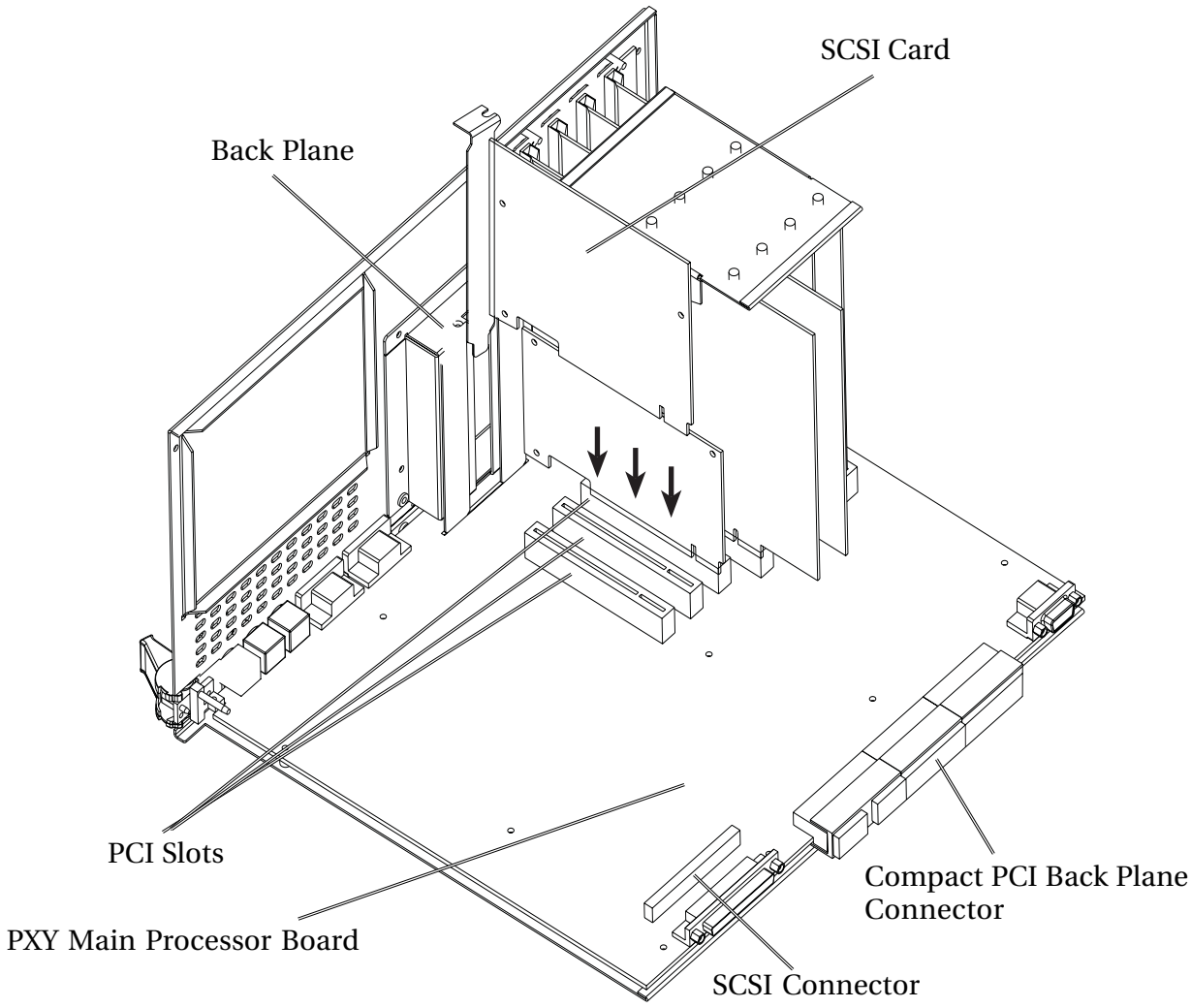
3. Next remove the SCSI loom from the PXY Main Processor Board and fully remove the System I/O Panel from the Engine and lay it horizontally on a anti static surface.

WARNING - MAKE SURE ANTI-STATIC PRECAUTIONS HAVE BEEN TAKEN BEFORE COMMENCING WORK ON THE Engine AND PXY MAIN PROCESSOR BOARD



4. Lay the System I/O Panel on its side so that the PXY Main Processor Board is horizontal.

5. Choose one of the available PCI slots on the PXY Main Processor Board and remove the blanking plate. Remember to remove the screw holding the plate in place !



Horizontal PXY Main Processor / System I/O Panel

6. Insert the SCSI Card into the PCI slot, making sure the connectors are fully inserted

7. Screw the Card onto the back plane.

8. Insert the System I/O Panel back into the Engine, being careful to reconnect to the compact PCI back plane.

9. Before fully inserting the System I/O Panel, reattach the SCSI loom to the SCSI connector on the PXY Main Processor Board.

10. Pull the PCI Receptacle holders inwards.

11. Replace the pozi-drive screws.

12. The physical installation is now complete.

5.4 Checking for Newly Installed SCSI Devices

Once you have mounted all external and internal SCSI devices, the following will aid you in determining if they are all detected.

1. Ensure that the Engine is completely reassembled and that there are no loose cables.

2. Power up the Engine and Console.

3. Press the SPACE BAR once a gray display is seen. If you miss the time window in which the Space bar must be pressed, simply reboot and try again.

4. The displayed prompt is " Select a boot method from the above menu: ".

5. From the prompt type " SCAN " < RETURN >.

6. Observe that all SCSI devices are detected.

7. You may need to run this command a couple of times as some drives are much slower to boot than the Engine.

8. If a SCSI device is not seen, power down the system and check all SCSI ID's and that the SCSI and power cables are connected.

5.6 Setting up SCSI Hard Disk Drives

Disk Drives can be low level formatted on a standard SCSI PC. Once the drive has been formatted, running the Diskinit command on the drive via the Engine will allow correct operation.

The Merlin can operate under two types of disk protocol -

- RBF - OS/9 protocol used on the MFX range of Fairlight products. Can format disks with up to a maximum size of a 4 GB's.
- FLFS - Fairlight disk protocol designed to accommodate disk drives with a partion greater than 4 GB's.

The Merlin system disk comes formatted as an FLFS disk. FLFS and RBF based media disk drives can be connected on the same SCSI buss without any conflicts.

To format a disk, Exit the Disk Recorder by typing 'QUIT' < Return > 'Y'

The displayed prompt is " # ". Then type -

For FLFS - Type DISKINIT /tdwx -w -n=name

< RETURN >.

(Where **td** is the raw device desriptor, **W** is the PCI slot number, 0 is on board, and 1 is the first PCI slot and **X** is the SCSI address of the device)

For RBF - Type DISKINIT / dwx -c=128 -v=1024

< RETURN >.

If a new boot drive is attached to the system the DISKINIT command can be run from system ROM, i.e. you do not need to boot from a drive with software. The following procedure outlines the steps:-

1. Connect the drive that requires setup.

2. Power up the Engine.

3. Press the SPACE BAR immediately on power up.

4. The displayed prompt is " Select a boot method from the above menu: ".

5. Type " ROM " < Return >. This will cause the system to boot from Rom.

6. Type the Diskinit command as outlined above.

7. The drive will be set up for software.

If after you have completed the above, you wish to install software from Exabyte complete the following;

1. Place the Exabyte tape in the Exabyte drive.

2. The displayed prompt is "#".

3. Type " UPGRADE -T " < Return >.

4. Follow the prompts and select the desired drive.

5. Software will be installed and the system will reboot.

Before connecting the drive to a system ensure that there are no SCSI ID conflicts, i.e. that a drive is not already connected with the same ID of the drive you are about to connect.

Drives being setup to be used on the system should have all internal termination's and termination power turned off. In all applications the termination power is supplied by the Engine. Termination is achieved by use of external terminators on the last device on the chain.

SCSI busses should be terminated at the beginning and end of the chain only. The internal SCSI buss is terminted on the motherboard and at the other end of the cable loom by an active terminator.

CAUTION - FAIRLIGHT FORMATTED FLFS DISK DRIVES MUST NOT BE CONNECTED TO WINDOWS NT PC BASED COMPUTERS. CORRUPTION AND DATA LOSS WILL RESULT

For file exchange, some drives may be formatted differently. Consult the File Exchange Manual for further guidance or contact your local Fairlight office or distributer.

5.7 Setting Up Removable Media Devices

To set up optical drives for use on the system it is not necessary to format the media. All that is required is that the following command be run on the media;

DISKINIT /tdwx -w -n=name

(W is the PCI #, X is the SCSI ID)

This command must be run from the shell, so you will need to quit from the main application to the shell.

When media is not in use it is strongly recommended that the media is ejected from the drive to ensure that the media has not deteriorated due to the level of heat in the drive itself.

> CAUTION - KEEP MEDIA AWAY FROM STRONG MAGNETIC FIELDS AND DIRECT SUN LIGHT AS THIS CAN DAMAGE THE DISK.

Please note - The system automatically detects new SCSI devices. For example if an Optical drive is connected at boot up and the media is not present the device will be seen on the Project page, however it will indicate no media. On placing a suitable formatted media in the drive the device will become available for use.

Hard drives will also be automatically detected if they are installed correctly.

Please avoid connecting external devices by breaking the SCSI chain while the system is running as it can either crash the system or if a project is open, lead to project corruption.

Section 6 - Connecting to a Local Area Network

The Merlin can be connected to a Local area network and run as part of a Fairlight Media Link network providing connectivity to other Merlin systems and the MFX range of Digital Audio Workstations.

For more details regarding connecting to a network please contact a local Fairlight office or distributor or read the *Media Link Installation and User Manuals.*

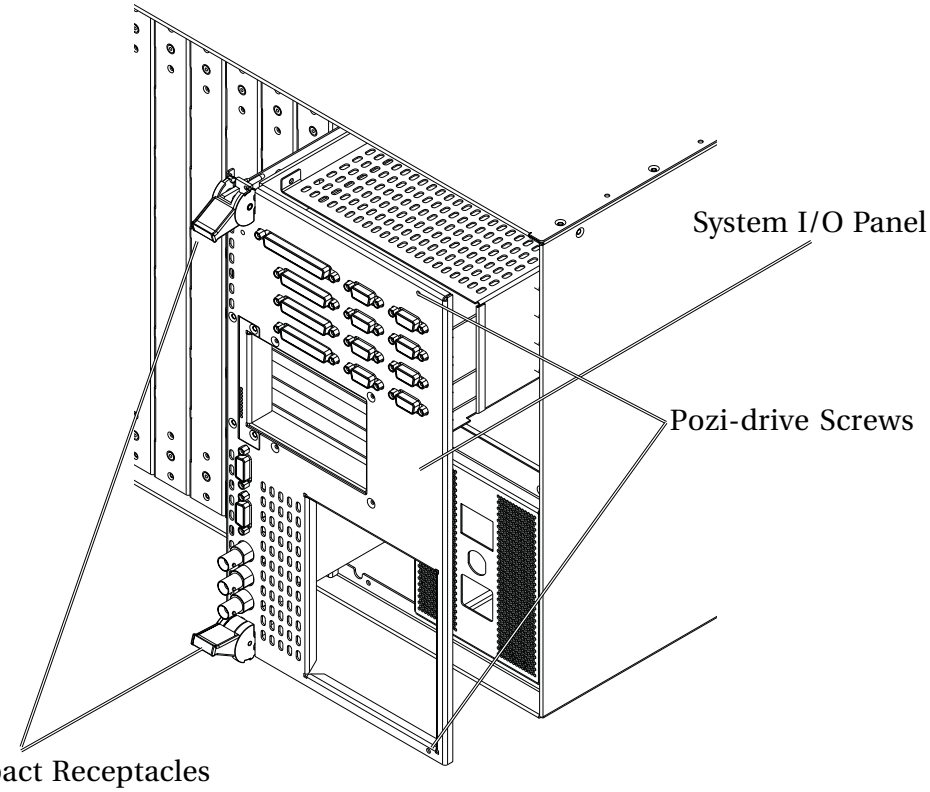
6.0.1 Adding a Network Card

1 Remove the pozi-drive screws from the panel, using a pozi-drive screwdriver.

2 First, the System I/O Panel must be removed from the Engine. Pull outwards the two compact PCI receptacle holders and slowly pull the panel out from the back of the Engine.

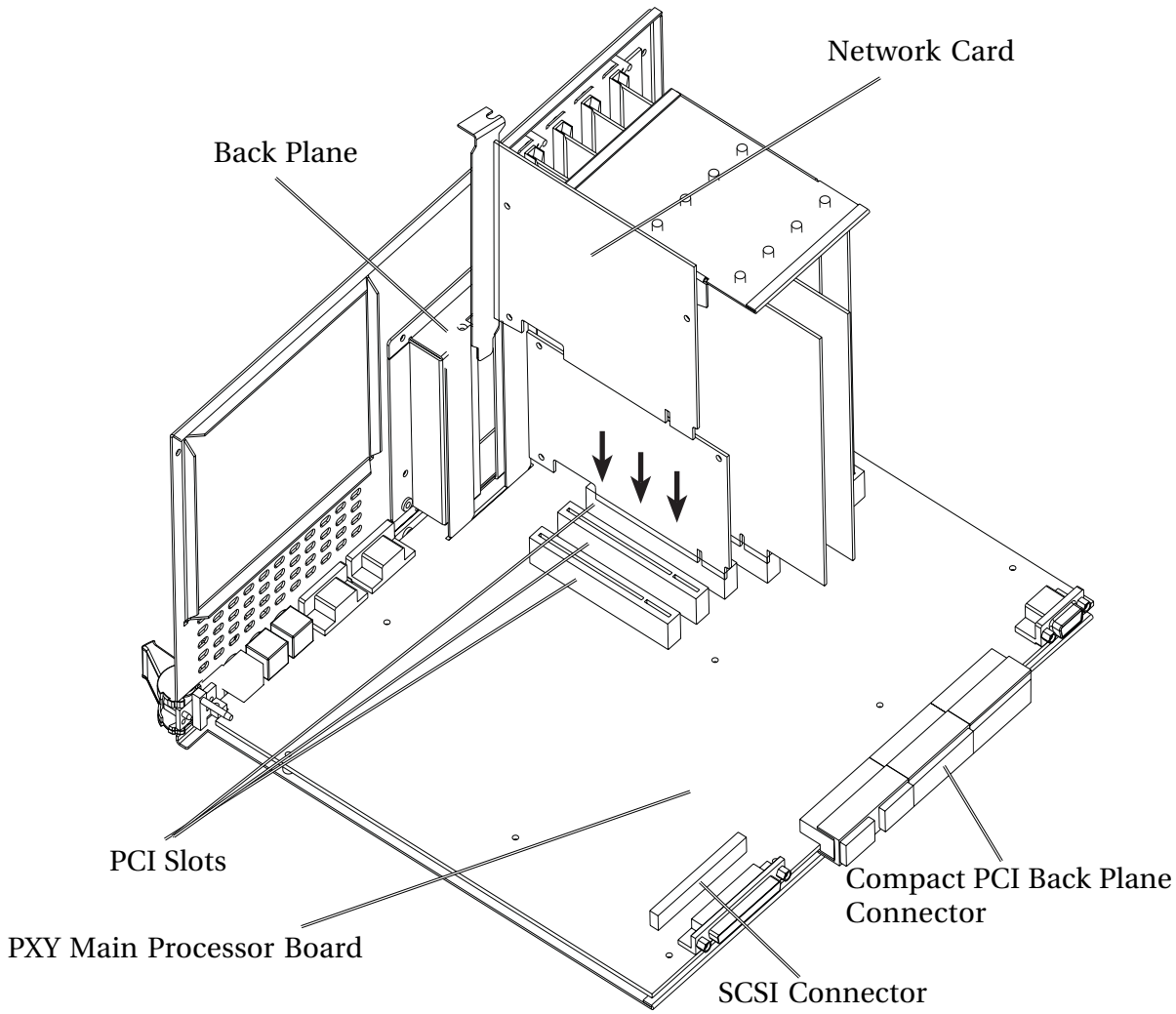
3 Next remove the SCSI loom from the PXY Main Processor Board and fully remove the System I/O Panel from the Engine and lay it horizontally on an anti static surface.

WARNING - MAKE SURE ANTI-STATIC PRECAUTIONS HAVE BEEN TAKEN BEFORE COMMENCING WORK ON THE Engine AND PXY MAIN PROCESSOR BOARD



4 Lay the System I/O Panel on its side so that the PXY Main Processor Board is horizontal.

5 Choose one of the available PCI slots on the PXY Main Processor Board and remove the blanking plate. Remember to remove the screw holding the plate in place !



Horizontal PXY Main Processor Board / System I/O Panel

6 Insert the Network Card into the PCI slot, making sure the connectors are fully inserted.

7 Screw the Card onto the back plane.

8 Insert the System I/O Panel back into the Engine, being careful to reconnect to the compact PCI back plane.

9 Before fully inserting the System I/O Panel, reattach the SCSI loom to the SCSI connector on the PXY Main Processor Board.

10 Pull the PCI receptacles holders inwards .

11 Replace pozi-drive screws.

12 The physical installation is now complete.

Section 7 - Routine Maintenance

6.1 Cleaning The Exterior Of The Units

You should clean the Merlin system units often enough to prevent dust or dirt from accumulating. Dirt acts as a thermal insulating blanket that prevents effective heat dissipation and may provide high-resistance electrical leakage paths between conductors or components in a humid environment.

Clean the dust from the outside by wiping with a soft cloth or small brush. A brush is especially useful for removing dust from around connectors and cooling grilles. Use a cloth dampened in water that contains 50% Isopropyl alcohol to remove hardened dirt. You should not use abrasive cleaners.

6.2 Cleaning The Monitor Screens

The Graphics Monitor has a special coating on the screen which prevents glare. A cleaning cloth should be supplied with the Graphics Monitor and the instructions given in the monitor manual should be followed.

6.3 Cleaning The Engine Air Filter

To ensure good airflow through the Engine, the air filter in the front panel must be periodically cleaned. It is usually sufficient to simply remove accumulated dust using a vacuum cleaner to suck it out of the front panel grille. From time to time, however, the front panel will have to be removed to give the filter a thorough clean or even replace it altogether. The front dress panel should removed to allow access to the Air Filter.

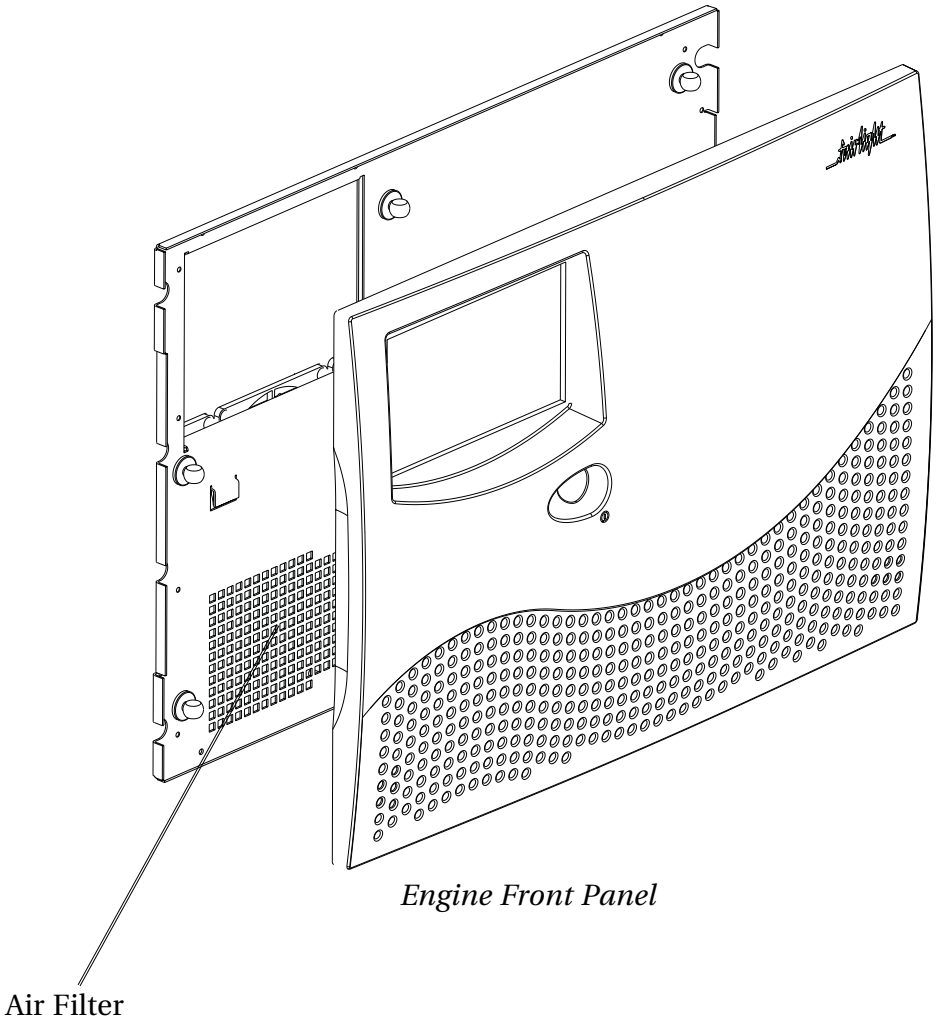
1. Gently lift the dress panel away from the Engine.

2. Unclip the Air Filter and remove it from the front facia of the 2nd panel.

3. Once the air filter has been removed, clean it thoroughly by washing it in warm water with mild detergent. Make sure it is completely dry before reinstalling it.

CAUTION: DO NOT ALLOW WATER TO GET INSIDE ANY ENCLOSED ASSEMBLY OR COMPONENT. DO NOT CLEAN ANY PLASTIC MATERIALS WITH ORGANIC CLEANING SOLVENTS, SUCH AS BENZENE, TOLUENE, XYLENE, ACETONE, OR SIMILAR COMPOUNDS, BECAUSE THEY MAY DAMAGE THE PLASTIC. CAUTION: DO NOT USE CLEANING FLUIDS, OTHER THAN THOSE MENTIONED IN THE GRAPHICS MONITOR MANUAL, TO CLEAN THE SCREEN - THE SPECIAL COATING COULD BE DAMAGED.

4. Reverse the above steps to attach the front dress panel back into place.



Engine Front Panel

New Air Filters

If the filter cannot be cleaned properly or is worn out, a new one should be ordered. Please contact your local Fairlight office or Distributor.

APPENDIX - CONNECTION SPECIFICATIONS

INTRODUCTION

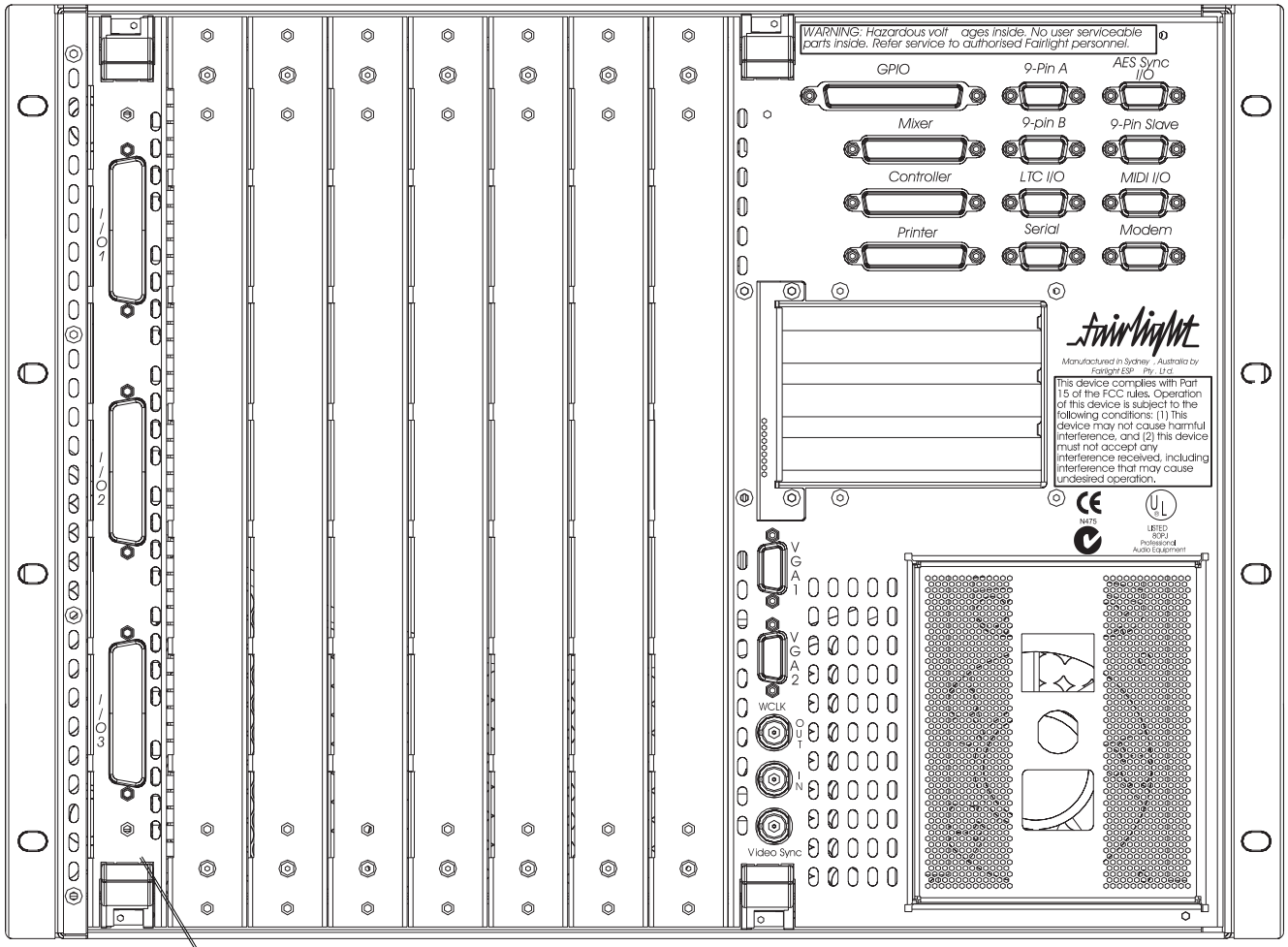
The following information contains all the wiring details to allow users to connect peripheral devices to the back panel of the Engine.

A1 - AUDIO I/O CONFIGURATION

Merlin uses a Fairlight ESP designed proprietary card called the QDC for all its audio I/O and processing. A number of QDC cards can be configured within a Engine. Merlin can be ordered with any of 12 Audio I/O combinations.

On each QDC , a maximum of 6 I/O module boards, can be configured, to allow 8 I/O channels per module. This allows for a maximum of 16 analog inputs and 32 analog outputs or 32 digital inputs / outputs and 16 analog inputs per QDC to be available.

The following pages describe the wiring pin outs for each QDC, to enable installation personnel to configure and wire the system.

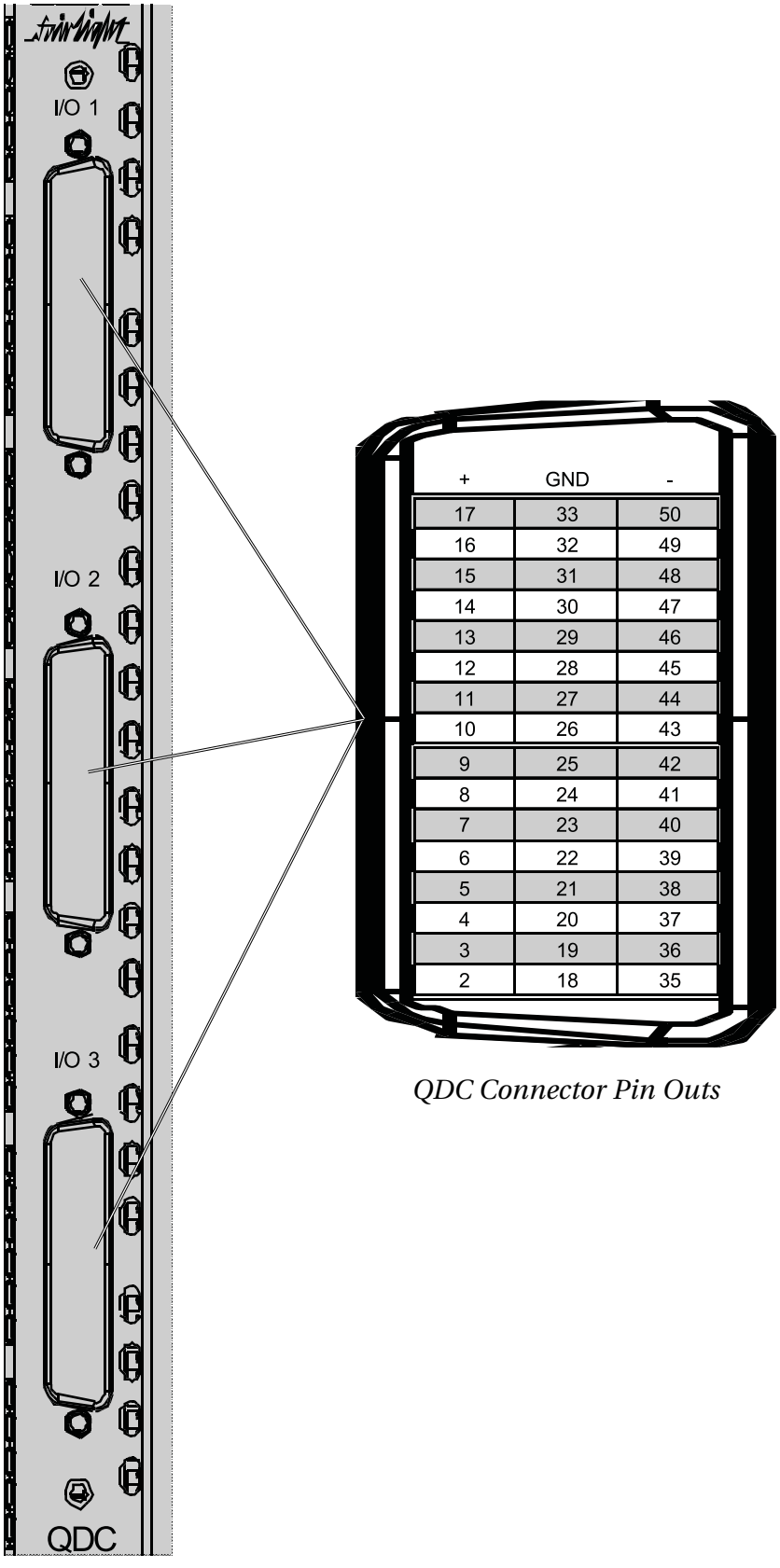


Engine Rear Panel

QDC card

QDC Configuration

Each QDC card comes with three connectors, each housing 50 pins. The following tables show the Audio I/O Configurations - the connectors and Pinouts for Merlin. In some configurations more than one QDC card is required to enable all analog and digital I/O.



+	GND	-
17	33	50
16	32	49
15	31	48
14	30	47
13	29	46
12	28	45
11	27	44
10	26	43
9	25	42
8	24	41
7	23	40
6	22	39
5	21	38
4	20	37
3	19	36
2	18	35

QDC Connector Pin Outs

A1.1 Analog Audio I/O Specifications

Connector	50 way 3 Row D Female
Input	Balanced
Input Level	+24dbu max
Input Sensitivity	+4dbu nominal (adjustable)
Input Impedence	> 10k Ohms
Output	Electronic balanced differential
Output Level	+24dbu max at 0dBFS, nominal +4dbu
Output Impedence	< 55 Ohms
Output Load	>600 Ohms

A1.2 Digital Audio I/O Specifications

Connector	50 way 3 row D Female
Channels	16 stereo pairs per I/O Module
Sample Rates	32KHz, 44.1 KHz, 48Khz, 88.2KHz, 96 KHz,
	0.1% run up and run down
Input Type	> 200mV differential
Output level	>4.3V TTL

1.1.1 24 Track Digital 24 Digital I/Os 1 QDC Card

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	1	3	9	25	42
D In 19 - 20			8	24	41
D In 21 - 22			7	23	40
D In 23 - 24			6	22	39

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	1	3	5	21	38
D Out 19 - 20			4	20	37
D Out 21 - 22			3	19	36
D Out 23 - 24			2	18	35

1.1.2 24 Track Mixed I/O 24 Digital I/Os 8 Analog Inputs 1 QDC Card

Analog Inputs

Port	QDC	Con	Pins		
			+	GND	-
A In 1	1	1	17	33	50
A In 2			16	32	49
A In 3			15	31	48
A In 4			14	30	47
A In 5			13	29	46
A In 6			12	28	45
A In 7			11	27	44
A In 8			10	26	43

Analog Outputs

Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs

Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	1	3	9	25	42
D In 19 - 20			8	24	41
D In 21 - 22			7	23	40
D In 23 - 24			6	22	39

Digital Outputs

Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	1	3	5	21	38
D Out 19 - 20			4	20	37
D Out 21 - 22			3	19	36
D Out 23 - 24			2	18	35

1.1.3 24 Track Analog 24 Analog Inputs 24 Analog Outputs 2 QDC Cards

Analog Inputs						Analog Outputs						Digital Inputs						Digital Outputs					
Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins		
			+	GND	-				+	GND	-				+	GND	-				+	GND	-
A In 1	1	1	17	33	50	A Out 1	1	1	9	25	42												
A In 2			16	32	49	A Out 2			8	24	41												
A In 3			15	31	48	A Out 3			7	23	40												
A In 4			14	30	47	A Out 4			6	22	39												
A In 5			13	29	46	A Out 5			5	21	38												
A In 6			12	28	45	A Out 6			4	20	37												
A In 7			11	27	44	A Out 7			3	19	36												
A In 8			10	26	43	A Out 8			2	18	35												
A In 9	1	3	17	33	50	A Out 9	1	3	9	25	42												
A In 10			16	32	49	A Out 10			8	24	41												
A In 11			15	31	48	A Out 11			7	23	40												
A In 12			14	30	47	A Out 12			6	22	39												
A In 13			13	29	46	A Out 13			5	21	38												
A In 14			12	28	45	A Out 14			4	20	37												
A In 15			11	27	44	A Out 15			3	19	36												
A In 16			10	26	43	A Out 16			2	18	35												
A In 17	2	1	17	33	50	A Out 17	1	2	17	33	50												
A In 18			16	32	49	A Out 18			16	32	49												
A In 19			15	31	48	A Out 19			15	31	48												
A In 20			14	30	47	A Out 20			14	30	47												
A In 21			13	29	46	A Out 21			13	29	46												
A In 22			12	28	45	A Out 22			12	28	45												
A In 23			11	27	44	A Out 23			11	27	44												
A In 24			10	26	43	A Out 24			10	26	43												

1.1.4 24 Track Analog plus Digital 24 Digital I/Os – 24 Analog Inputs – 24 Analog Outputs

Analog Inputs

Port	QDC	Con	Pins +	GND	-
A In 1	1	1	17	33	50
A In 2			16	32	49
A In 3			15	31	48
A In 4			14	30	47
A In 5			13	29	46
A In 6			12	28	45
A In 7			11	27	44
A In 8			10	26	43
A In 9	1	3	17	33	50
A In 10			16	32	49
A In 11			15	31	48
A In 12			14	30	47
A In 13			13	29	46
A In 14			12	28	45
A In 15			11	27	44
A In 16			10	26	43
A In 17	2	1	17	33	50
A In 18			16	32	49
A In 19			15	31	48
A In 20			14	30	47
A In 21			13	29	46
A In 22			12	28	45
A In 23			11	27	44
A In 24			10	26	43

Analog Outputs

Port	QDC	Con	Pins +	GND	-
A Out 1	1	1	9	25	42
A Out 2			8	24	41
A Out 3			7	23	40
A Out 4			6	22	39
A Out 5			5	21	38
A Out 6			4	20	37
A Out 7			3	19	36
A Out 8			2	18	35
A Out 9	1	3	17	33	50
A Out 10			16	32	49
A Out 11			15	31	48
A Out 12			14	30	47
A Out 13			13	29	46
A Out 14			12	28	45
A Out 15			11	27	44
A Out 16			10	26	43
A Out 17	2	1	9	25	42
A Out 18			8	24	41
A Out 19			7	23	40
A Out 20			6	22	39
A Out 21			5	21	38
A Out 22			4	20	37
A Out 23			3	19	36
A Out 24			2	18	35

Digital Inputs

Port	QDC	Con	Pins +	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	2	2	17	33	50
D In 19 - 20			16	32	49
D In 21 - 22			15	31	48
D In 23 - 24			14	30	47

Digital Outputs

Port	QDC	Con	Pins +	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	2	2	13	29	46
D Out 19 - 20			12	28	45
D Out 21 - 22			11	27	44
D Out 23 - 24			10	26	43

2.1.1 32 Track Digital 32 Digital I/Os 2 QDC Cards

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	1	3	9	25	42
D In 19 - 20			8	24	41
D In 21 - 22			7	23	40
D In 23 - 24			6	22	39
D In 25 - 26	2	1	17	33	50
D In 27 - 28			16	32	49
D In 29 - 30			15	31	48
D In 31 - 32			14	30	47

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	1	3	5	21	38
D Out 19 - 20			4	20	37
D Out 21 - 22			3	19	36
D Out 23 - 24			2	18	35
D Out 25 - 26	2	1	13	29	46
D Out 27 - 28			12	28	45
D Out 29 - 30			11	27	44
D Out 31 - 32			10	26	43

2.1.2 32 Track Mixed I/O 32 Digital I/O – 16 Analog Inputs 1 QDC Card

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-
A In 1	1	1	17	33	50
A In 2			16	32	49
A In 3			15	31	48
A In 4			14	30	47
A In 5			13	29	46
A In 6			12	28	45
A In 7			11	27	44
A In 8			10	26	43
A In 9	1	3	17	33	50
A In 10			16	32	49
A In 11			15	31	48
A In 12			14	30	47
A In 13			13	29	46
A In 14			12	28	45
A In 15			11	27	44
A In 16			10	26	43

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	2	2	17	33	50
D In 19 - 20			16	32	49
D In 21 - 22			15	31	48
D In 23 - 24			14	30	47
D In 25 - 26	2	2	9	25	42
D In 27 - 28			8	24	41
D In 29 - 30			7	23	40
D In 31 - 32			6	22	39

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	2	2	13	29	46
D Out 19 - 20			12	28	45
D Out 21 - 22			11	27	44
D Out 23 - 24			10	26	43
D Out 25 - 26	2	2	5	21	38
D Out 27 - 28			4	20	37
D Out 29 - 30			3	19	36
D Out 31 - 32			2	18	35

2.1.3 32 Track Analog 32 Analog Inputs 32 Analog Outputs 2 QDC Cards

Analog Inputs						Analog Outputs						Digital Inputs						Digital Outputs					
Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins		
			+	GND	-				+	GND	-				+	GND	-				+	GND	-
A In 1	1	1	17	33	50	A Out 1	1	1	9	25	42												
A In 2			16	32	49	A Out 2			8	24	41												
A In 3			15	31	48	A Out 3			7	23	40												
A In 4			14	30	47	A Out 4			6	22	39												
A In 5			13	29	46	A Out 5			5	21	38												
A In 6			12	28	45	A Out 6			4	20	37												
A In 7			11	27	44	A Out 7			3	19	36												
A In 8			10	26	43	A Out 8			2	18	35												
A In 9	1	3	17	33	50	A Out 9	1	3	9	25	42												
A In 10			16	32	49	A Out 10			8	24	41												
A In 11			15	31	48	A Out 11			7	23	40												
A In 12			14	30	47	A Out 12			6	22	39												
A In 13			13	29	46	A Out 13			5	21	38												
A In 14			12	28	45	A Out 14			4	20	37												
A In 15			11	27	44	A Out 15			3	19	36												
A In 16			10	26	43	A Out 16			2	18	35												
A In 17	2	1	17	33	50	A Out 17	1	2	9	25	42												
A In 18			16	32	49	A Out 18			8	24	41												
A In 19			15	31	48	A Out 19			7	23	40												
A In 20			14	30	47	A Out 20			6	22	39												
A In 21			13	29	46	A Out 21			5	21	38												
A In 22			12	28	45	A Out 22			4	20	37												
A In 23			11	27	44	A Out 23			3	19	36												
A In 24			10	26	43	A Out 24			2	18	35												
A In 25	2	3	17	33	50	A Out 25	1	2	17	33	50												
A In 26			16	32	49	A Out 26			16	32	49												
A In 27			15	31	48	A Out 27			15	31	48												
A In 28			14	30	47	A Out 28			14	30	47												
A In 29			13	29	46	A Out 29			13	29	46												
A In 30			12	28	45	A Out 30			12	28	45												
A In 31			11	27	44	A Out 31			11	27	44												
A In 32			10	26	43	A Out 32			10	26	43												

2.1.4 32 Track Analog plus Digital 32 Digital I/Os – 32 Analog Inputs – 32 Analog Outputs

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-
A In 1	1	1	17	33	50
A In 2			16	32	49
A In 3			15	31	48
A In 4			14	30	47
A In 5			13	29	46
A In 6			12	28	45
A In 7			11	27	44
A In 8			10	26	43
A In 9	1	3	17	33	50
A In 10			16	32	49
A In 11			15	31	48
A In 12			14	30	47
A In 13			13	29	46
A In 14			12	28	45
A In 15			11	27	44
A In 16			10	26	43
A In 17	2	1	17	33	50
A In 18			16	32	49
A In 19			15	31	48
A In 20			14	30	47
A In 21			13	29	46
A In 22			12	28	45
A In 23			11	27	44
A In 24			10	26	43
A In 25	2	3	17	33	50
A In 26			16	32	49
A In 27			15	31	48
A In 28			14	30	47
A In 29			13	29	46
A In 30			12	28	45
A In 31			11	27	44
A In 32			10	26	43

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-
A Out 1	1	1	9	25	42
A Out 2			8	24	41
A Out 3			7	23	40
A Out 4			6	22	39
A Out 5			5	21	38
A Out 6			4	20	37
A Out 7			3	19	36
A Out 8			2	18	35
A Out 9	1	3	9	25	42
A Out 10			8	24	41
A Out 11			7	23	40
A Out 12			6	22	39
A Out 13			5	21	38
A Out 14			4	20	37
A Out 15			3	19	36
A Out 16			2	18	35
A Out 17	2	1	9	25	42
A Out 18			8	24	41
A Out 19			7	23	40
A Out 20			6	22	39
A Out 21			5	21	38
A Out 22			4	20	37
A Out 23			3	19	36
A Out 24			2	18	35
A Out 25	2	3	9	25	42
A Out 26			8	24	41
A Out 27			7	23	40
A Out 28			6	22	39
A Out 29			5	21	38
A Out 30			4	20	37
A Out 31			3	19	36
A Out 32			2	18	35

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	2	2	17	33	50
D In 19 - 20			16	32	49
D In 21 - 22			15	31	48
D In 23 - 24			14	30	47
D In 25 - 26	2	2	9	25	42
D In 27 - 28			8	24	41
D In 29 - 30			7	23	40
D In 31 - 32			6	22	39

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	2	2	13	29	46
D Out 19 - 20			12	28	45
D Out 21 - 22			11	27	44
D Out 23 - 24			10	26	43
D Out 25 - 26	2	2	5	21	38
D Out 27 - 28			4	20	37
D Out 29 - 30			3	19	36
D Out 31 - 32			2	18	35

3.1.1 48 Track Digital 48 Digital I/Os

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	1	1	9	25	42
D In 19 - 20			8	24	41
D In 21 - 22			7	23	40
D In 23 - 24			6	22	39
D In 25 - 26	1	3	17	33	50
D In 27 - 28			16	32	49
D In 29 - 30			15	31	48
D In 31 - 32			14	30	47
D In 33 - 34	2	2	17	33	50
D In 35 - 36			16	32	49
D In 37 - 38			15	31	48
D In 39 - 40			14	30	47
D In 41 - 42	2	2	9	25	42
D In 43 - 44			8	24	41
D In 45 - 46			7	23	40
D In 47 - 48			6	22	39

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	1	1	5	21	38
D Out 19 - 20			4	20	37
D Out 21 - 22			3	19	36
D Out 23 - 24			2	18	35
D Out 25 - 26	1	3	13	29	46
D Out 27 - 28			12	28	45
D Out 29 - 30			11	27	44
D Out 31 - 32			10	26	43
D Out 33 - 34	2	2	13	29	46
D Out 35 - 36			12	28	45
D Out 37 - 38			11	27	44
D Out 39 - 40			10	26	43
D Out 41 - 42	2	2	5	21	38
D Out 43 - 44			4	20	37
D Out 45 - 46			3	19	36
D Out 47 - 48			2	18	35

3.1.2 48 Track Mixed I/O 48 Digital I/Os – 24 Analog Inputs

Analog Inputs					
Port	QDC	Con	Pins		
			+	GND	-
A In 1	1	1	17	33	50
A In 2			16	32	49
A In 3			15	31	48
A In 4			14	30	47
A In 5			13	29	46
A In 6			12	28	45
A In 7			11	27	44
A In 8			10	26	43
A In 9	1	3	17	33	50
A In 10			16	32	49
A In 11			15	31	48
A In 12			14	30	47
A In 13			13	29	46
A In 14			12	28	45
A In 15			11	27	44
A In 16			10	26	43
A In 17	2	1	17	33	50
A In 18			16	32	49
A In 19			15	31	48
A In 20			14	30	47
A In 21			13	29	46
A In 22			12	28	45
A In 23			11	27	44
A In 24			10	26	43

Analog Outputs					
Port	QDC	Con	Pins		
			+	GND	-

Digital Inputs					
Port	QDC	Con	Pins		
			+	GND	-
D In 1 - 2	1	2	17	33	50
D In 3 - 4			16	32	49
D In 5 - 6			15	31	48
D In 7 - 8			14	30	47
D In 9 - 10	1	2	9	25	42
D In 11 - 12			8	24	41
D In 13 - 14			7	23	40
D In 15 - 16			6	22	39
D In 17 - 18	2	2	17	33	50
D In 19 - 20			16	32	49
D In 21 - 22			15	31	48
D In 23 - 24			14	30	47
D In 25 - 26	2	2	9	25	42
D In 27 - 28			8	24	41
D In 29 - 30			7	23	40
D In 31 - 32			6	22	39
D In 33 - 34	2	1	9	25	42
D In 35 - 36			8	24	41
D In 37 - 38			7	23	40
D In 39 - 40			6	22	39
D In 41 - 42	3	2	17	33	50
D In 43 - 44			16	32	49
D In 45 - 46			15	31	48
D In 47 - 48			14	30	47

Digital Outputs					
Port	QDC	Con	Pins		
			+	GND	-
D Out 1 - 2	1	2	13	29	46
D Out 3 - 4			12	28	45
D Out 5 - 6			11	27	44
D Out 7 - 8			10	26	43
D Out 9 - 10	1	2	5	21	38
D Out 11 - 12			4	20	37
D Out 13 - 14			3	19	36
D Out 15 - 16			2	18	35
D Out 17 - 18	2	2	13	29	46
D Out 19 - 20			12	28	45
D Out 21 - 22			11	27	44
D Out 23 - 24			10	26	43
D Out 25 - 26	2	2	5	21	38
D Out 27 - 28			4	20	37
D Out 29 - 30			3	19	36
D Out 31 - 32			2	18	35
D Out 33 - 34	2	1	5	21	38
D Out 35 - 36			4	20	37
D Out 37 - 38			3	19	36
D Out 39 - 40			2	18	35
D Out 41 - 42	3	2	13	29	46
D Out 43 - 44			12	28	45
D Out 45 - 46			11	27	44
D Out 47 - 48			10	26	43

3.1.3 48 Track Analog 48 Analog Inputs – 48 Analog Outputs

Analog Inputs						Analog Outputs						Digital Inputs						Digital Outputs					
Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins		
			+	GND	-				+	GND	-				+	GND	-				+	GND	-
A In 1	1	1	17	33	50	A Out 1	1	1	9	25	42												
A In 2			16	32	49	A Out 2			8	24	41												
A In 3			15	31	48	A Out 3			7	23	40												
A In 4			14	30	47	A Out 4			6	22	39												
A In 5			13	29	46	A Out 5			5	21	38												
A In 6			12	28	45	A Out 6			4	20	37												
A In 7			11	27	44	A Out 7			3	19	36												
A In 8			10	26	43	A Out 8			2	18	35												
A In 9	1	3	17	33	50	A Out 9	1	3	9	25	42												
A In 10			16	32	49	A Out 10			8	24	41												
A In 11			15	31	48	A Out 11			7	23	40												
A In 12			14	30	47	A Out 12			6	22	39												
A In 13			13	29	46	A Out 13			5	21	38												
A In 14			12	28	45	A Out 14			4	20	37												
A In 15			11	27	44	A Out 15			3	19	36												
A In 16			10	26	43	A Out 16			2	18	35												
A In 17	2	1	17	33	50	A Out 17	1	2	17	33	50												
A In 18			16	32	49	A Out 18			16	32	49												
A In 19			15	31	48	A Out 19			15	31	48												
A In 20			14	30	47	A Out 20			14	30	47												
A In 21			13	29	46	A Out 21			13	29	46												
A In 22			12	28	45	A Out 22			12	28	45												
A In 23			11	27	44	A Out 23			11	27	44												
A In 24			10	26	43	A Out 24			10	26	43												
A In 25	2	3	17	33	50	A Out 25	1	2	9	25	42												
A In 26			16	32	49	A Out 26			8	24	41												
A In 27			15	31	48	A Out 27			7	23	40												
A In 28			14	30	47	A Out 28			6	22	39												

A In 29			13	29	46	A Out 29			5	21	38
A In 30			12	28	45	A Out 30			4	20	37
A In 31			11	27	44	A Out 31			3	19	36
A In 32			10	26	43	A Out 32			2	18	35
A In 33	3	1	17	33	50	A Out 33	2	1	9	25	42
A In 34			16	32	49	A Out 34			8	24	41
A In 35			15	31	48	A Out 35			7	23	40
A In 36			14	30	47	A Out 36			6	22	39
A In 37			13	29	46	A Out 37			5	21	38
A In 38			12	28	45	A Out 38			4	20	37
A In 39			11	27	44	A Out 39			3	19	36
A In 40			10	26	43	A Out 40			2	18	35
A In 41	3	3	17	33	50	A Out 41	2	3	9	25	42
A In 42			16	32	49	A Out 42			8	24	41
A In 43			15	31	48	A Out 43			7	23	40
A In 44			14	30	47	A Out 44			6	22	39
A In 45			13	29	46	A Out 45			5	21	38
A In 46			12	28	45	A Out 46			4	20	37
A In 47			11	27	44	A Out 47			3	19	36
A In 48			10	26	43	A Out 48			2	18	35

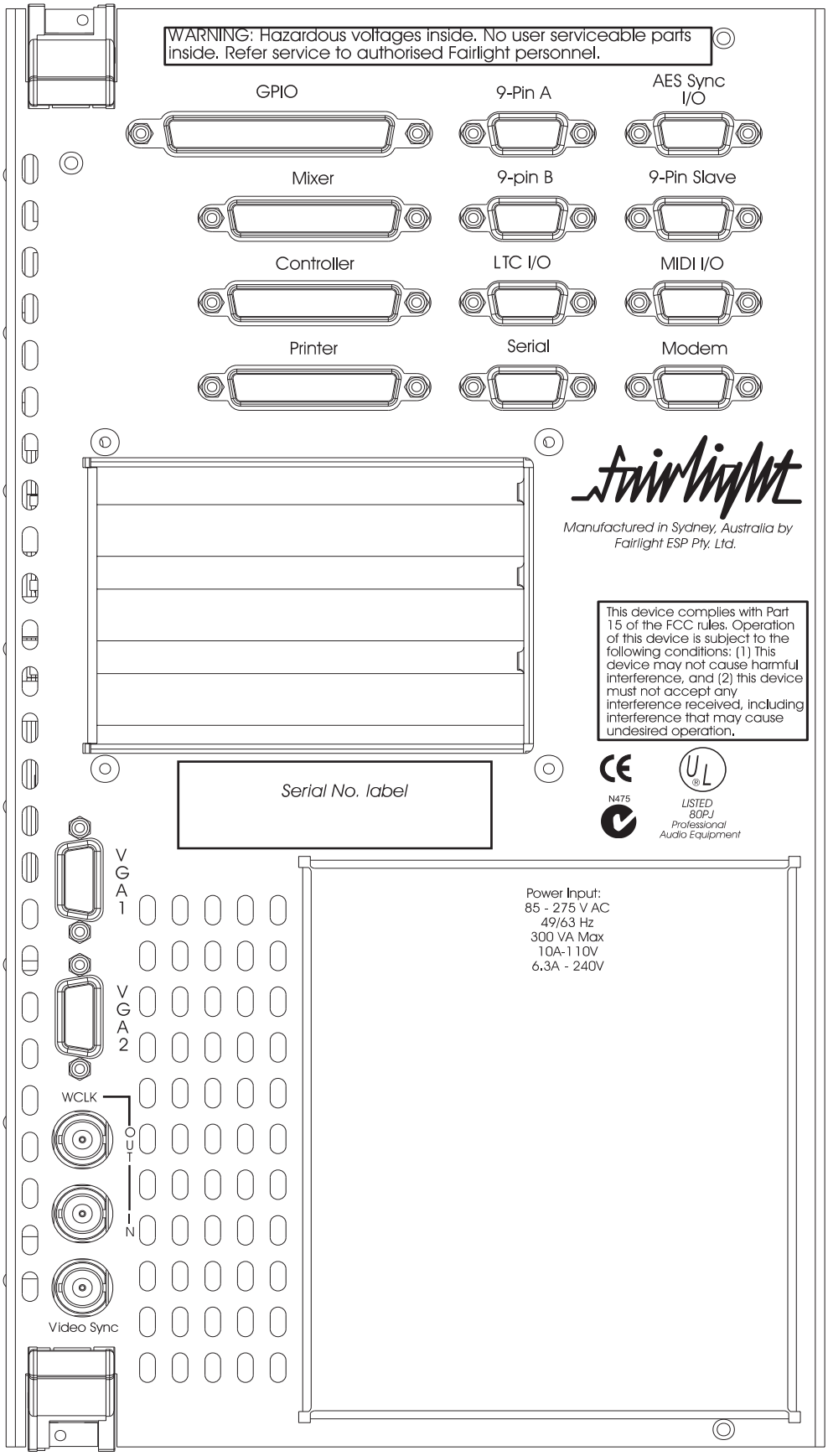
3.1.4 48 Track Analog plus Digital 48 Digital I/Os – 48 Analog Inputs – 48 Analog Outputs

Analog Inputs						Analog Outputs						Digital Inputs						Digital Outputs					
Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins			Port	QDC	Con	Pins		
			+	GND	-				+	GND	-				+	GND	-				+	GND	-
A In 1	1	1	17	33	50	A Out 1	1	1	9	25	42	D In 1 - 2	1	2	17	33	50	D Out 1 - 2	1	2	13	29	46
A In 2			16	32	49	A Out 2			8	24	41	D In 3 - 4			16	32	49	D Out 3 - 4			12	28	45
A In 3			15	31	48	A Out 3			7	23	40	D In 5 - 6			15	31	48	D Out 5 - 6			11	27	44
A In 4			14	30	47	A Out 4			6	22	39	D In 7 - 8			14	30	47	D Out 7 - 8			10	26	43
A In 5			13	29	46	A Out 5			5	21	38	D In 9 - 10	1	2	9	25	42	D Out 9 - 10	1	2	5	21	38
A In 6			12	28	45	A Out 6			4	20	37	D In 11 - 12			8	24	41	D Out 11 - 12			4	20	37
A In 7			11	27	44	A Out 7			3	19	36	D In 13 - 14			7	23	40	D Out 13 - 14			3	19	36
A In 8			10	26	43	A Out 8			2	18	35	D In 15 - 16			6	22	39	D Out 15 - 16			2	18	35
A In 9	1	3	17	33	50	A Out 9	1	3	9	25	42	D In 17 - 18	2	2	17	33	50	D Out 17 - 18	2	2	13	29	46
A In 10			16	32	49	A Out 10			8	24	41	D In 19 - 20			16	32	49	D Out 19 - 20			12	28	45
A In 11			15	31	48	A Out 11			7	23	40	D In 21 - 22			15	31	48	D Out 21 - 22			11	27	44
A In 12			14	30	47	A Out 12			6	22	39	D In 23 - 24			14	30	47	D Out 23 - 24			10	26	43
A In 13			13	29	46	A Out 13			5	21	38	D In 25 - 26	2	2	9	25	42	D Out 25 - 26	2	2	5	21	38
A In 14			12	28	45	A Out 14			4	20	37	D In 27 - 28			8	24	41	D Out 27 - 28			4	20	37
A In 15			11	27	44	A Out 15			3	19	36	D In 29 - 30			7	23	40	D Out 29 - 30			3	19	36
A In 16			10	26	43	A Out 16			2	18	35	D In 31 - 32			6	22	39	D Out 31 - 32			2	18	35
A In 17	2	1	17	33	50	A Out 17	2	1	9	25	42	D In 33 - 34	3	2	17	33	50	D Out 33 - 34	3	2	13	29	46
A In 18			16	32	49	A Out 18			8	24	41	D In 35 - 36			16	32	49	D Out 35 - 36			12	28	45
A In 19			15	31	48	A Out 19			7	23	40	D In 37 - 38			15	31	48	D Out 37 - 38			11	27	44
A In 20			14	30	47	A Out 20			6	22	39	D In 39 - 40			14	30	47	D Out 39 - 40			10	26	43
A In 21			13	29	46	A Out 21			5	21	38	D In 41 - 42	3	2	9	25	42	D Out 41 - 42	3	2	5	21	38
A In 22			12	28	45	A Out 22			4	20	37	D In 43 - 44			8	24	41	D Out 43 - 44			4	20	37
A In 23			11	27	44	A Out 23			3	19	36	D In 45 - 46			7	23	40	D Out 45 - 46			3	19	36
A In 24			10	26	43	A Out 24			2	18	35	D In 47 - 48			6	22	39	D Out 47 - 48			2	18	35
A In 25	2	3	17	33	50	A Out 25	2	3	9	25	42												
A In 26			16	32	49	A Out 26			8	24	41												

A In 27			15	31	48	A Out 27			7	23	40	
A In 28			14	30	47	A Out 28			6	22	39	
A In 29			13	29	46	A Out 29			5	21	38	
A In 30			12	28	45	A Out 30			4	20	37	
A In 31			11	27	44	A Out 31			3	19	36	
A In 32			10	26	43	A Out 32			2	18	35	
A In 33	3	1	17	33	50	A Out 33	3	1	9	25	42	
A In 34			16	32	49	A Out 34			8	24	41	
A In 35			15	31	48	A Out 35			7	23	40	
A In 36			14	30	47	A Out 36			6	22	39	
A In 37			13	29	46	A Out 37			5	21	38	
A In 38			12	28	45	A Out 38			4	20	37	
A In 39			11	27	44	A Out 39			3	19	36	
A In 40			10	26	43	A Out 40			2	18	35	
A In 41	3	3	17	33	50	A Out 41	3	3	9	25	42	
A In 42			16	32	49	A Out 42			8	24	41	
A In 43			15	31	48	A Out 43			7	23	40	
A In 44			14	30	47	A Out 44			6	22	39	
A In 45			13	29	46	A Out 45			5	21	38	
A In 46			12	28	45	A Out 46			4	20	37	
A In 47			11	27	44	A Out 47			3	19	36	
A In 48			10	26	43	A Out 48			2	18	35	

APPENDIX - CONNECTION & SIGNAL SPECIFICATIONS

A2 CONTROL & REFERENCE PINOUTS



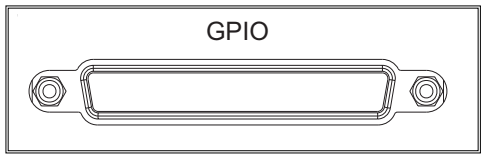
Engine System I/O Panel

A3 General Purpose Interface

Connector 37 Pin D Male

Input TTL (1 LS Load)

Output/Bank TTL (max 5 TTL loads)



1	GND
2	GPIO6
3	GPIO5
4	GND
5	GPIOBO2
6	GPIOBO1
7	GND
8	GPIOIN6
9	GPIOIN5
10	GND
11	GPIOIN2
12	GPIOIN1
13	GND
14	GPIOOUT6
15	GPIOOUT5
16	GND
17	GPIOOUT2
18	GPIOOUT1
19	GND
20	GPI0B07
21	GND
22	GPI
23	GPIOBO3
24	GND
25	GPIOBO0
26	GPIOIN7
27	GND
28	GPIOIN4
29	GPIOIN3
30	GND
31	GPIOINO
32	GPIOOUT7
33	GND
34	GPIOOUT4
35	GPIOOUT3
36	GND
37	GPIOOUT0

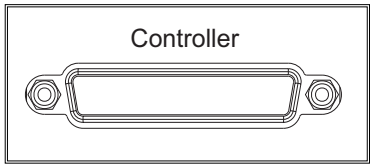
A4 Mixer

Connector 25 pin D Female

1	GND
2	RxFFN
3	RxCLKN
4	RxDATN
5	RxWRN
6	NC
7	NC
8	TxFFN
9	TxCLKN
10	TxDATN
11	TxWRPN
12	HSSLDETn
13	SYNCN
14	RxFFP
15	RxCLKP
16	RxDATP
17	RxWRP
18	NC
19	GND
20	TxFFP
21	TXxCLKP
22	TxDATP
23	TxWRP
24	GND
25	SYNCP

A5 Controller

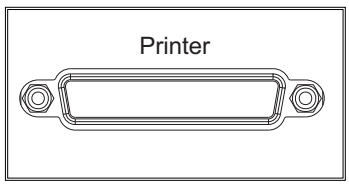
Connector 25 pin D Male



PIN 1	GND
PIN 2	CONTx
PIN 3	CONRx
PIN 4	NC
PIN 5	H_TxDATA
PIN 6	CONPR
PIN 7	GNDC
PIN 8	NC
PIN 9	GNDC
PIN 10	CONTxPOS
PIN 11	CONRxPOS
PIN 12	NC
PIN 13	NC
PIN 14	NC
PIN 15	NC
PIN 16	NC
PIN 17	NC
PIN 18	NC
PIN 19	NC
PIN 20	H_RxDATA
PIN 21	CONPR
PIN 22	CONPR
PIN 23	CONRI
PIN 24	CONRxNEG
PIN 25	NC

A6 PRINTER

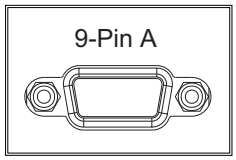
Connector Standard 25 pin D female



PIN 1	PSTROBEn
PIN 2	PDR0
PIN 3	PDR1
PIN 4	PDR2
PIN 5	PDR3
PIN 6	PDR4
PIN 7	PDR5
PIN 8	PDR6
PIN 9	PDR7
PIN 10	PRACKn
PIN 11	PRBUSYn
PIN 12	PRERROR
PIN 13	PRSELECT
PIN 14	PRAUTOFDn
PIN 15	PRFAULTn
PIN 16	PRINTITn
PIN 17	PRSELINn
PIN 18	GND
PIN 19	GND
PIN 20	GND
PIN 21	GND
PIN 22	GND
PIN 23	GND
PIN 24	GND
PIN 25	GND

A8 9-Pin A

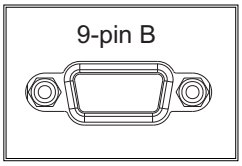
Connector 9 pin D Female



PIN 1	GND
PIN 2	9ARxA
PIN 3	9ATxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9ARxB
PIN 8	9ATxA
PIN 9	NC

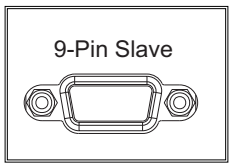
A9 9-Pin B

Connector 9 pin D Female



PIN 1	GND
PIN 2	9BRxA
PIN 3	9BTxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9BRxB
PIN 8	9BTxA
PIN 9	NC

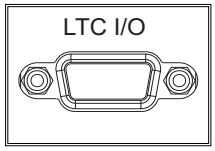
A10 9-Pin Slave



Connector 9 pin D Female

PIN 1	GND
PIN 2	9BTxA
PIN 3	9RRxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9BTxB
PIN 8	9BRxA
PIN 9	GND

A11 LTC - I/O



Connector 9 pin D Male

Input Level -20dbm to +10dbm

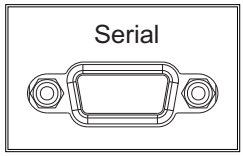
Output Level 0dbm

Important note: Unbalanced loads connected to LTC OUT should NOT ground the LTC OUT NEGATIVE signal.

PIN 1	GND
PIN 2	LTC A NEGATIVE
PIN 3	LTC OUT NEGATIVE
PIN 4	GND
PIN 5	LTC B POSITIVE
PIN 6	LTC A POSITIVE
PIN 7	GND
PIN 8	LTC OUT POSITIVE
PIN 9	LTC B NEGATIVE

A12 Serial Port

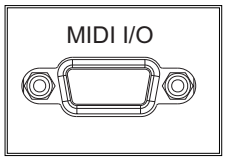
Connector Standard 9 pin D male



PIN 1	SER_DCD
PIN 2	SER_Rx
PIN 3	SER_Tx
PIN 4	SER_DTR
PIN 5	GND
PIN 6	SER_DSR
PIN 7	SER_RTS
PIN 8	SER_CTS
PIN 9	NC

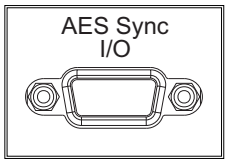
A13 Midi I/O

Connector 9 pin D female



PIN 1	NOT CONNECTED		
PIN 2	MIDI IN NEGATIVE	MIDI IN	DIN PIN 5
PIN 3	MIDI OUT NEGATIVE	MIDI OUT	DIN PIN 5
PIN 4	GND	MIDI THROUGH	DIN PIN 2
PIN 5	MIDI THROUGH POSITIVE	MIDI THROUGH	DIN PIN 4
PIN 6	MIDI POSITIVE	MIDI IN	DIN PIN 4
PIN 7	GND	MIDI OUT	DIN PIN 2
PIN 8	MIDI OUT POSITIVE	MIDI OUT	DIN PIN 4
PIN 9	MIDI THROUGH NEGATIVE	MIDI THROUGH	DIN PIN 5

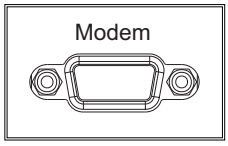
A14 AES Sync I/O



Connector 9 pin D Male

PIN 1	GND
PIN 2	AES IN NEGATIVE
PIN 3	AES OUT POSITIVE
PIN 4	BIPHASE TACH
PIN 5	BIP DIRECTION
PIN 6	AES IN POSITIVE
PIN 7	GND
PIN 8	AES OUT NEGATIVE
PIN 9	NOT CONNECTED

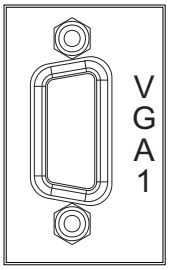
A15 Modem



Connector 9 pin D Male

PIN 1	MOD_DCD
PIN 2	MOD_RX
PIN 3	MOD_TX
PIN 4	MOD_DTR
PIN 5	GND
PIN 6	MOD_DSR
PIN 7	MOD_RTS
PIN 8	MOS_CTS
PIN 9	NC

A16 VGA



Connector 15 pin High Density D Female

Resolution 1024(H) x 768(V)

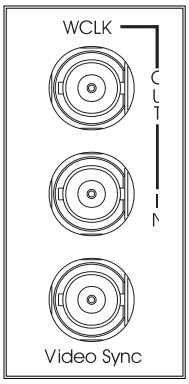
Frequency HSYNC: 60khz VSYNC: 75hz SVGA STANDARD

PIN 1	RED
PIN 2	GREEN
PIN 3	BLUE
PIN 4	GND
PIN 5	GND
PIN 6	GND
PIN 7	GND
PIN 8	GND
PIN 10	GND
PIN 11	GND
PIN 12	NC
PIN 13	HSYNC
PIN 14	VSYNC
PIN 15	NC

A17 Video Sync - In

Connector BNC

Input Level 1V p-p 75 Ohms Terminated Internally



A18 Word Clock - In

Connector BNC

Input Optically Isolated

Output Impedence 75 Ohms

A19 Word Clock - Out

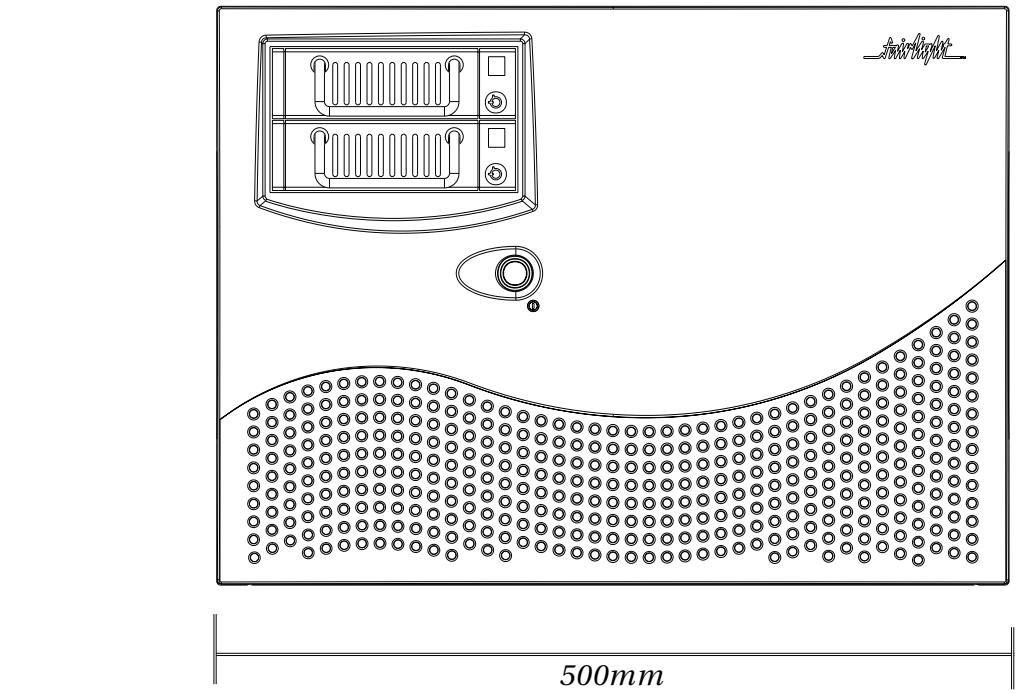
Connector BNC

Output Level > 4.3V TTL

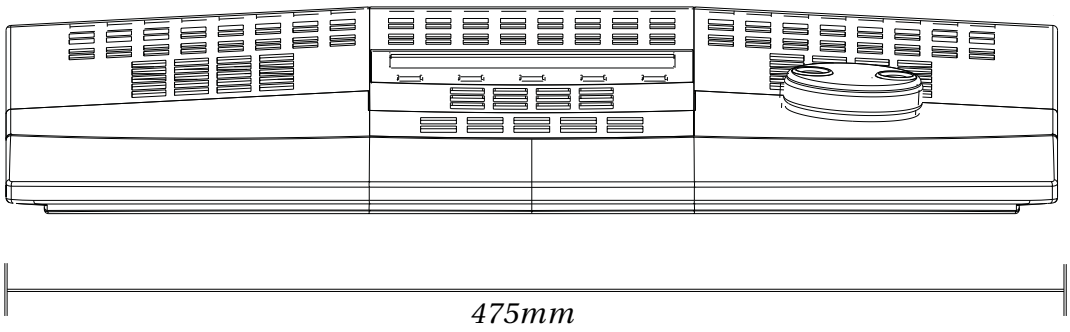
Output Impendence 75 Ohms

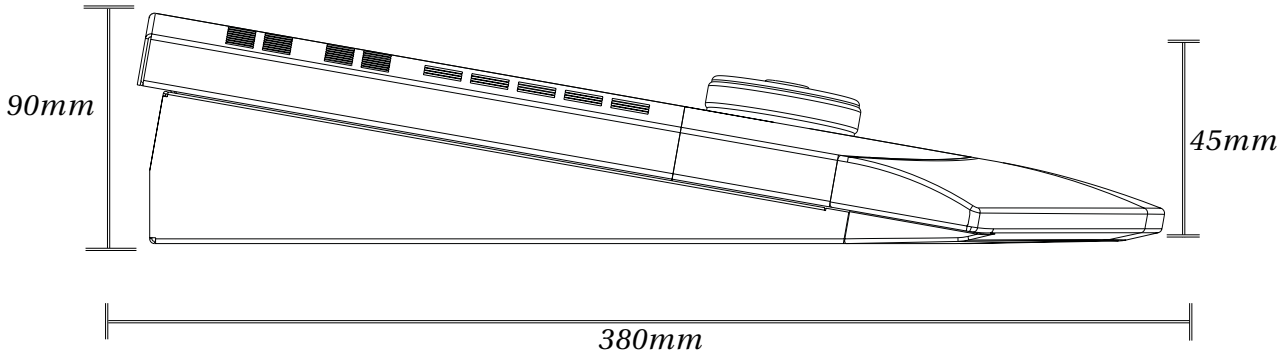
A20 Dimensions

A20.1 Engine



A20.2 Merlin Console





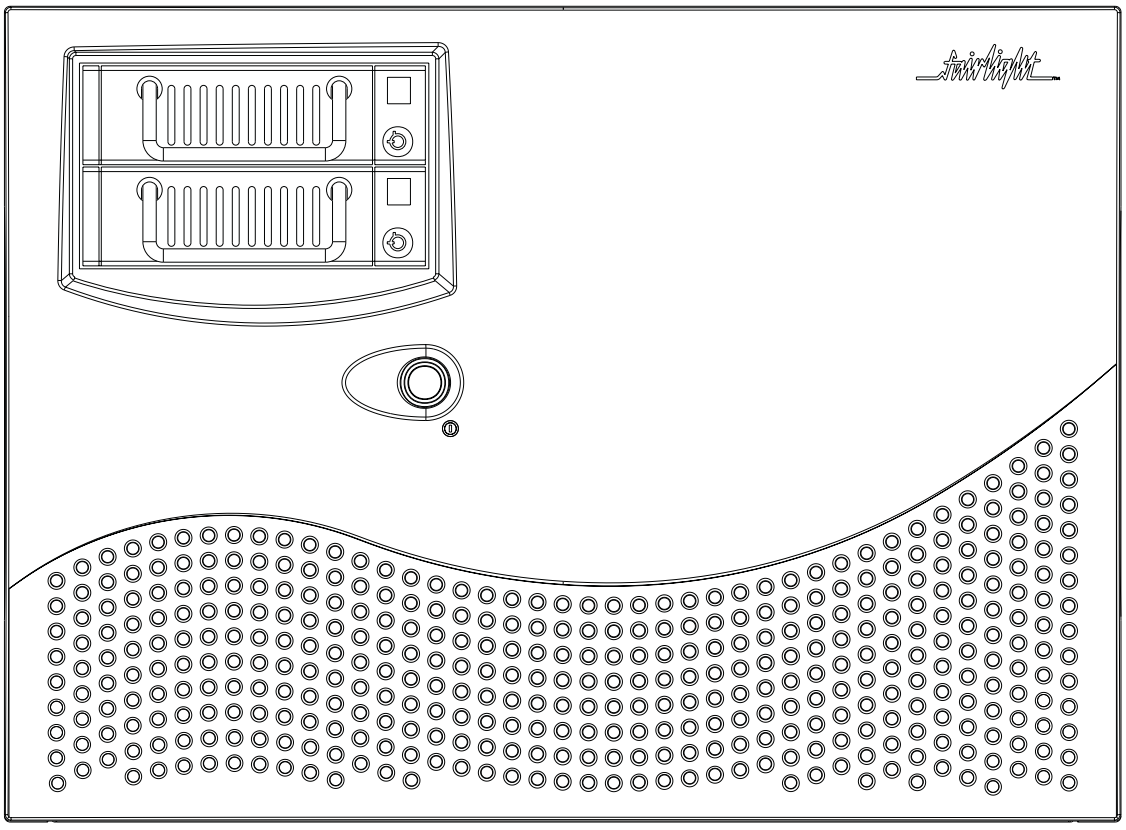
A20.1 Power Requirments

Input	85-275 Vac
	49-63 Hz 300VA
Fuse	10A - 110V
	6.3A - 240V

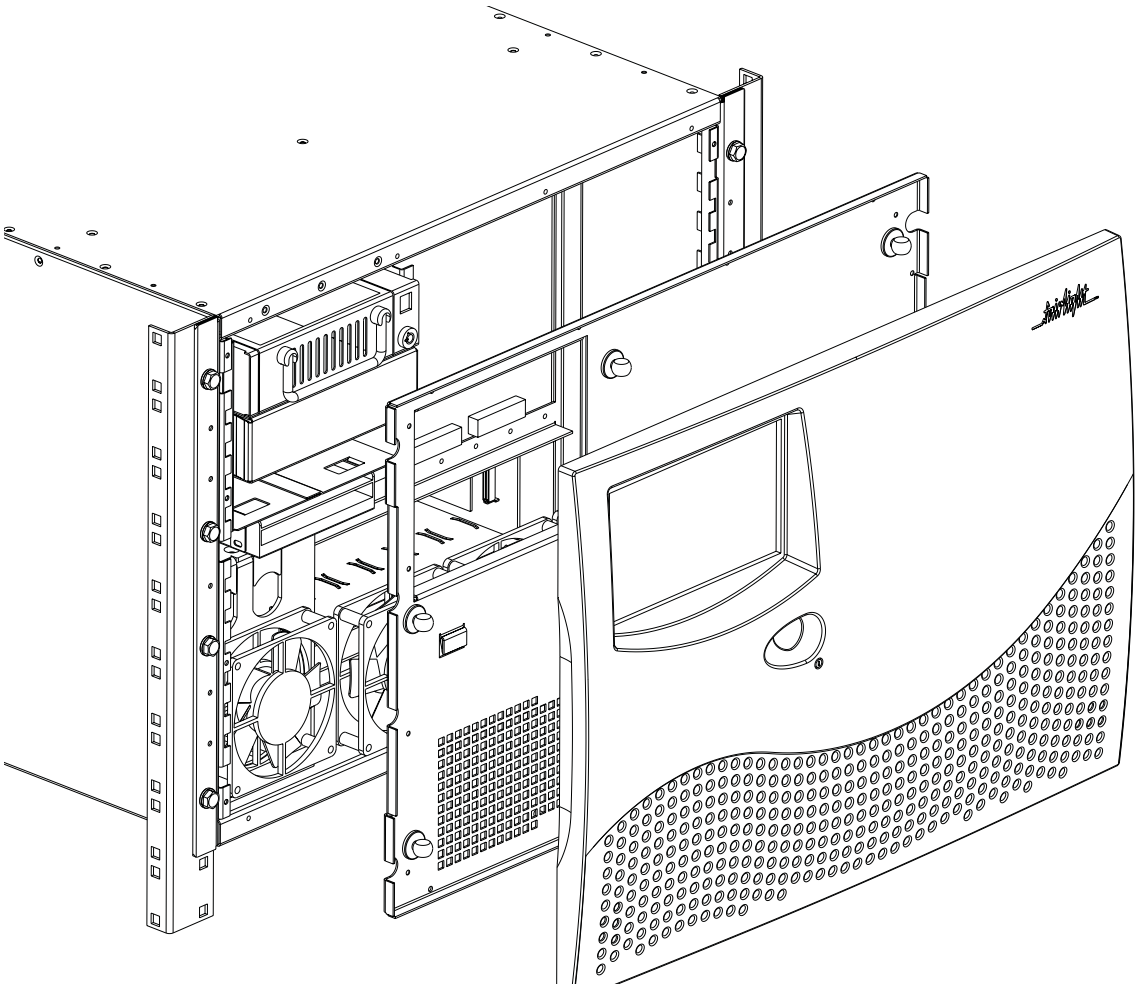
Chasis Diagrams

QDC Engine

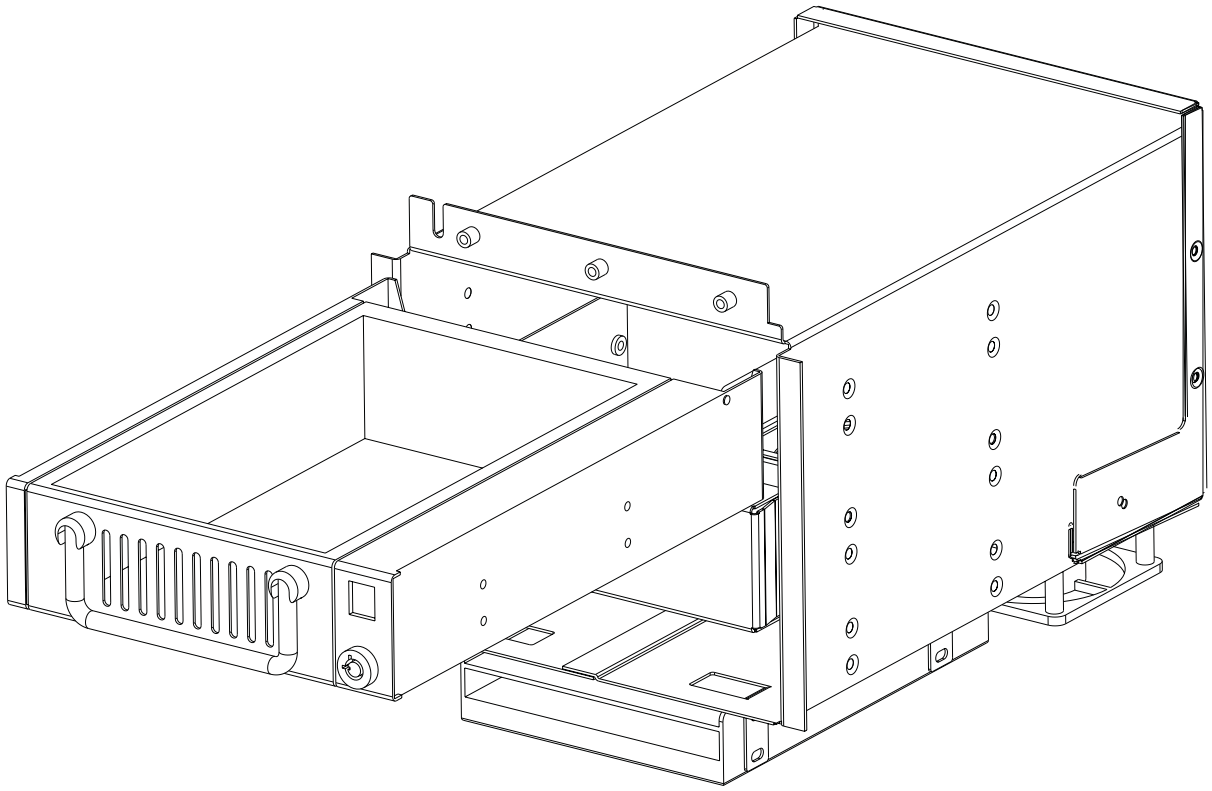
Engine Front



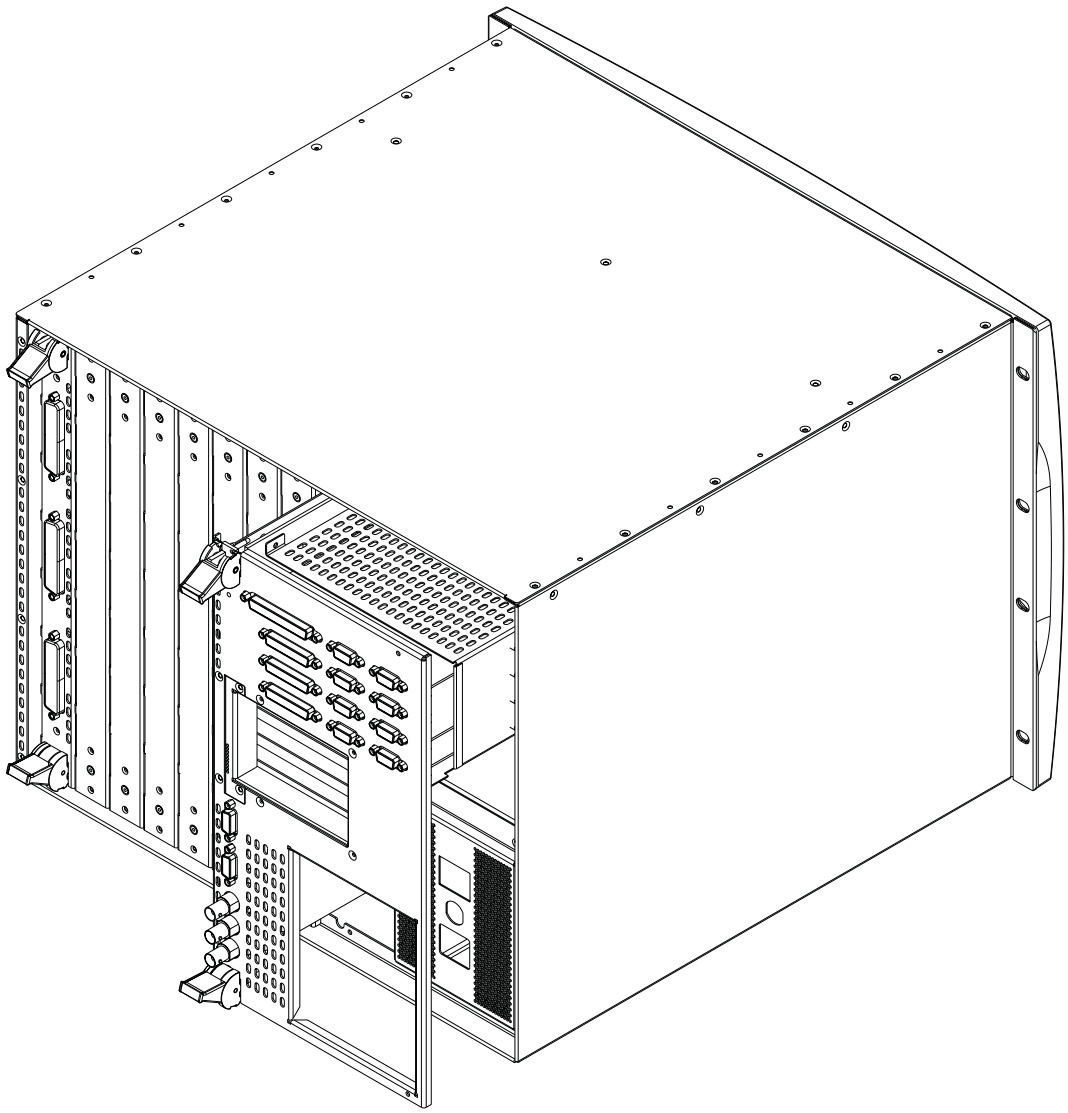
Engine Front Panels Removed



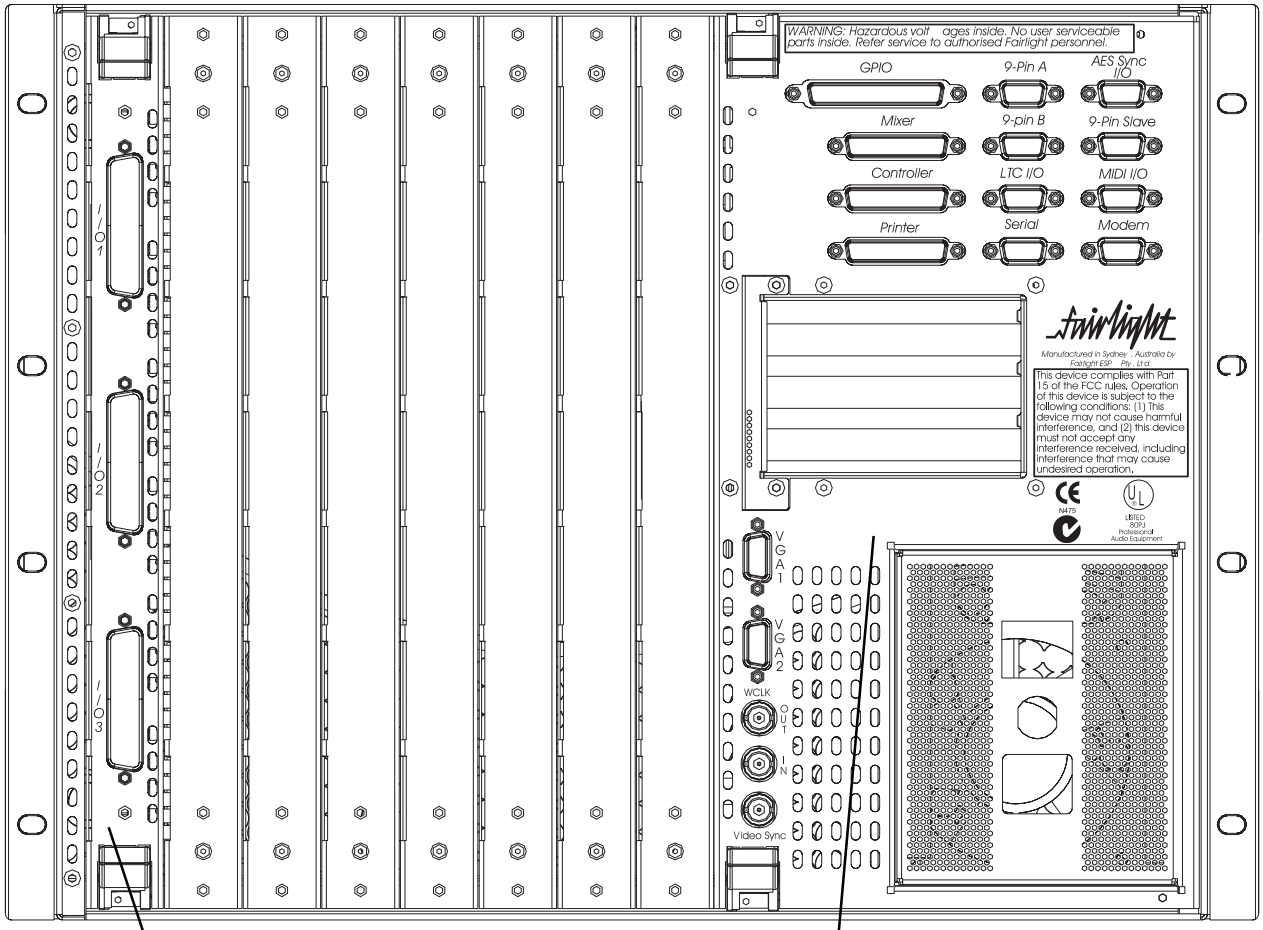
Drive Enclosure



Engine Back Panel / PXY Partly Removed



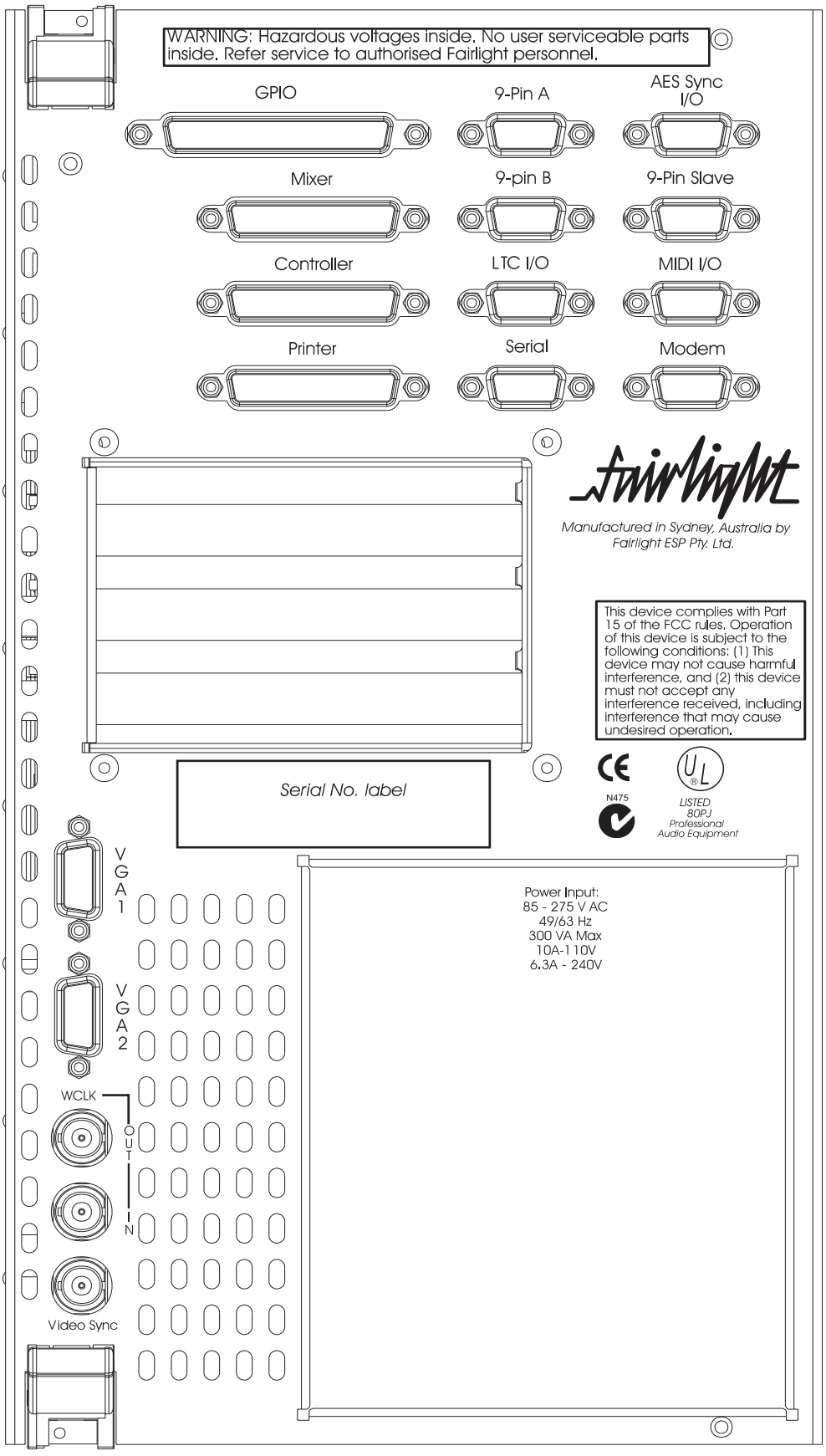
ENGINE BACK PANEL



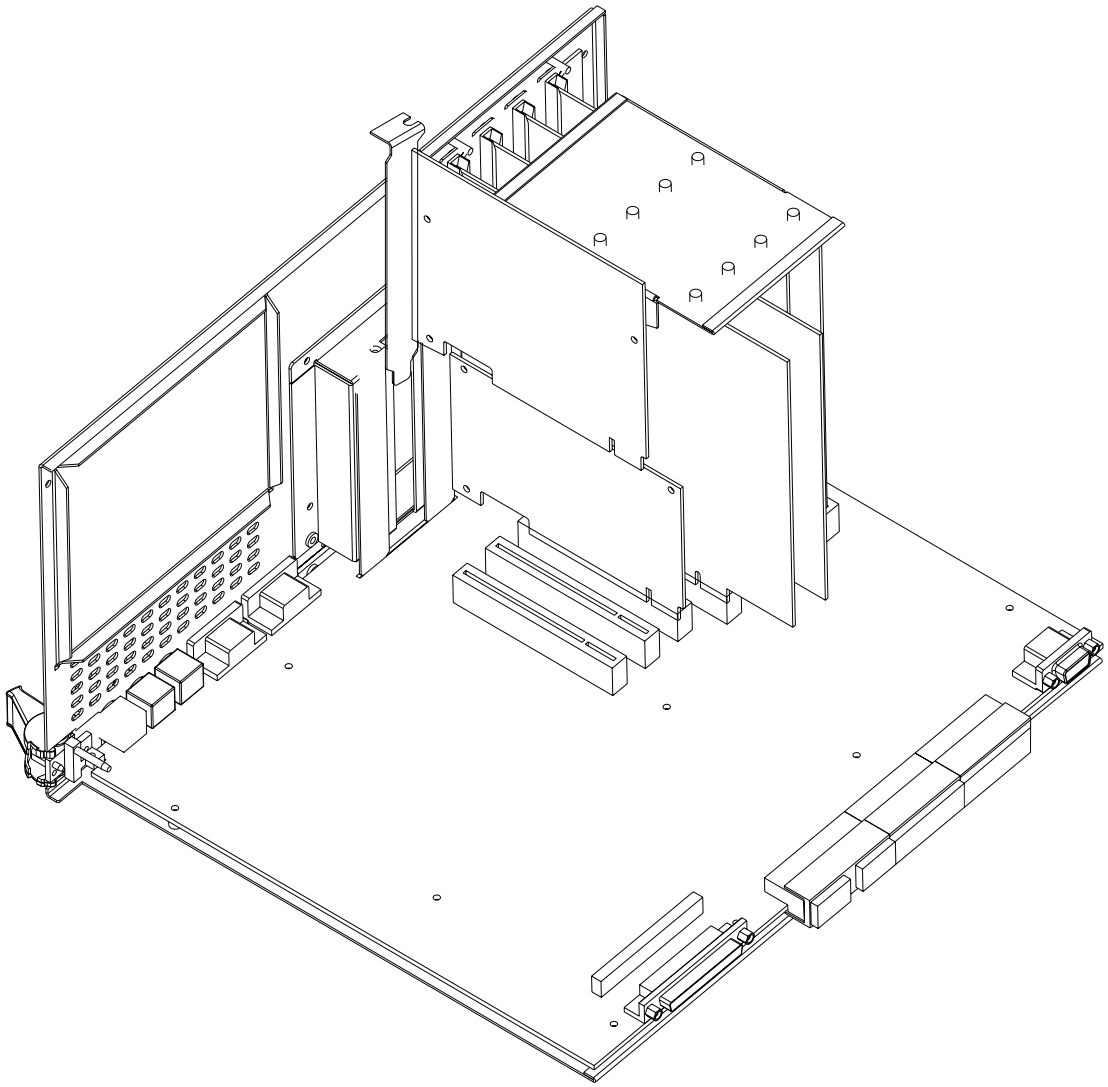
QDC Card

System I/O Panel

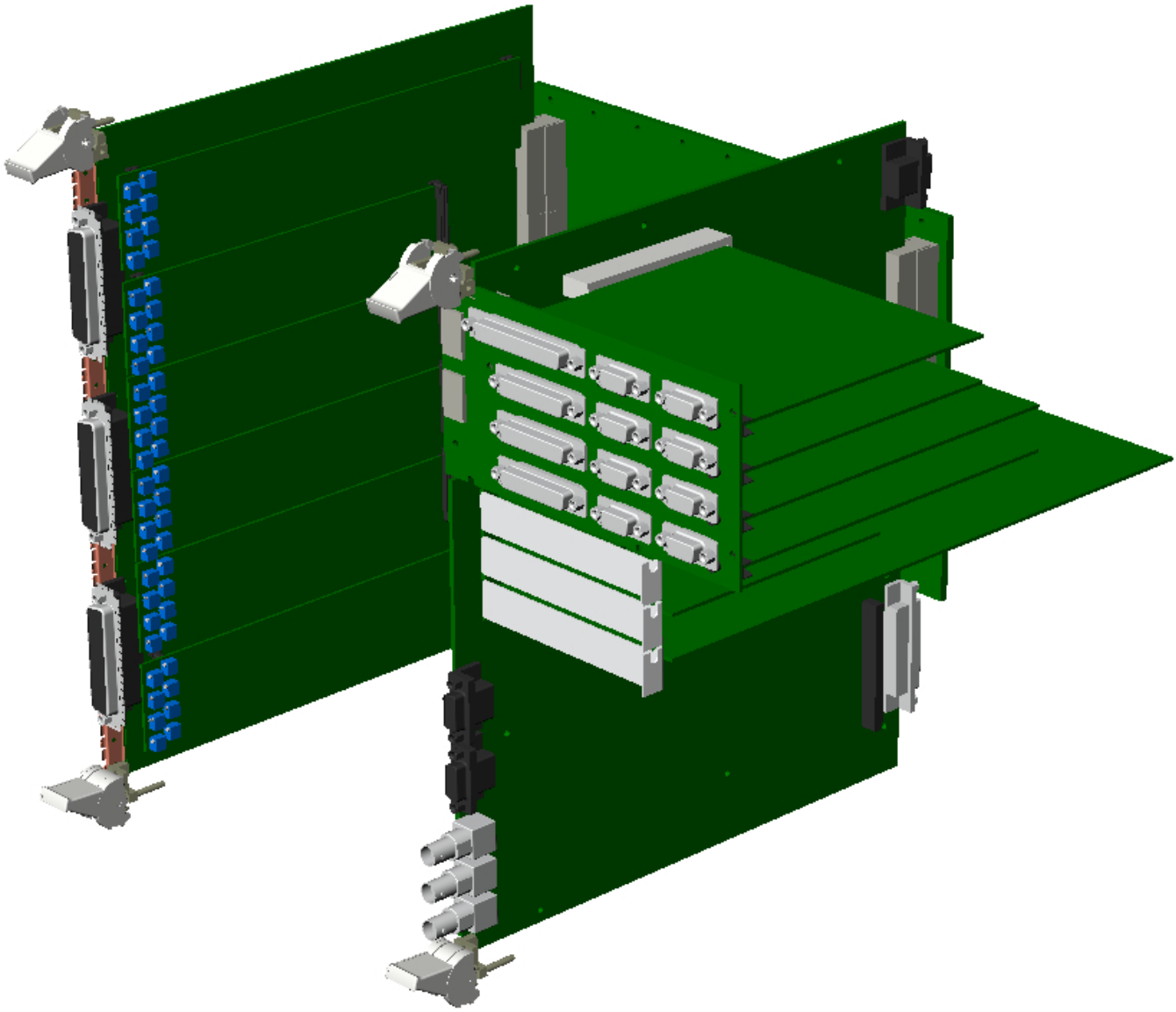
System I/O Panel



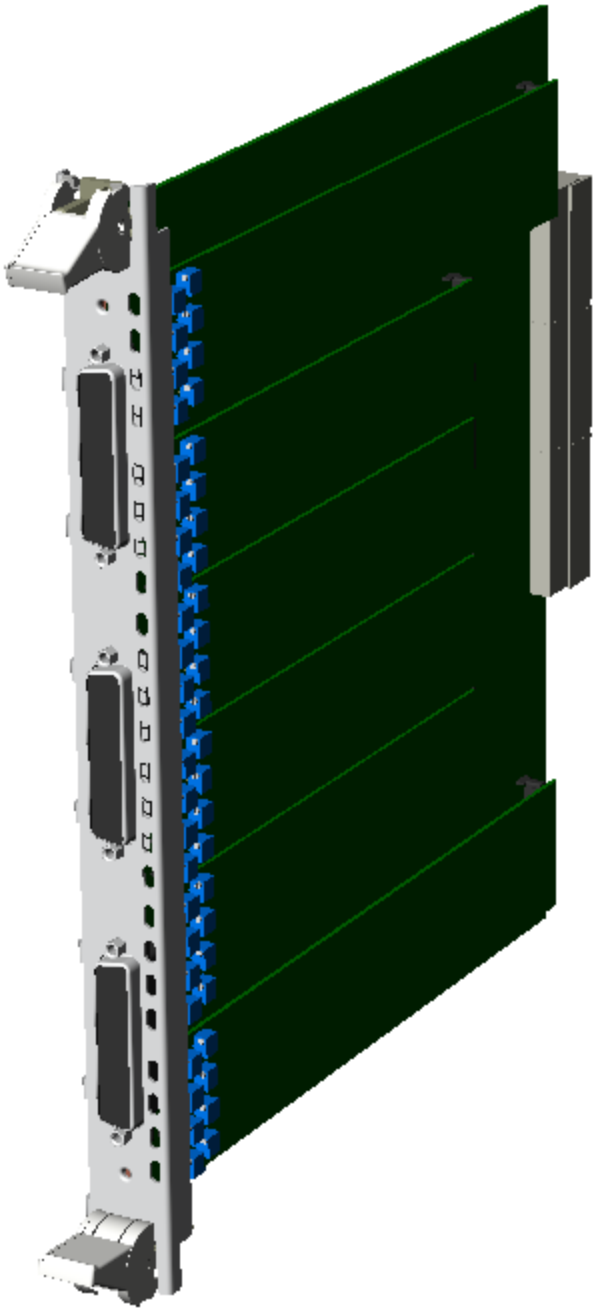
PXY Main Processor Board



QDC Card / PXY Main Processor Board / Backplane



QDC Card



QDC Engine Chassis

The Engine unit, takes up 8 RU, when fitted into a 19" rack. It operates from either 100-120v or 200-250v, 50-60Hz with the mains inputs being auto- switching, as such there are no switches to be set. At least two people are required to fit the Engine into a 19" rack as the unit is quite heavy. If available it is suggested that a third person be made available for the initial installation into the rack, such that a person can guide the Engine into the rack, from the rear.

The Engine should be fitted so that there is no restrictions to the ventilation, at the rear of the unit. If external SCSI devices are to be connected it is recommended that these be placed on a rack tray above or below the Engine.

It should be noted that typically the Engine unit is fitted with a boot drive with SCSI I.D. " 0 "(although the boot drive can be at any ID). The Engine uses fans for its forced ventilation system, these generate an amount of ambient noise. As stated before the Engine should be located in an air conditioned machine room away from the studio and other heat generating equipment.

Engine Rear Panel Connections

The Engine rear is split into two distinct sections; the System I/O Panel, located to the right and the Audio I/O section, located to the left.

The System I/O Panel contains all the synchronization needed to allow communication with external devices including RS-422, Midi, LTC, AES Sync, Serial and GPIO.

To allow communication with other Fairlight products including Fame and Prodigy, a Mixer port is provided.

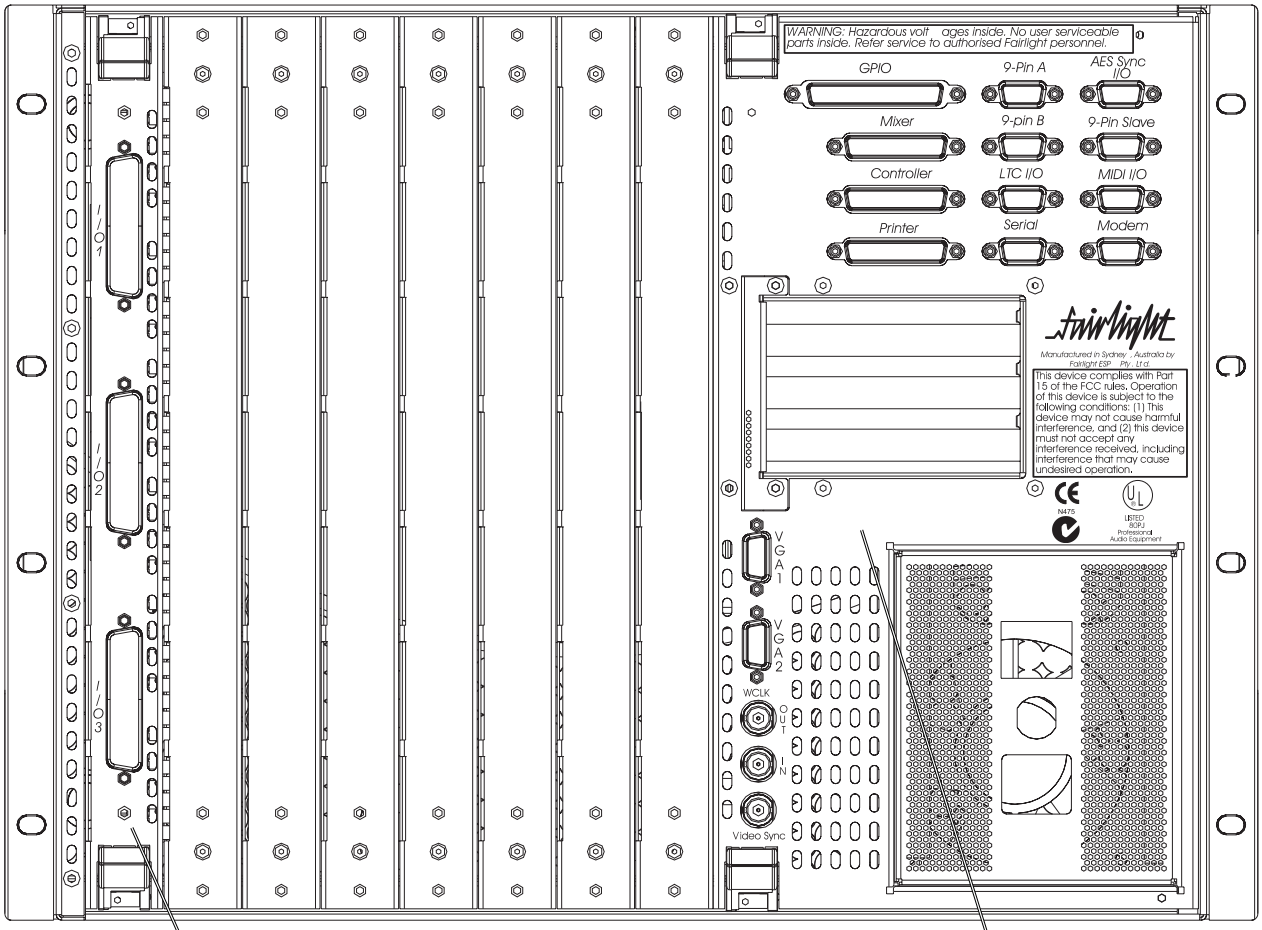
To allow comunication with the Merlin Console, a Controller port is provided.

The System I/O Panel also contains the VGA Output, Word Clock and Video sync In connectors.

The Audio I/O Section can contain up to a maximum of 4 QDC cards, which perform all analog ue and digital I/O Connections and Processing. Each QDC card can contain a maximum of 16 analogue inputs and 32 analogue outputs or a maximum of 32 digital inputs / outputs and 16 analogue inputs.

Depending on what configuration is ordered, the system can allow for more QDC cards to be configured. Please contact your local Fairlight office or distributor for further information regarding the maximum inputs and outputs which can be configured within the system.

Please refer to the Appendix page 36 for further details on the Audio I/O and System I/O Panels.


WARNING: Hazardous volt ages inside. No user serviceable parts inside. Refer service to authorised Fairlight personnel.
GPIO
9-Pin A
AES Sync I/O
Mixer
9-pin B
9-Pin Slave
Controller
LTC I/O
MIDI I/O
Printer
Serial
Modem
I/O 1
I/O 2
I/O 3
VGA1
VGA2
WCLK
OUT
IN
Video Sync
Manufactured in Sydney, Australia by Fairlight ESP Pty. Ltd.
This device compilies with Part 15 of the FCC rules. Operation of this device is subject to the following conditions: (1) This device may not cause harmful interference, and (2) this device must not accept any interference received, including interference that may cause undesired operation.
N475
LISTED 80PJ Professional Audio Equipment
QDC Card
Engine Back Panel
System I/O Panel

INTERNAL AND EXTERNAL SCSI DEVICES

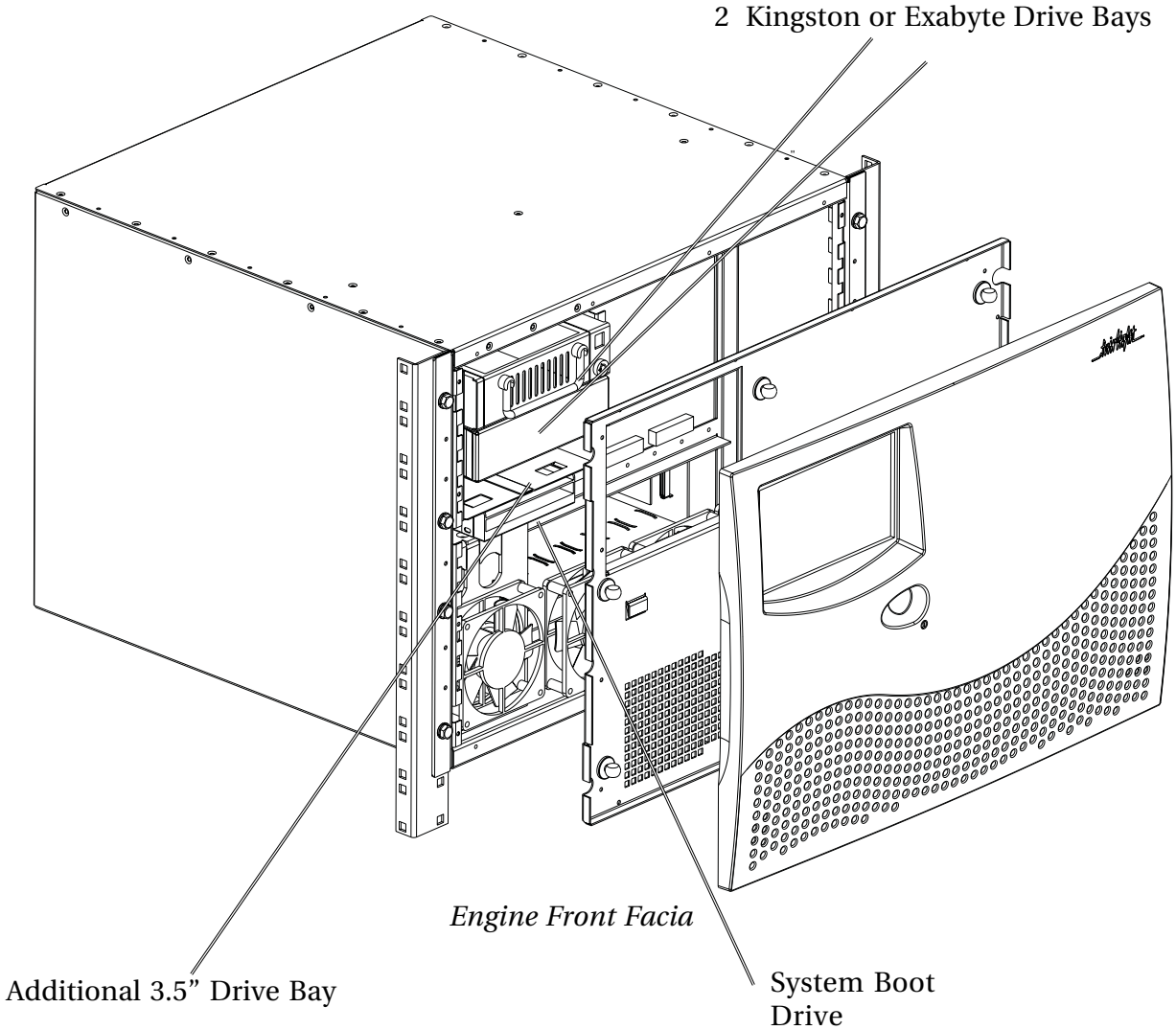
The Engine unit has been designed to accept two 3.5 Inch drives and 2 5.5” drive bays internally which can take either Kingston Technology drive enclosures or an Exabyte enclosure. The system typically comes configured with one system disk which contains the O/S9 Operating System and Merlin software. This allows for 3 media drives to be fitted internally in the system.

With a second SCSI Controller installed within the Engine an additional 4 SCSI devices can be attached externally.

Typically Exabyte drives should be set to ID “5” when connected on either SCSI Buss.

Optical based devices should be set to ID “3”. When connected on either SCSI bus.

It is recommended that a rack tray be fitted either above or below the Engine to hold external SCSI devices. The last device on the chain should be terminated with all other devices being looped through. The cables should be the shortest length possible to avoid SCSI bus corruption.



Engine Front Facia

9MW4PXY - Dual Processor Card

Functional Description

1. Introduction

The PXY card is a stand-alone dual 68040 processor card with 3 PCI slots and provision for all I/O except for the audio. There are on-card slots for the synchronisation I/O (SIO1, SIO2) and two graphics cards (CG5 - called CGA and CGB).

PXY is placed in mother board slot 1 which is right most when viewed from the rear of the system. The PXY can also be used stand-alone by connecting it to a standard ATX power supply.

By way of comparison to MFX3, PX is equivalent to the ESP-WX, and PY is equivalent to the ESP-SYN. ESP-SIO has now been replaced by SIO1 and SIO2. The ESP-PCI card is now incorporated as the PCI interface now accessable by both PX and PY.

The two processors are called PX and PY - hence the name PXY. PX is the operating system, user-interface and graphics processor. PY is the audio synchronisation processor.

All audio processing is provided by the QDCs connected to the backplace.

2. Features of PXY

CPU subsystem

. System clocking phase locked to single 14.318MHz crystal.

. Power on reset.

. Dual 68040 processors running at 40MHz (PX and PY).

. Fully vectored interrupts with software generated interrupts.

. Power supply status with intellegent power off switching.

. Dual interleaved 0WS 72 pin SIMMs per processor. Allows up to 256M per processor.

. 32M of uploadable FROM.

. 512k of socketed boot FROM.

. Real time clock with 128k of non-volatile RAM.

. 128k shared SRAM between PX,PY.

QDC communications

. TSB interface using CPCI signalling

PCI INTERFACE

. PCI interface (called P1) to 3 slots accessable by PX and PY.

. SCSI interface on P1 with WIDE and FAST interface.

. CPCI interface to QDC (called P2) which replaces the old WFM bus.

DEBUGGING

. Interface to quad graphic LED display.

. 2 x 8 way DIP switches.

. 4 tone speaker

. One bit control port for logic analysis synchronisation to

software.

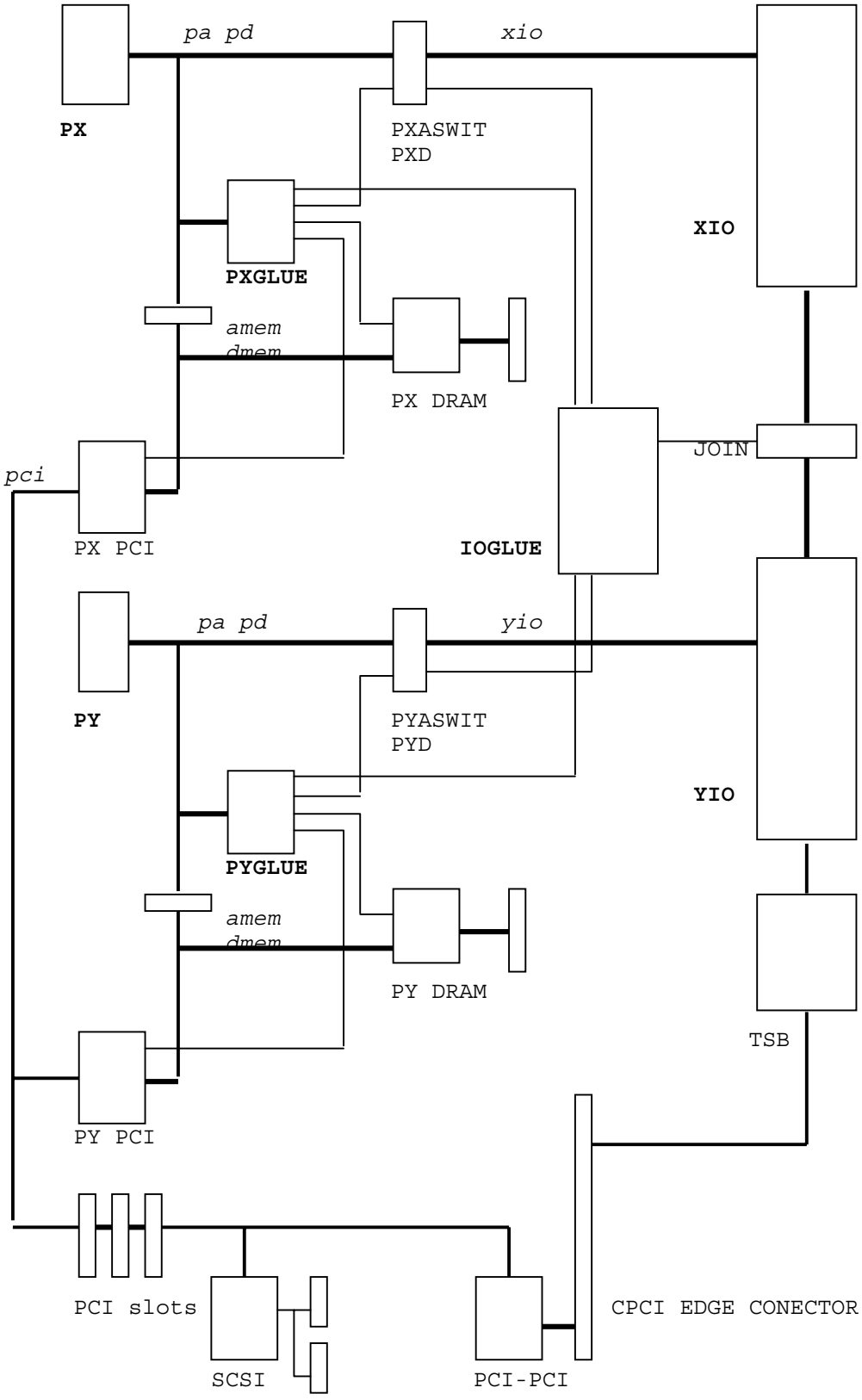
SERIAL PORTS

. Console RS232, download and RS422 on DB25F wired as standard RS232 cable with unused pins for the RS422 and download.

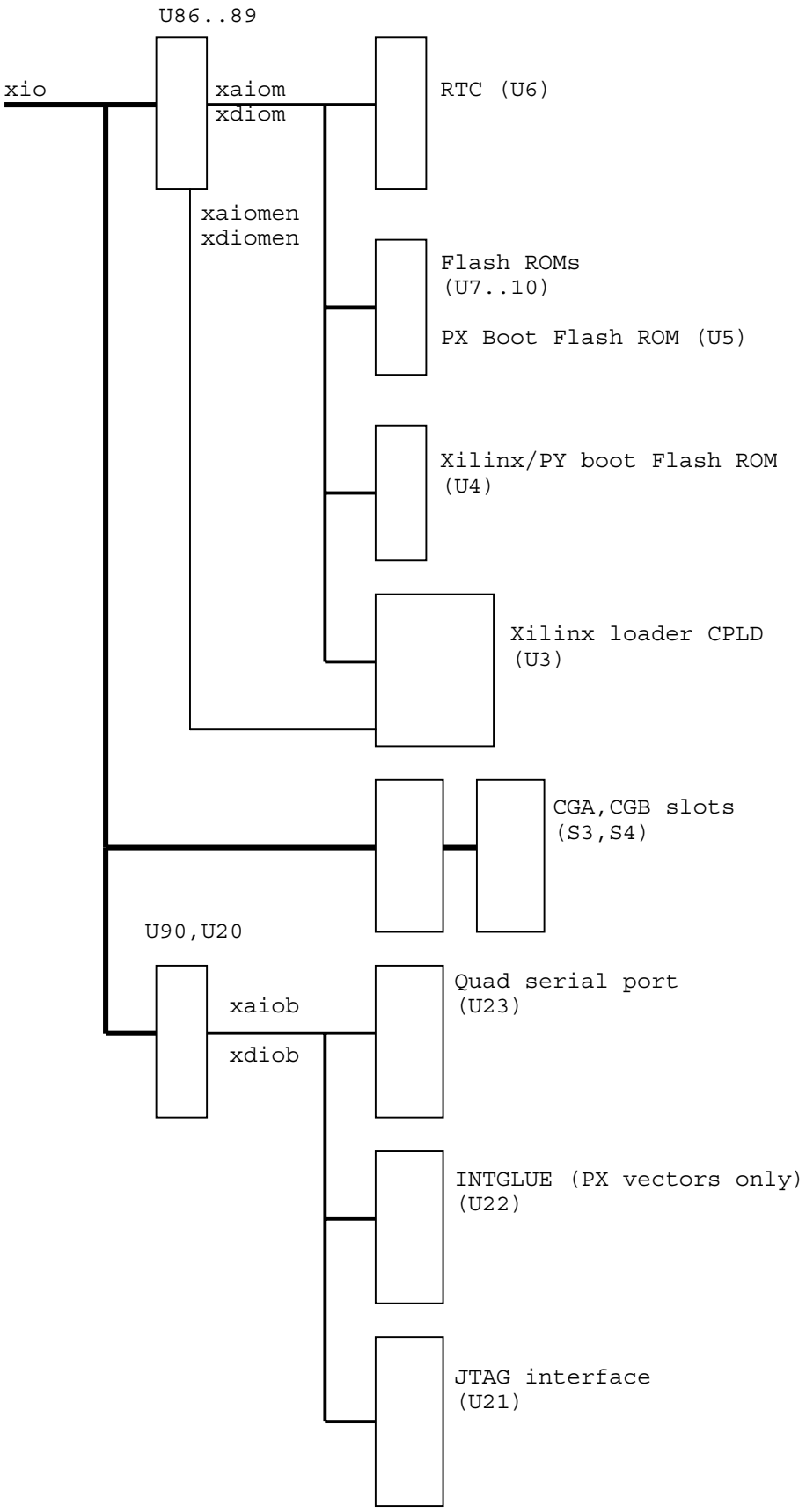
. Dongle interface

. 2 spare debugging serial ports

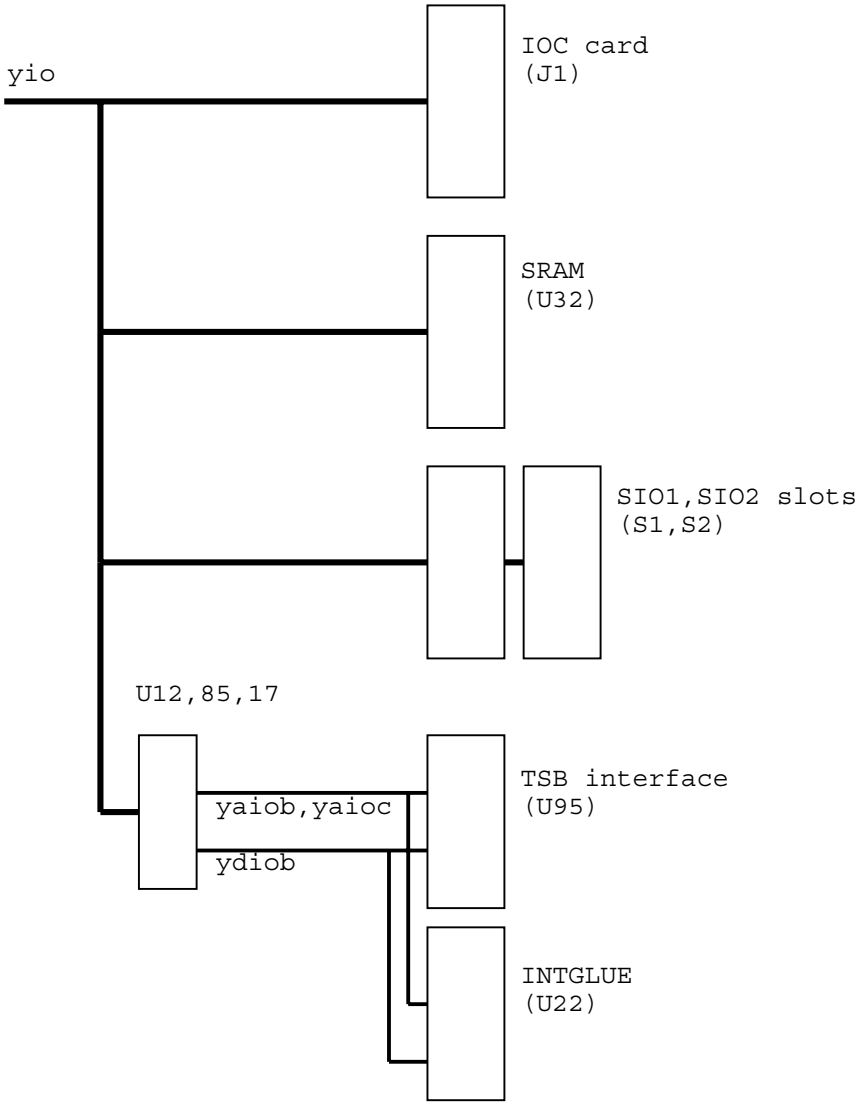
System Block Diagram



XIO Block Diagram



YIO Block Diagram



CLOCKS (CLOCKS.SCH)

CPU CLOCKS (CLOCKS/CPUCLOCK.SCH)

All clocks for PXY are phase locked to *14M318* from X1. This signal, is buffered by the low skew clock buffers in U29 (IDT49FCT805) to be distributed to the PLLs.

14M318_CPU is phase locked by U81 (AV9107S) to produce *CPUCLK* at 40MHz and *CPUCLKx2* at 80MHz. U78 and U48 (IDT49FCT805) buffer these signals to drive all the synchronous logic on the PXY.

4.1.2 PCI CLOCKS (CLOCKS/PCICLOCK.SCH)

Similar to the CPU clocks, *14M318* is phase locked by U31 (AV9107S) and buffered by U35 (49FCT805) to generate the clocks for the PCI bus. Selection of the PCI bus speed is via R37,R36.

R37	R36	PCI clock speed
installed	open	33MHz (default)
open	installed	66 MHz

PCI CLOCKS (CLOCKS/PCICLOCK.SCH)

4.2 PCI (PCI.SCH)

There are 2 PCI busses in the system. Local to PXY, third party PCI cards can be installed. This PCI bus is called P1. To commumicate to the QDCs, the backplane uses a compact PCI bus and is called P2. The PCI bus arbitration is part of IOGLUE (U38).

4.2.1 PCI SLOTS (PCI/PCISLOTS.SCH,

PCI/PCISLOTS/PCI_S1.SCH,
PCI/PCISLOTS/PCI_S2.SCH,
PCI/PCISLOTS/PCI_S3.SCH)

The P1 PCI slots (P6,P4,P3) are standard. On each slot the open collector slot presence bits (*PRSNT1,*PRSNT2) are wired together to detect whether the card is present (PRESENTn). If the card is not present, the TDI and TDO signals are joined to complete the JTAG test chain.

For configuration cycles (IDSEL asserted), the slot to be accessed is selected via address lines - A16 for slot 1, A17 for slot 2, A18 for slot 3, A19 for PX PCI interface (U103), A20 for PY PCI interface (U104), A21 for P1-P2 PCI-PCI bridge (U102), A22 for on-board PCI SCSI (U99).

4.2.2 SCSI INTERFACE (PCI/PCISLOTS/SCSI.SCH)

PXY has an onboard PCI SCSI WIDE and FAST interface provided by U99 (SYM53C875) on the P1 PCI bus. All signals are actively terminated via U30,U33,U34 (UC5613DP). The active termination can be enabled by shorting JP8 - in normal operation, this should be shorted.

Connection to the SCSI cable can be either 8 bit single-ended narrow SCSI connected to J9 (50 way), or 16 bit WIDE single-ended SCSI connector J10 (68 way high-density).

4.2.3 Motherboard PCI connection (PCI/PCI-PCI.SCH)

The P2 PCI bus is connected to the P1 PCI bus via the PCI to PCI bridge at U102 (DEC21152). This bridge also provides PLL rebuffered clocks to the PCI bus (P2CLK1,P2CLK2,P2CLK3,P2CLK4). P2CLK0 is a 10" track used to equalise the timing of the clocks across the QDC P2 slots by simulating the length of the traces on the back plane. This is fed back as the reference to the PLL to align all clocks.

4.3 PX/PY (PX.SCH, PY.SCH, PX/PX_CPU.SCH, PY/PY_CPU.SCH)

PX and PY sub-modules both include a CPLD for logic 'glue', a DRAM interface, a PCI interface and buffers to the I/O. The logic is identical up to the I/O. For this reason the CPU sub-modules are described below in parallel.

PX and PY are 68040s (U71,U70). The 68040 requires 2 clocks for operation. The internal clock PCLK (processor clock) is twice BCLK (bus clock) which is the bus clock speed.

4.3.1 PX,PY GLUE (PX/PXGLUE.SCH, PY/PYGLUE.SCH)

PXGLUE/PYGLUE CPLDs (U74,U72) control the CPU bus cycles and provides the top level system decoding.

PX and PY have different local DRAM addresses. This allows each processor to access the other processor's memory, and PCI to have access to all peripherals. Note that since the 68040 resets to address 00000000, the XIO I/O space contains the ROMs.

Global Map

Address	Decode
80000000-FFFFFFFF	PCI bus 2 (backplane)
60000000-7FFFFFFF	PCI bus 1 (local PCI)
50000000-5FFFFFFF	PY DRAM
40000000-4FFFFFFF	PX DRAM
30000000-3FFFFFFF	PX,PY EPC PCI controller
20000000-2FFFFFFF	YIO peripherals
1F0F0000-1F0FFFFF	BMC DRAM memory controller
00000000-0FFFFFFF	XIO peripherals

The IO on the system is accessable by both processors. However, as PX is normally used for operating system functions, and PY is used for synchronisation functions; the IO bus is split into XIO and YIO. The fastest and uninterrupted accesses occur when each processor acccess its own IO bus (PX to XIO and PY to YIO). If a processor needs to access a peripheral on the other processor's IO bus, *I*OGLUE will arbitrate for exclusive access to IO and join XIO to YIO.

4.3.2 IO bus isolation (PX/PXASWIT.SCH, PY/PYASWIT.SCH PX/PXD.SCH, PY/PYD.SCH)

When an access to XIO or YIO is granted, the processor bus is enabled via sets of buffers to the IO bus by *IOGLUE* (PX - U59..62,U122,U124,U127,U129 PY - U54..57,U123,U125,U128,U130).

4.3.3 PCI INTERFACE (PX/PXPCI.SCH, PY/PYPCI.SCH)

The CPU address and data is isolated from the PCI (and DRAM) interface by buffers at U64, U69, U75, U80, U114..117 for PX; and U63, U66, U73,U77, U118..121 for PY. As the DRAM and PCI busses (*AMEM,DMEM*) is localised by these buffers, the PCI can only access the DRAM.

The PCI controller is a V360EPC located at U103 for PX and U104 for PY. Arbitration for the local memory bus between the CPU and PCI controller and buffer control, is handled by the respective processor's *PXGLUE/PYGLUE* part.

The PCI bus is 32 bits 5V format.

Note that in the address map for the system, the local PCI devices are in a 256M window and the CPCI (to QDCs etc) is a 2G window.

4.3.4 DRAM INTERFACE (PX/PXDRAM.SCH,PX/PXDRAM/XODD_DIM.SCH,PX/PXDRAM/XEVENDIM.SCH,PY/PYDRAM.SCH,PY/PYDRAM/YODD_DIM.SCH,PY/PYDRAM/YEVENDIM.SCH,

The DRAM inteface is controlled by V292BMC at U67 for PX and U65 for PY. Each DRAM interface has dual DRAM SIMMs which are interleaved during accesses to achieve 0WS. The maximum installable memory is a 128M SIMM in each slot thus allowing up to 256M per processor.

As the *HMODE#* pin is unconnected (not shown on schematic), the startup address for the BMC registers is *1F0F0000*.

4.4 XIO/YIO BUS INTERFACE

4.4.1 JTAG INTERFACE (IO.SCH)

To program and test the PXY card, JTAG is used. This interface uses a 5 wire interface comprising of the following signals:

TDI	test data in
TDO	test data out
TMS	test mode select
TCK	test data clock
TRSTn	test interface reset

All devices capable of JTAG are connected in a chain using TDI and TDO. To allow debugging of faulty parts, the chain has jumpers at each device to allow bypassing that device in the chain.

Non-volatile CPLDs in the system are initially programmed via JTAG using the connector at JP7 (the Xilinx cable also needs Vcc,GND which are present on JP3 pins 1,2 respectively). Once the system is operational, the JTAG interface chip at U103 is used by the processors to read the JTAG chain.

The last JTAG device on every PCB (i.e. first device read) is a QS3J245 (U28 for PXY). This is simply a JTAG scannable device which has all pins binary encoded as PCB revision (pins 2,3,4,5 MSB on pin 5), modification level (pins 6,7,8,9 MSB on pin 9), and PCB identification

(pins 22,21,20,19 MSB on pin 19). The PCB identification numbers are allocated as follows

PCB ID	Card
0	PXY dual processor card
1	CG5 colour graphics/HSSL
2	QDC quad digital channel card
3	SIO1 sync I/O 1
4	SIO2 sync I/O 2
5	unused
6	AI analog in card
7	AO analog out card
8	AES digital I/O card
9..F	unused

The PCB revision is 'hard-wired' on the PCB to reflect the PCB revision number. The PCB modification level is set according to the ECNs in the field. It is essential that all of these pins are set to the correct revison levels as the software uses this information.

As the JTAG chain must be distributed to all cards, the signals are buffered by U43 (low skew buffer).

4.4.2 Joining of XIO and YIO (IO/IOSWITCH.SCH)

When a processor wants to access the other processor's IO bus, the JOINIOn signal is asserted (after it gains exclusive access to the IO bus) which connects the busses using the quickswitches at U13..16.

4.4.3 IOGLUE (IO/IOGLUE.SCH)

The XIO and YIO busses can be joined or accessed independently by their respective processors, IOGLUE manages all the buffer enabling and arbitration to the IO busses. IOGLUE is passed a chip select as a request to access the IO bus from PXGLUE and PYGLUE (XTOXIOn, XTOYIOn, YTOXIOn, YTOYIOn). Additionally, the XVECCSn, YVECCSn may be asserted by PXGLUE,PYGLUE when the accesses is to get the vector number for vectored interrupts.

IOGLUE further sub decodes the addresses for the IO chip selects.

XIO decoding A31..A28 = 00002

A27..A19	Address	Decode
1111	0F000000-0FFFFFFF	Address trapper
1110		
1101		
1100		
1011	0B000000-0BFFFFFF	TAP interface
1010	0A000000-0AFFFFFF	HSSL
1001	09000000-09FFFFFF	CG B
1000	08000000-08FFFFFF	CG A
0111		
0110		
0101		
0100	04000000-04FFFFFF	32M flash ROM
0011		
0010		

0001		
01.. .	01400000-17FFFFFF	Real Time Clock
0011 .	01300000-013FFFFF	Quad serial port 3
0010 .	01200000-012FFFFF	Quad serial port 2
0001 .	01100000-011FFFFF	Quad serial port 1
0000 .	01000000-010FFFFF	Quad serial port 0
0000		
0000 1	00080000-000FFFFF	Xilinx download flash ROM
0000 0	00000000-0007FFFF	Boot flash ROM

YIO decoding **A31..A28 = 00102**

A27..A19	**Address**	**Decode**
1111	2F000000-2FFFFFFF	Address Trapper
1110		
1101	2D000000-2DFFFFFF	SIO 2
1100	2C000000-2CFFFFFF	SIO 1
1011		
1010		
1001		
1000		
0111		
0110		
0101		
0100		
0011		
0010		
110. .	22C00000-22DFFFFF	GPIO bank
101. .	22A00000-22BFFFFF	GPIO output
100. .	22800000-229FFFFF	GPIO input
011. .	22600000-227FFFFF	Super IO (printer/serial)
010. .	22400000-225FFFFF	INTGLUE interrupt controller
001. .	22200000-223FFFFF	TSB interface
000. .	22000000-221FFFFF	Shared SRAM (128k)
0001		
0000		

IOGLUE also provides all the XIO and YIO control signals, IO wait-state generation and PCI bus arbitration.

4.4.4 INTGLUE INTERRUPT CONTROLLER (IO/INT.SCH)

All interrupt sources are connected to INTGLUE. This FPGA prioritises the interrupts and provides the vector number when the interrupt is acknowledged by the CPU. All vector numbers are hard-wired in the FPGA, however, IOGLUE can be changed as it is loaded from flash ROM at every power-on reset.

INTGLUE also provides all of the debugging features. For further information on the debug control consult the INTGLUE - interrupt glue FPGA (INTGLUE.DOC) documentation.

The power-on reset is fed into INTGLUE to produce the CPU and IO resets. Initially a CPLD loads the contents of INTGLUE from flash ROM. Once this programming is complete INTGLUE starts and hence deasserts the reset lines and ... off we go. If the FPGAs have loaded

correctly, all of the LEDs D3..10 should light.

As the PXY design in quite symmetric, a jumper at JP5 (NOTMEn) allows swapping the functions of the processors for debugging purposes. A status bit in INTGLUE allows the processors to know which one they are operating as, and who they are really.

4.5 XIO BUS

The XIO bus has IO primarily for the PX processor and hence includes IO primarily for the operating system and the GUI.

4.5.1 XIO SLOTS (IO/XIO/XIOSLOTS.SCH)

XIO provides two slots for the CG5 colour graphics cards at S3 and S4. For a single graphics card system, S3 (CGA) is used. Refer to the CG5 documenation for more information.

4.5.2 XIO MEMORY AND FPGA LOADING (IO/XIO/XIOMEM.SCH)

Upon power-on and reset switch assertion, the FPGALD CPLD at U3 has direct access to the FROM at U4 (assuming JP4 has pins 11,12 shorted) which holds the data for the FPGAs. A state machine in FGPALD reads the data from the FROM and loads the devices serially via XPROGn,XDONE,XBITS,XINITn,CCLK. It is possible to load the data from different flash ROMS by shifting the jumper at JP4.

When power-on reset is deasserted, FPGALD reads successive addresses starting form the last address in the ROM and counts down. The data read from each location is serialised to be sent to the FPGAs via XBITS and CCLK. When the XDONE signal is asserted, the FPGAs are loaded and FPGALD stops loading. Note that all jumpers should be installed at JP1 to wire-or the XDONE signals from the FPGAs.

Once the CPUs are released from reset (automatically by INTGLUE once loaded), they will attempt to access memory at 00000000. This is the address where U5 is located. By reading the status bit in INTGLUE to determine which processor they are operating as, they jump into the rest of the boot code has held in U5 (for PX) or U4 (for PY).

U6 is a DS1486 use for retaining the current time and configuration data. This chip is a real time clock with 128k of (internally) battery backed up RAM.

4.5.3 XIO BUFFERS (IO/XIO/XIOBUF.SCH)

The load of the many memories on the XIO bus requires the buffers on this sheet to provide adequate drive. All buffer controls are from IOGLUE.

4.5.4 SYSTEM SERIAL IO (IO/XIO/XIOCOMMS.SCH)

U23 is a quad serial port based on the 16450 uart. Ports 1 and 2 provide the RS232 and RS422 as required by the MFX console. Port 3 is for the dongle. The fourth port is used for console download and is also available at J10.

4.6 YIO BUS

YIO has the IO primarily for the PY processor and hence is mainly synchronisation hardware.

4.6.1 SHARED SRAM (IO/YIO.SCH)

A 128k byte SRAM at U32 is uses to provide inter-PX/PY software communications.

4.6.2 SIO SLOTS (IO/YIO/YIOSLOTS.SCH)

SIO1 is placed into the slot at S1 to provide the essential clocking and synchronisation features of the disk recorder. SIO2 is placed in the slot at S2 and provides the optional synchronisation features.

4.6.3 AUDIO CLOCKS (IO/YIO/YIOSLOTS/ACLOCKS.SCH)

The audio clocks derived from SIO1 are buffered by U19,U24 to the CPCI connector at J2 for distribution to the QDCs. When digital input sync is selected, one of the QDC clocks its DCLK and DCLKF signal; all other QDCs hold their clocks high. All channel's DCLKs and DCLKFs are NANDed (inverted ORed) together by U91,U25.

4.6.4 CON BOARD CONNECTOR (IO/YIO/IOCON.SCH)

The CON board holds most of the IO connectors for the system. CON connects to J1.

4.6.5 TSB INTERFACE (IO/YIO/TSB.SCH,IO/YIO/TSBCLOCK.SCH)

The TSB interface for digital audio exchange between the QDCs and PY is controlled by U95 (TSB) and connected via J4. The clocking is synchronised to the 14.31818MHz crystal by U11 and buffered by U97.

For information on the TSB specification refer to the Digital Audio Timesliced Bus (TSB) Design Specification document.
5.Summary of jumper settings

Summery Of Jumper Settings

R37	R36	PCI clock speed
installed	open	33MHz DEFAULT
open	installed	66 MHz

R7	R6	TSB clock speed
installed	open	33MHz DEFAULT
open	installed	66 MHz

JP9	
1-2	include IO JTAG DEFAULT
3-4	bypass IO JTAG

JP10	
1-2	include ID JTAG DEFAULT
3-4	bypass ID JTAG

JP5	NOTMEn
open	normal operation DEFAULT
short	swap PX/PY

JP6	
1	logic analyser strobe
2	GND

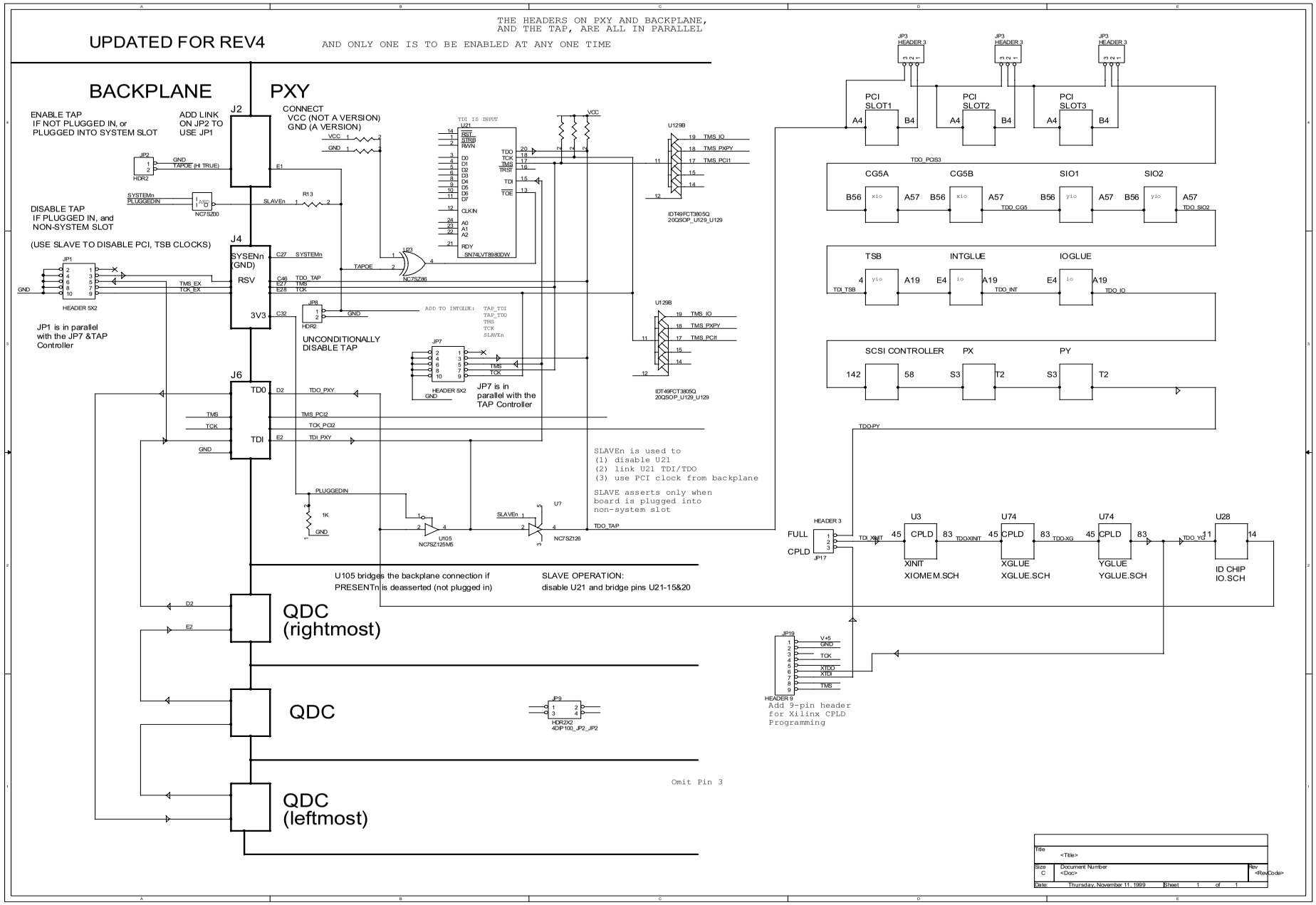
JP11	PX non-maskable interrupt
1	PX NMIn
2	GND

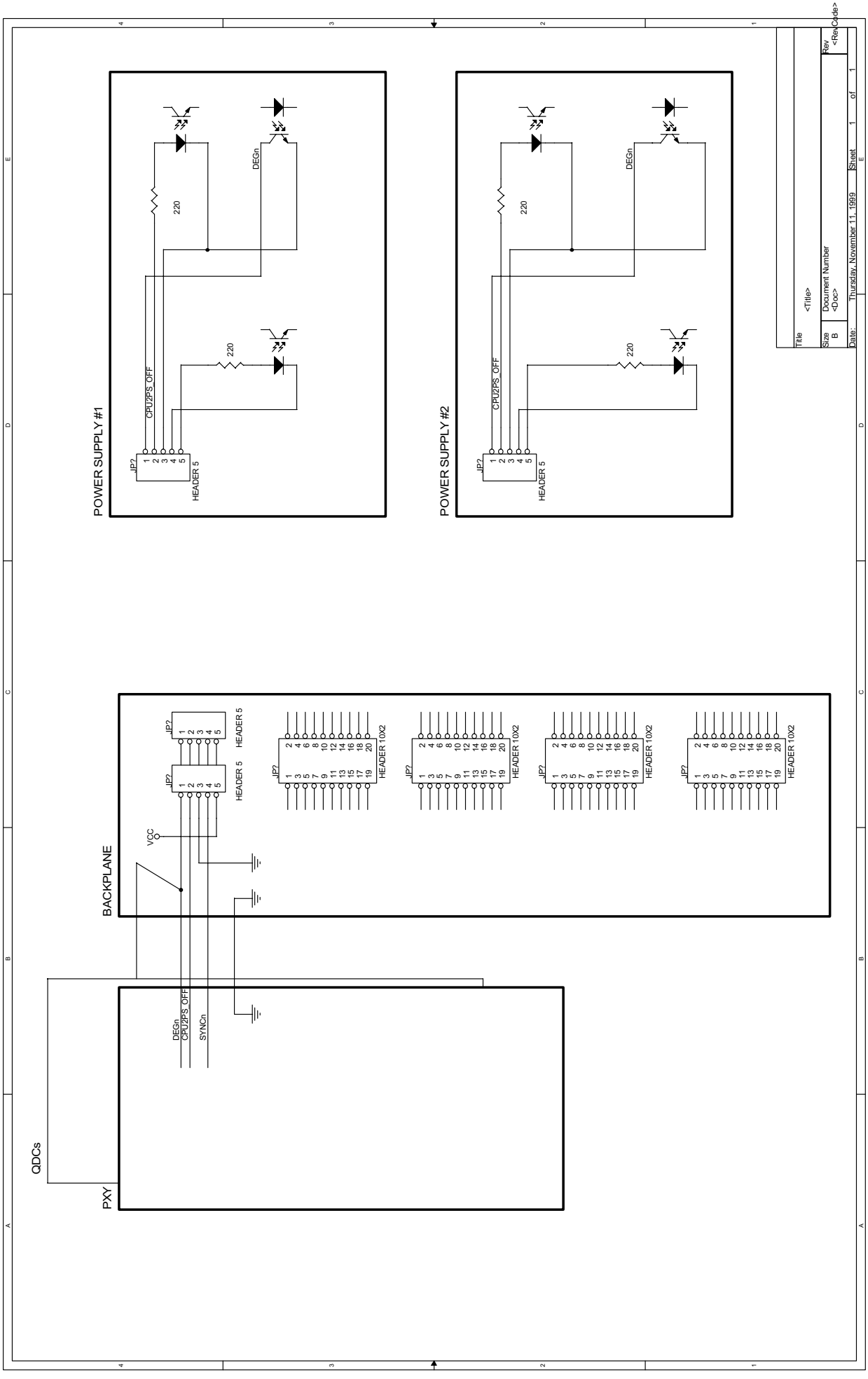
JP12	PY non-maskable interrupt
1	PY NMIn
2	GND

JP2	
open	Enable backup FROM
short	normal operation DEFAULT

JP8	
open	no SCSI termintion
short	SCSI terminated DEFAULT

JP4	FPGA load source
1-2	U9
3-4	U7
5-6	U8
7-8	U10
9-10	U5
11-12	U4 DEFAULT


THE HEADERS ON PXY AND BACKPLANE,
AND THE TAP, ARE ALL IN PARALLEL
UPDATED FOR REV4
AND ONLY ONE IS TO BE ENABLED AT ANY ONE TIME
BACKPLANE
PXY
ENABLE TAP
IF NOT PLUGGED IN, or
PLUGGED INTO SYSTEM SLOT
ADD LINK
ON JP2 TO
USE JP1
DISABLE TAP
IF PLUGGED IN, and
NON-SYSTEM SLOT
(USE SLAVE TO DISABLE PCI, TSB CLOCKS)
CONNECT
VCC (NOT A VERSION)
GND (A VERSION)
JP1 is in parallel
with the JP7 &TAP
Controller
UNCONDITIONALLY
DISABLE TAP
JP7 is in
parallel with the
TAP Controller
SLAVEn is used to
(1) disable U21
(2) link U21 TDI/TDO
(3) use PCI clock from backplane
SLAVE asserts only when
board is plugged into
non-system slot
U105 bridges the backplane connection if
PRESENTn is deasserted (not plugged in)
SLAVE OPERATION:
disable U21 and bridge pins U21-15&20
QDC
(rightmost)
QDC
QDC
(leftmost)
Omit Pin 3
PCI
SLOT1
PCI
SLOT2
PCI
SLOT3
CG5A
CG5B
SIO1
SIO2
TSB
INTGLUE
IOGLUE
SCSI CONTROLLER
PX
PY
CPLD
XINIT
XIOMEM.SCH
XGLUE
XGLUE.SCH
YGLUE
YGLUE.SCH
ID CHIP
IO.SCH
Add 9-pin header
for Xilinx CPLD
Programming
Title
<Title>
Size
C
Document Number
<Doc>
Rev
<RevCode>
Date:
Thursday, November 11, 1999
Sheet
1
of
1


POWER SUPPLY #1
POWER SUPPLY #2
220
DEGn
CPU2PS_OFF
JP2
HEADER 5
BACKPLANE
VCC
HEADER 10X2
PXY
QDCs
SYNCn
Title
<Title>
Size
B
Document Number
<Doc>
Rev
<RevCode>
Date:
Thursday, November 11, 1999
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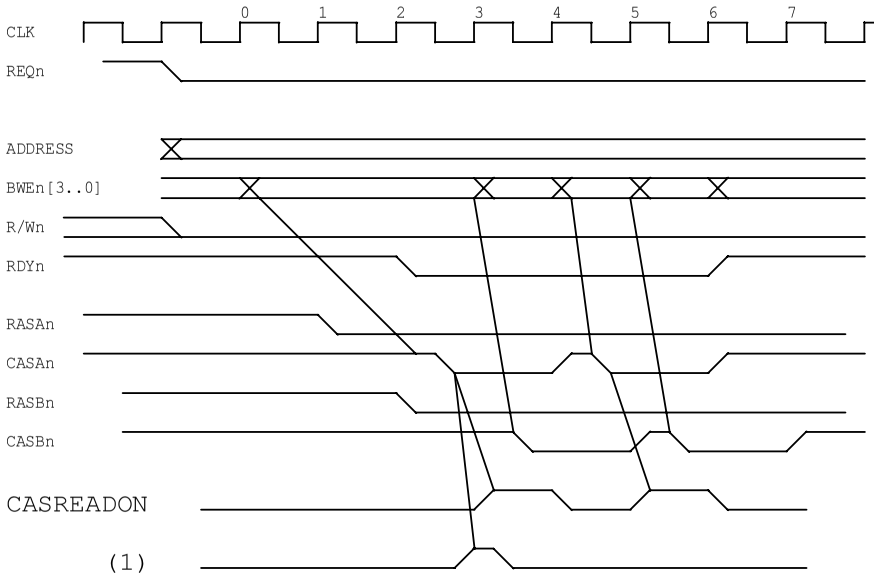
1
of
1

SETn

REQUIRED BY BMC

Figure8 (page14) BMC USer Manual



tCOV(clock to output) < 10 (BWE from EPC)

tCHL (falling clock to CAS) < 12.5ns

CAS_SET and CAS_CLR drive a SR
latch to generate CAS

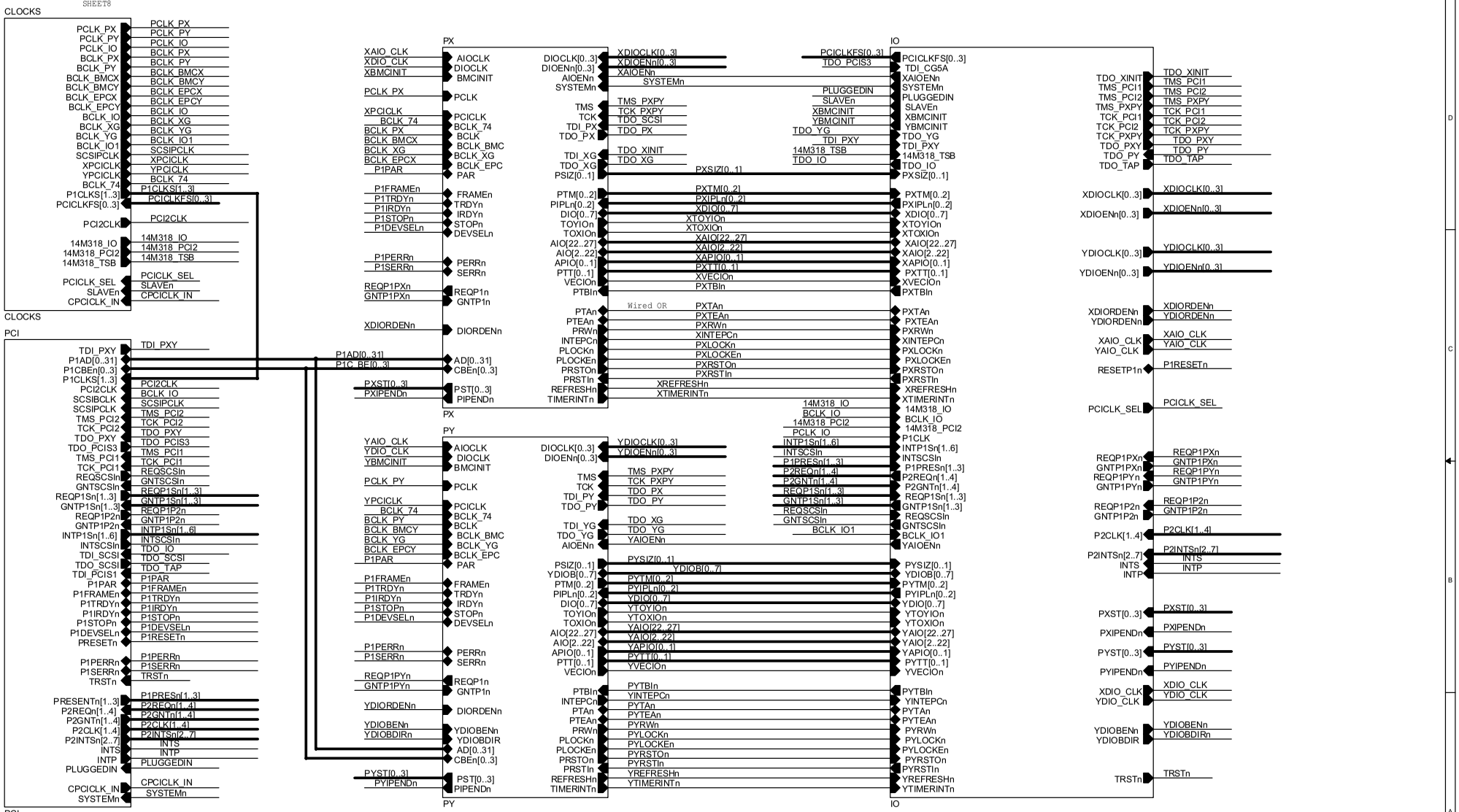
CAS_SET = BWE * CAS(bmc)_START

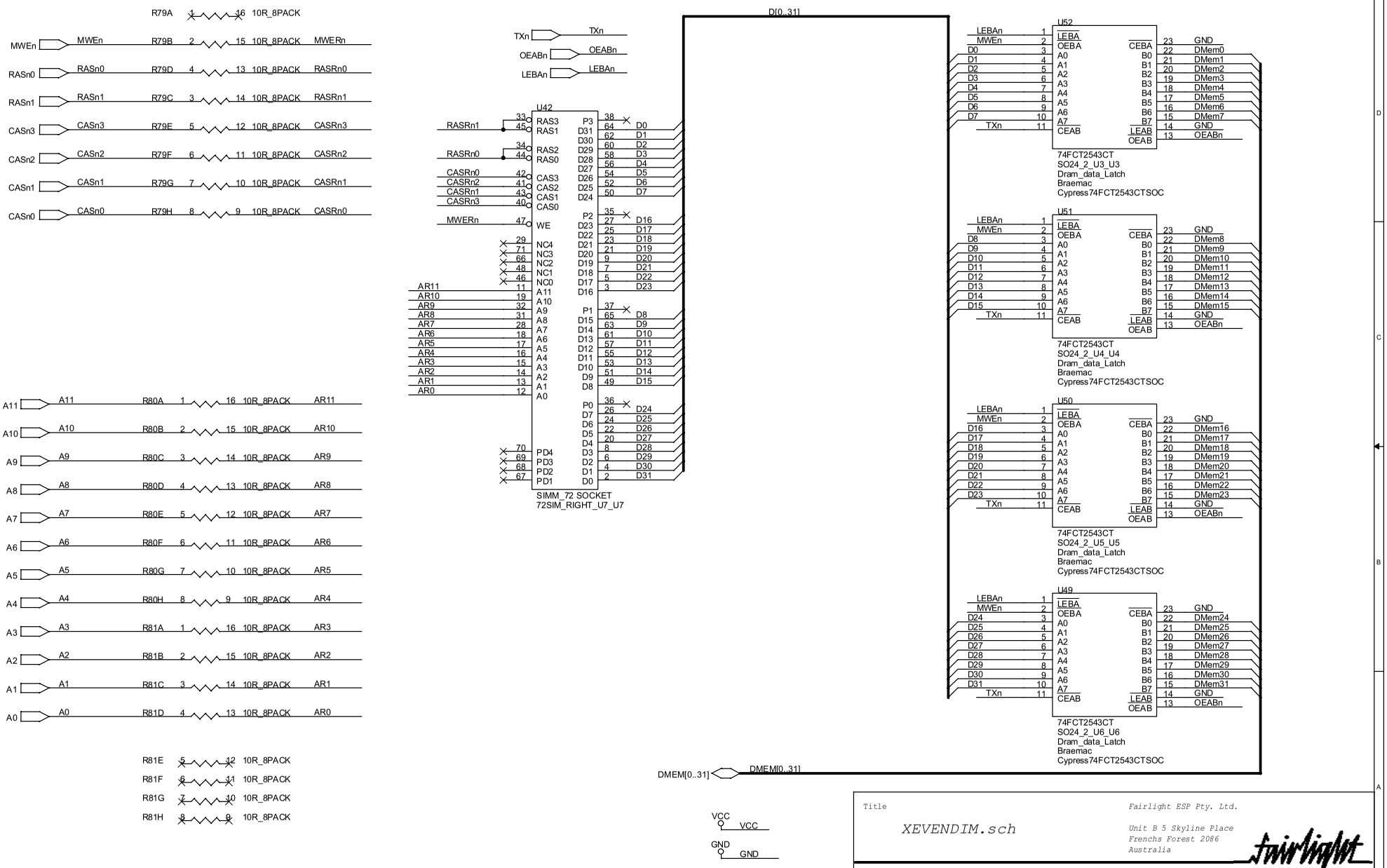
CAS_CLR = CAS(bmc)_END

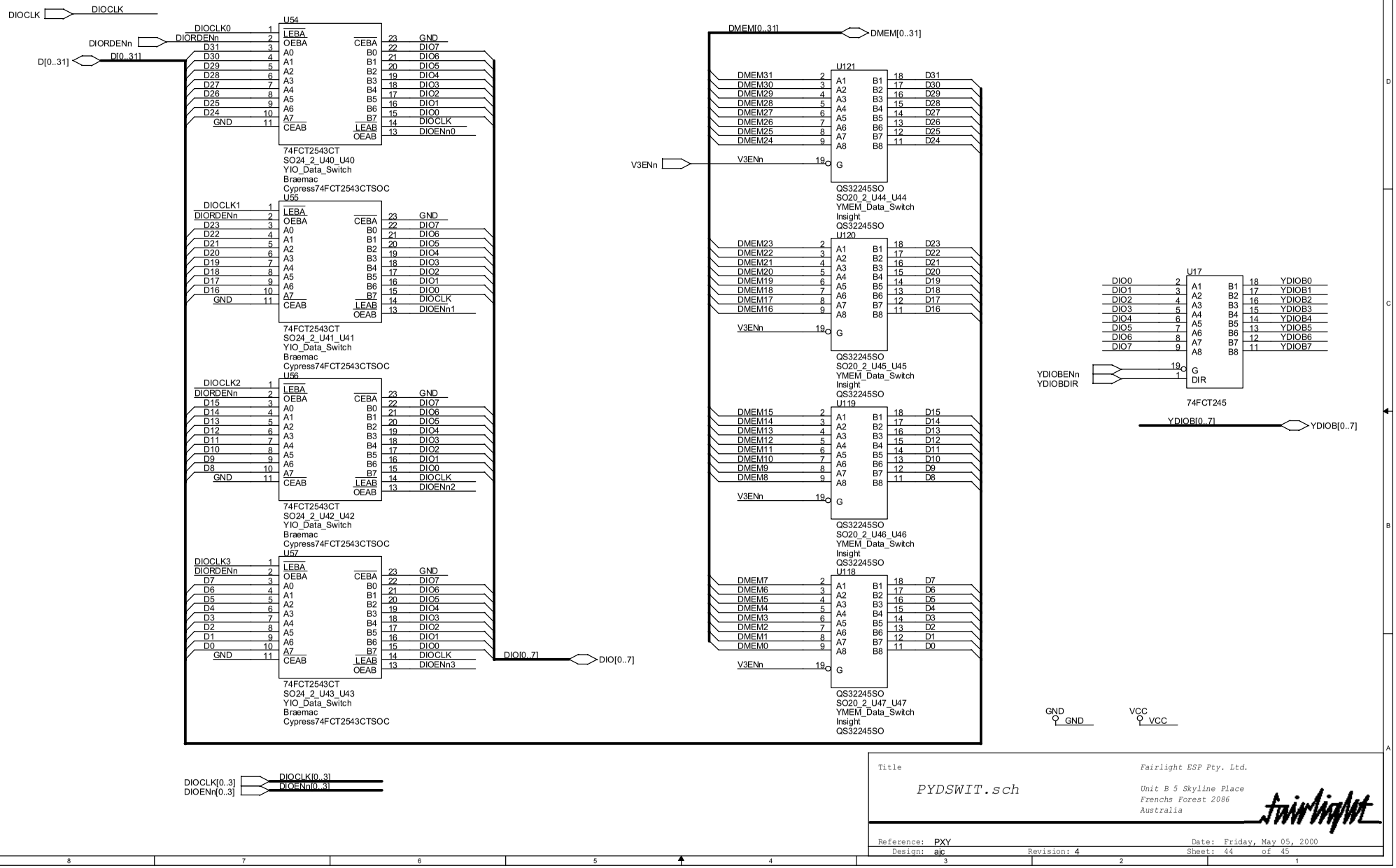
CAS(bmc)_START = CAS(bmc)-XOR-CAS(bmc)_delayed * !MEMCLK_delayed

CAS(bmc)_END = CAS(bmc)-XOR-CAS(bmc)_delayed * MEMCLK_delayed

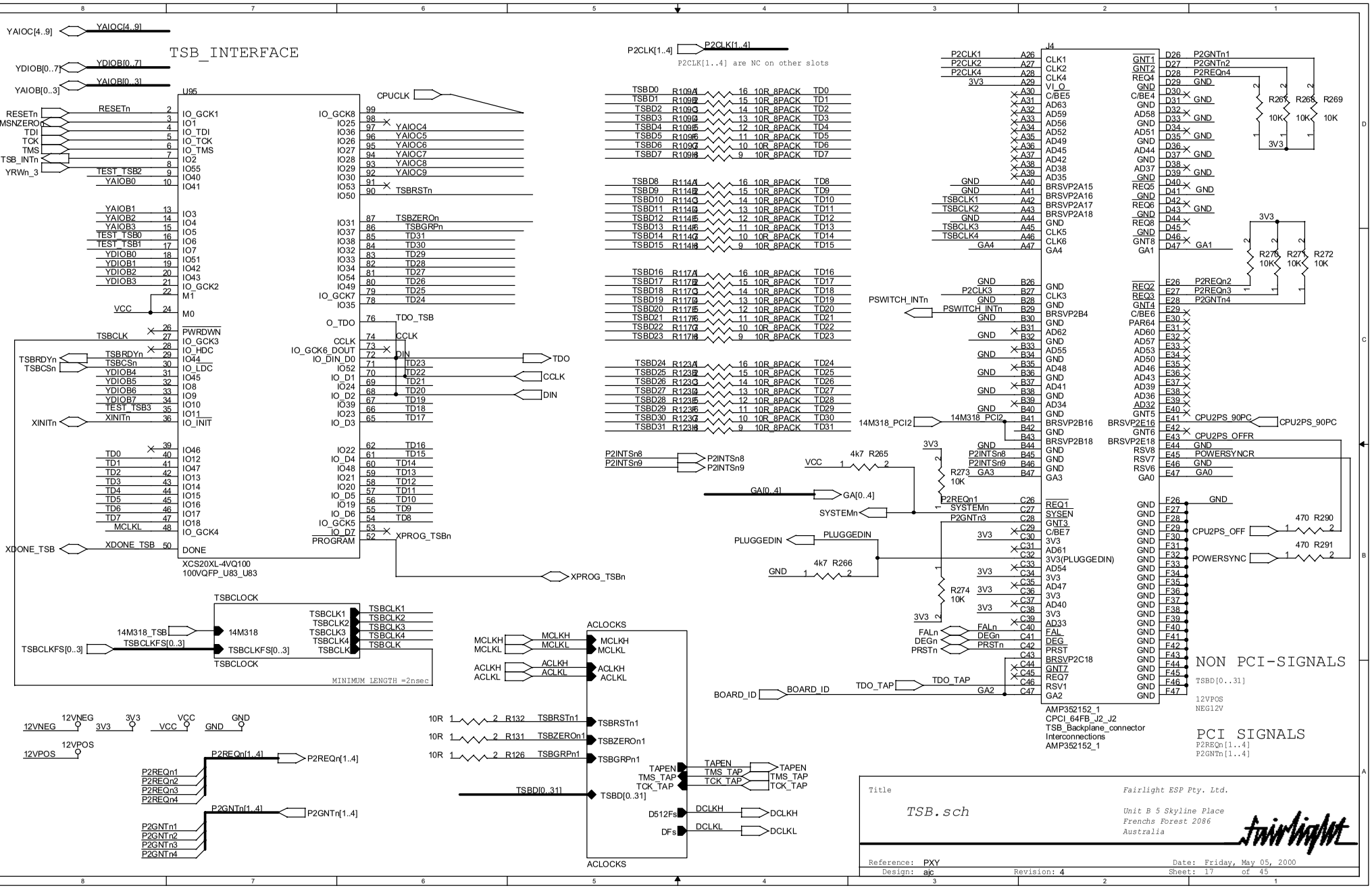
Title <Title>		
Size A	Document Number <Doc>	Rev <RevCode>
Date: Thursday, November 11, 1999	Sheet 1 of 1	


SHEET8
CLOCKS
PCLK_PX
PCLK_PY
PCLK_IO
BCLK_PX
BCLK_PY
BCLK_BMCX
BCLK_BMCY
BCLK_EPCX
BCLK_EPCY
BCLK_IO
BCLK_XG
BCLK_YG
BCLK_IO1
SCSIPCLK
XPCICLK
YPCICLK
BCLK_74
P1CLKS[1..3]
PCICLKFS[0..3]
PCI2CLK
14M318_IO
14M318_PCI2
14M318_TSB
PCICLK_SEL
SLAVEn
CPCICLK_IN
PCI
TDI_PXY
P1AD[0..31]
P1CBEn[0..3]
P1CLKS[1..3]
PCI2CLK
BCLK_IO
SCSIBCLK
SCSIPCLK
TMS_PCI2
TCK_PCI2
TDO_PXY
TDO_PCIS3
TMS_PCI1
TCK_PCI1
REQSCSIn
GNTSCSIn
REQP1Sn[1..3]
GNTP1Sn[1..3]
REQP1P2n
GNTP1P2n
INTP1Sn[1..6]
INTSCSIn
TDI_SCSI
TDO_SCSI
TDO_TAP
TDI_PCIS1
P1PAR
P1FRAMEn
P1TRDYn
P1IRDYn
P1STOPn
P1DEVSELn
P1RESETn
P1PERRn
P1SERRn
TRSTn
PRESENTn[1..3]
P2REQn[1..4]
P2GNTn[1..4]
P2CLK[1..4]
P2INTSn[2..7]
INTS
INTP
PLUGGEDIN
CPCICLK_IN
SYSTEMn
PX
XAIO_CLK
XDIO_CLK
XBMCINIT
PCLK_PX
XPCICLK
BCLK_74
BCLK_PX
BCLK_BMCX
BCLK_XG
BCLK_EPCX
P1PAR
P1FRAMEn
P1TRDYn
P1IRDYn
P1STOPn
P1DEVSELn
P1PERRn
P1SERRn
REQP1PXn
GNTP1PXn
XDIORDENn
P1AD[0..31]
P1C_BE[0..3]
PXST[0..3]
PXIPENDn
AIOCLK
DIOCLK
BMCINIT
PCLK
PCICLK
BCLK_74
BCLK
BCLK_BMC
BCLK_XG
BCLK_EPC
PAR
FRAMEn
TRDYn
IRDYn
STOPn
DEVSELn
PERRn
SERRn
REQP1n
GNTP1n
DIORDENn
AD[0..31]
CBEn[0..3]
PST[0..3]
PIPENDn
DIOCLK[0..3]
DIOENn[0..3]
AIOENn
SYSTEMn
TMS
TCK
TDI_PX
TDO_PX
TDI_XG
TDO_XG
PSIZ[0..1]
PTM[0..2]
PIPLn[0..2]
DIO[0..7]
TOYIOn
TOXIOn
AIO[22..27]
AIO[2..22]
APIO[0..1]
PTT[0..1]
VECIOn
PTBIn
PTAn
PTEAn
PRWn
INTEPCn
PLOCKn
PLOCKEn
PRSTOn
PRSTIn
REFRESHn
TIMERINTn
XDIOCLK[0..3]
XDIOENn[0..3]
TMS_PXPY
TCK_PXPY
TDO_SCSI
TDO_XINIT
PXSIZ[0..1]
PXTM[0..2]
PXIPLn[0..2]
XDIO[0..7]
XTOYIOn
XTOXIOn
XAIO[22..27]
XAIO[2..22]
XAPIO[0..1]
PXTT[0..1]
XVECIOn
PXTBIn
Wired OR
PXTAn
PXTEAn
PXRWn
XINTEPCn
PXLOCKn
PXLOCKEn
PXRSTOn
PXRSTIn
XREFRESHn
XTIMERINTn
PY
YAIO_CLK
YDIO_CLK
YBMCINIT
PCLK_PY
YPCICLK
BCLK_PY
BCLK_BMCY
BCLK_YG
BCLK_EPCY
P1PAR
P1FRAMEn
P1TRDYn
P1IRDYn
P1STOPn
P1DEVSELn
P1PERRn
P1SERRn
REQP1PYn
GNTP1PYn
YDIORDENn
YDIOBENn
YDIOBDIRn
PYST[0..3]
PYIPENDn
YDIOCLK[0..3]
YDIOENn[0..3]
TMS_PXPY
TCK_PXPY
TDO_PX
TDO_PY
TDI_YG
TDO_YG
YAIOENn
PSIZ[0..1]
YDIOB[0..7]
PTM[0..2]
PIPLn[0..2]
DIO[0..7]
TOYIOn
TOXIOn
AIO[22..27]
AIO[2..22]
APIO[0..1]
PTT[0..1]
VECIOn
PTBIn
INTEPCn
PTAn
PTEAn
PRWn
PLOCKn
PLOCKEn
PRSTOn
PRSTIn
REFRESHn
TIMERINTn
YDIOCLK[0..3]
YDIOENn[0..3]
TMS_PXPY
TCK_PXPY
TDO_PX
TDO_PY
TDO_XG
TDO_YG
YAIOENn
PSIZ[0..1]
YDIOB[0..7]
PTM[0..2]
PYIPLn[0..2]
YDIO[0..7]
YTOYIOn
YTOXIOn
YAIO[22..27]
YAIO[2..22]
YAPIO[0..1]
PYTT[0..1]
YVECIOn
PYTBIn
YINTEPCn
PYTAn
PYTEAn
PYRWn
PYLOCKn
PYLOCKEn
PYRSTOn
PYRSTIn
YREFRESHn
YTIMERINTn
IO
PCICLKFS[0..3]
TDO_PCIS3
TDI_CG5A
XAIOENn
SYSTEMn
PLUGGEDIN
SLAVEn
XBMCINIT
YBMCINIT
TDO_YG
TDI_PXY
14M318_TSB
TDO_IO
PXSIZ[0..1]
PXTM[0..2]
PXIPLn[0..2]
XDIO[0..7]
XTOYIOn
XTOXIOn
XAIO[22..27]
XAIO[2..22]
XAPIO[0..1]
PXTT[0..1]
XVECIOn
PXTBIn
PXTAn
PXTEAn
PXRWn
XINTEPCn
PXLOCKn
PXLOCKEn
PXRSTOn
PXRSTIn
XREFRESHn
XTIMERINTn
14M318_IO
BCLK_IO
14M318_PCI2
PCLK_IO
P1CLK
INTP1Sn[1..6]
INTSCSIn
P1PRESn[1..3]
P2REQn[1..4]
P2GNTn[1..4]
REQP1Sn[1..3]
GNTP1Sn[1..3]
REQSCSIn
GNTSCSIn
BCLK_IO1
YAIOENn
PYSIZ[0..1]
YDIOB[0..7]
PYTM[0..2]
PYIPLn[0..2]
YDIO[0..7]
YTOYIOn
YTOXIOn
YAIO[22..27]
YAIO[2..22]
YAPIO[0..1]
PYTT[0..1]
YVECIOn
PYTBIn
YINTEPCn
PYTAn
PYTEAn
PYRWn
PYLOCKn
PYLOCKEn
PYRSTOn
PYRSTIn
YREFRESHn
YTIMERINTn
TDO_XINIT
TMS_PCI1
TMS_PCI2
TMS_PXPY
TCK_PCI1
TCK_PCI2
TCK_PXPY
TDO_PXY
TDO_PY
TDO_TAP
XDIOCLK[0..3]
XDIOENn[0..3]
YDIOCLK[0..3]
YDIOENn[0..3]
XDIORDENn
YDIORDENn
XAIO_CLK
YAIO_CLK
RESETP1n
P1RESETn
PCICLK_SEL
REQP1PXn
GNTP1PXn
REQP1PYn
GNTP1PYn
REQP1P2n
GNTP1P2n
P2CLK[1..4]
P2INTSn[2..7]
INTS
INTP
PXST[0..3]
PXIPENDn
PYST[0..3]
PYIPENDn
XDIO_CLK
YDIO_CLK
YDIOBENn
YDIOBDIRn
TRSTn
Title
MW4PXY.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 1 of 45


R79A 1 16 10R_8PACK
MWEn MWEn R79B 2 15 10R_8PACK MWERn
RASn0 RASn0 R79D 4 13 10R_8PACK RASRn0
RASn1 RASn1 R79C 3 14 10R_8PACK RASRn1
CASn3 CASn3 R79E 5 12 10R_8PACK CASRn3
CASn2 CASn2 R79F 6 11 10R_8PACK CASRn2
CASn1 CASn1 R79G 7 10 10R_8PACK CASRn1
CASn0 CASn0 R79H 8 9 10R_8PACK CASRn0
A11 A11 R80A 1 16 10R_8PACK AR11
A10 A10 R80B 2 15 10R_8PACK AR10
A9 A9 R80C 3 14 10R_8PACK AR9
A8 A8 R80D 4 13 10R_8PACK AR8
A7 A7 R80E 5 12 10R_8PACK AR7
A6 A6 R80F 6 11 10R_8PACK AR6
A5 A5 R80G 7 10 10R_8PACK AR5
A4 A4 R80H 8 9 10R_8PACK AR4
A3 A3 R81A 1 16 10R_8PACK AR3
A2 A2 R81B 2 15 10R_8PACK AR2
A1 A1 R81C 3 14 10R_8PACK AR1
A0 A0 R81D 4 13 10R_8PACK AR0
R81E 5 12 10R_8PACK
R81F 6 11 10R_8PACK
R81G 7 10 10R_8PACK
R81H 8 9 10R_8PACK
TXn
OEABn
LEBAn
U42
RASRn1
RASRn0
CASRn0
CASRn2
CASRn1
CASRn3
MWERn
AR11
AR10
AR9
AR8
AR7
AR6
AR5
AR4
AR3
AR2
AR1
AR0
RAS3 RAS1 RAS2 RAS0 CAS3 CAS2 CAS1 CAS0 WE NC4 NC3 NC2 NC1 NC0 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
P3 P2 P1 P0 PD4 PD3 PD2 PD1
D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
SIMM_72 SOCKET
72SIM_RIGHT_U7_U7
D[0..31]
U52
U51
U50
U49
LEBAn MWEn D0 D1 D2 D3 D4 D5 D6 D7 TXn
D8 D9 D10 D11 D12 D13 D14 D15
D16 D17 D18 D19 D20 D21 D22 D23
D24 D25 D26 D27 D28 D29 D30 D31
LEBA OEBA A0 A1 A2 A3 A4 A5 A6 A7 CEAB
CEBA B0 B1 B2 B3 B4 B5 B6 B7 LEAB OEAB
GND DMem0 DMem1 DMem2 DMem3 DMem4 DMem5 DMem6 DMem7 OEABn
DMem8 DMem9 DMem10 DMem11 DMem12 DMem13 DMem14 DMem15
DMem16 DMem17 DMem18 DMem19 DMem20 DMem21 DMem22 DMem23
DMem24 DMem25 DMem26 DMem27 DMem28 DMem29 DMem30 DMem31
74FCT2543CT
SO24_2_U3_U3
Dram_data_Latch
Braemac
Cypress74FCT2543CTSOC
SO24_2_U4_U4
SO24_2_U5_U5
SO24_2_U6_U6
DMEM[0..31]
VCC
GND
Title
XEVENDIM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 33 of 45



Title	PYDSWIT.sch	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference: PXY	Date: Friday, May 05, 2000	
Design: ajc	Revision: 4	Sheet: 44 of 45


TSB_INTERFACE
U95
XCS20XL-4VQ100
100VQFP_U83_U83
J4
AMP352152_1
CPCI_64FB_J2_J2
TSB_Backplane_connector
Interconnections
AMP352152_1
NON PCI-SIGNALS
PCI SIGNALS
TSB.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 17 of 45

TRACES ON BACKPLANE ARE 65OHM

CLOCK LINES USE TWO PINS, AND TWO TRACES

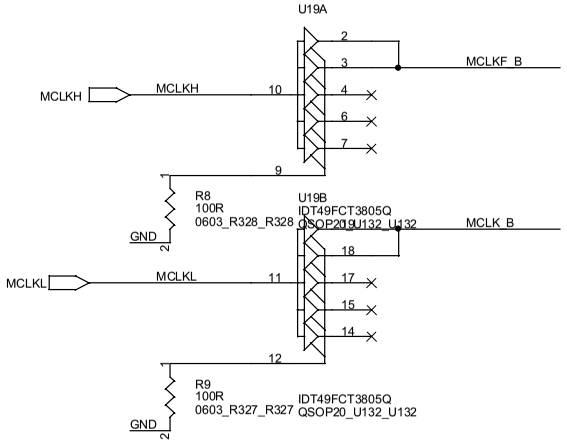
THE TRACES ARE CONNECTED AT EACH POINT WHERE
A BOARD IS PLUGGED IN

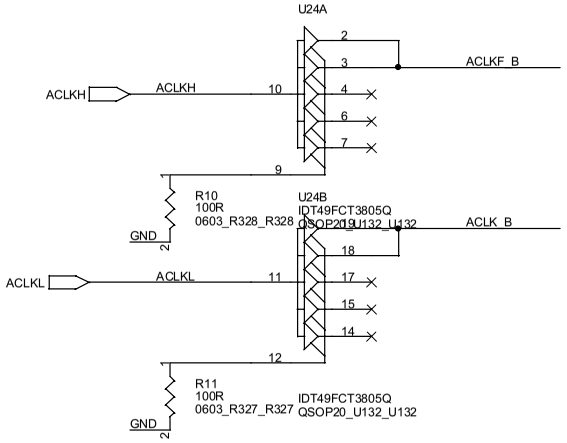
THIS IS SO THE SPARES CAN BE USED AS 65 OR 33 OHM
OR EVEN 22 OHM BY CONNECTING MORE

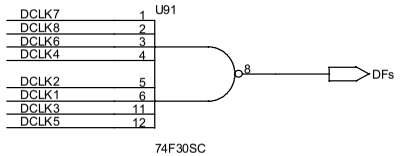
33 OHM TRACES ON ONE SIDE OF BACKPLANE

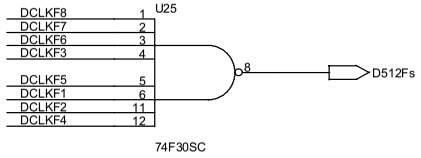
RESERVED FOR FUTURE USE

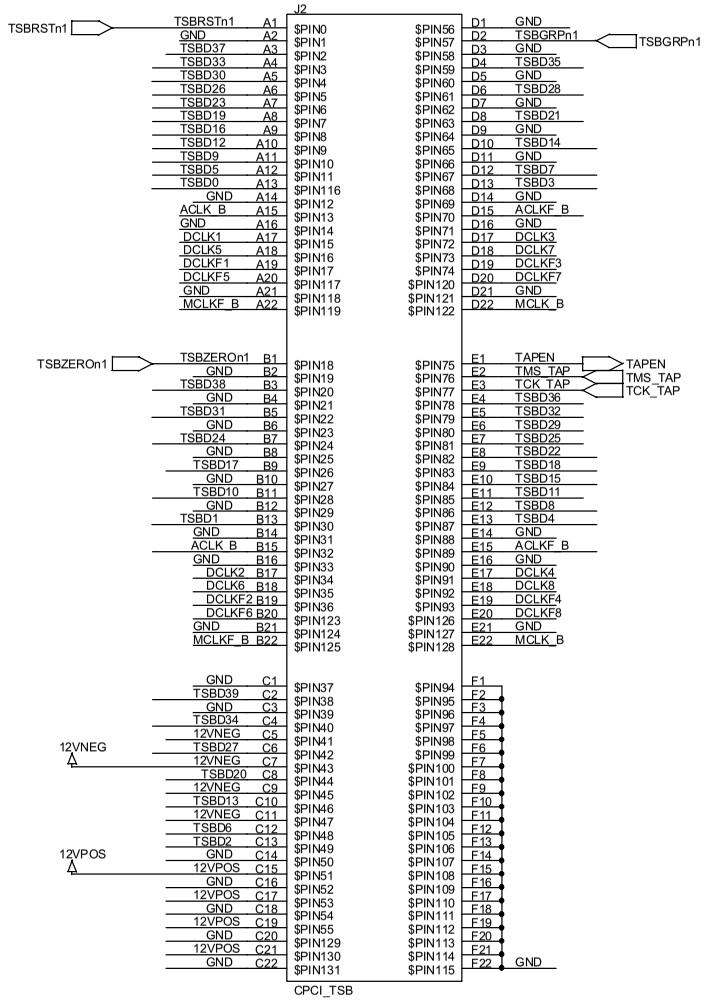
TSBD[0..31] <-> TSBD[0..31]



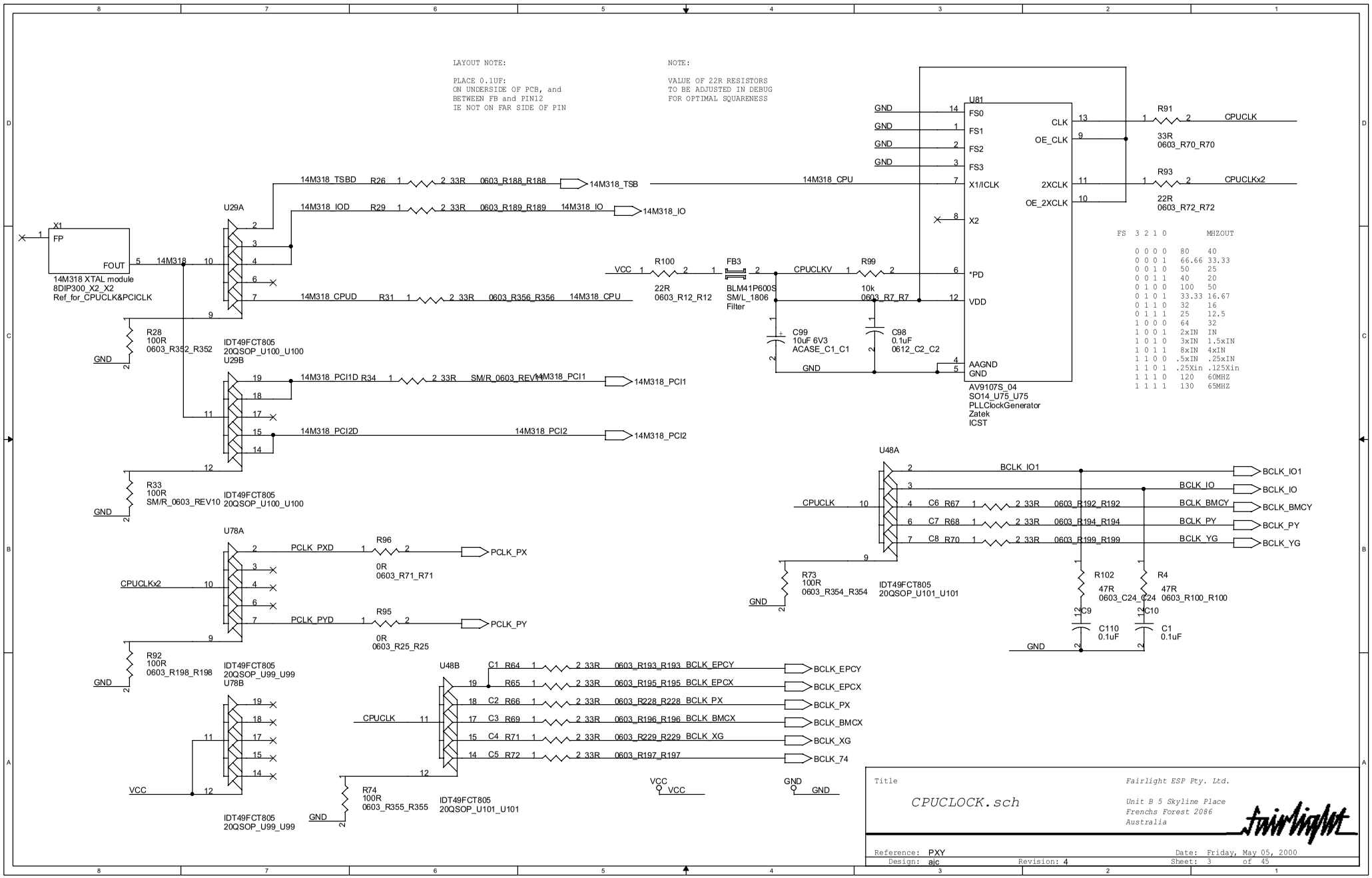


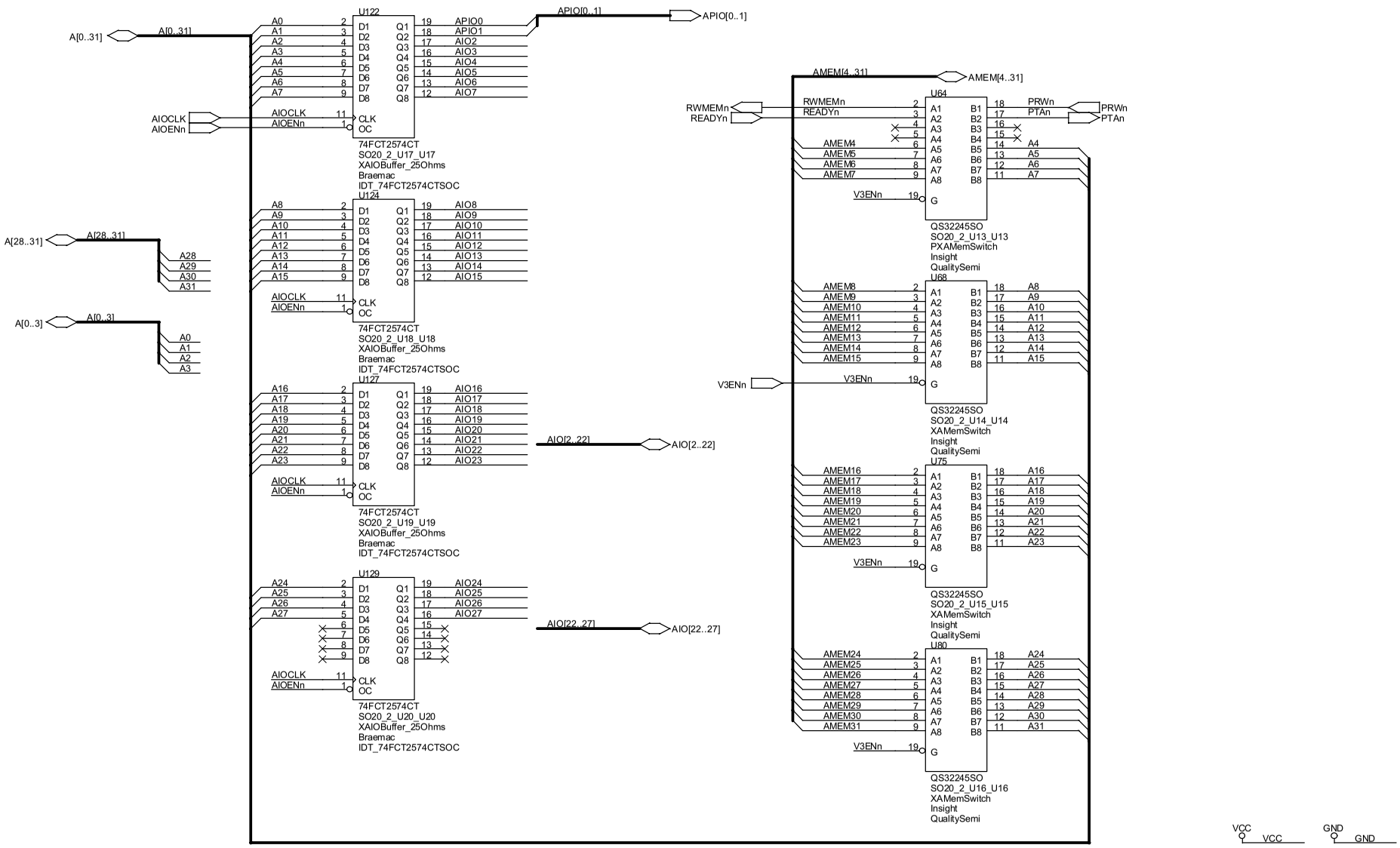




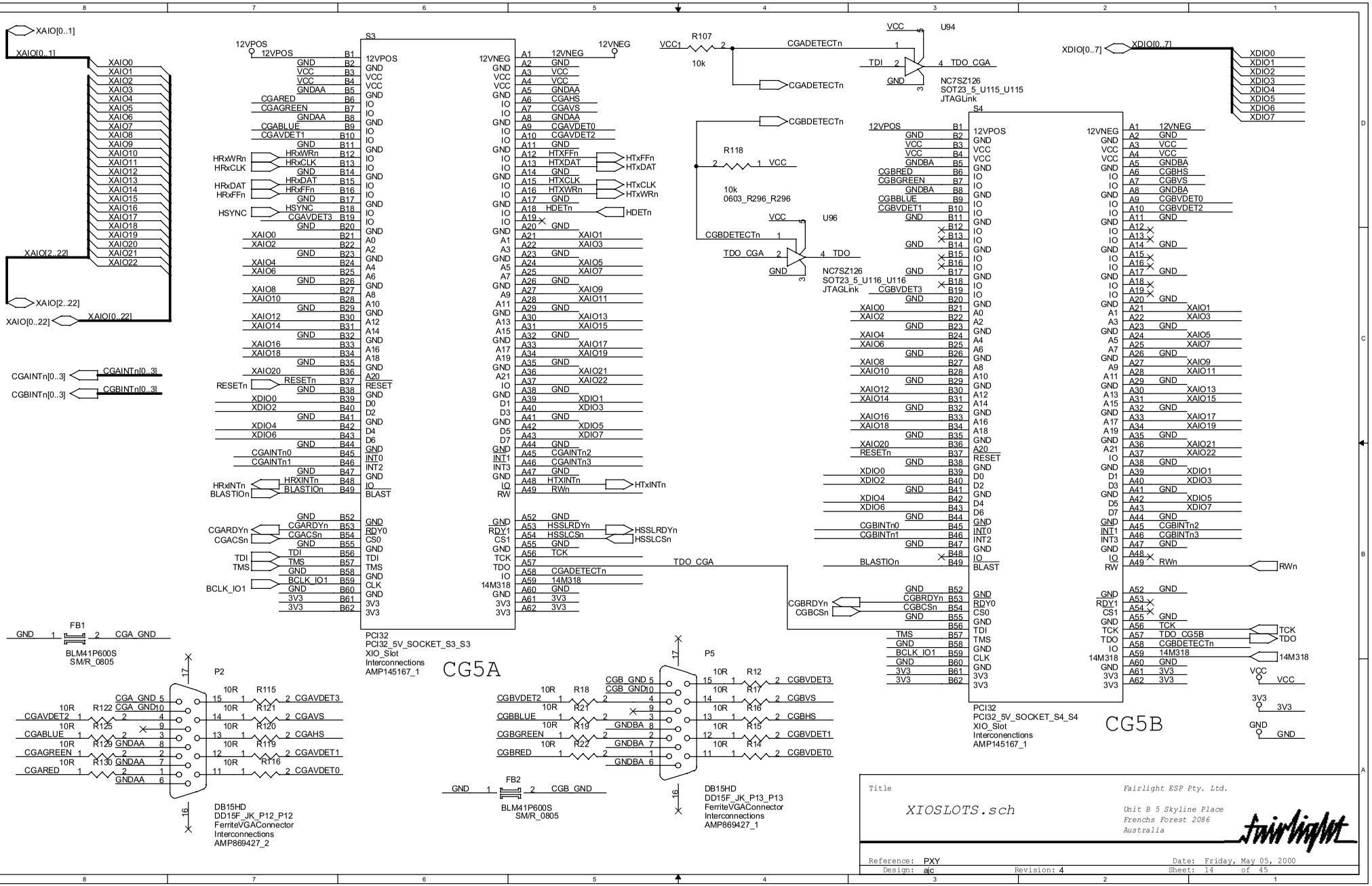


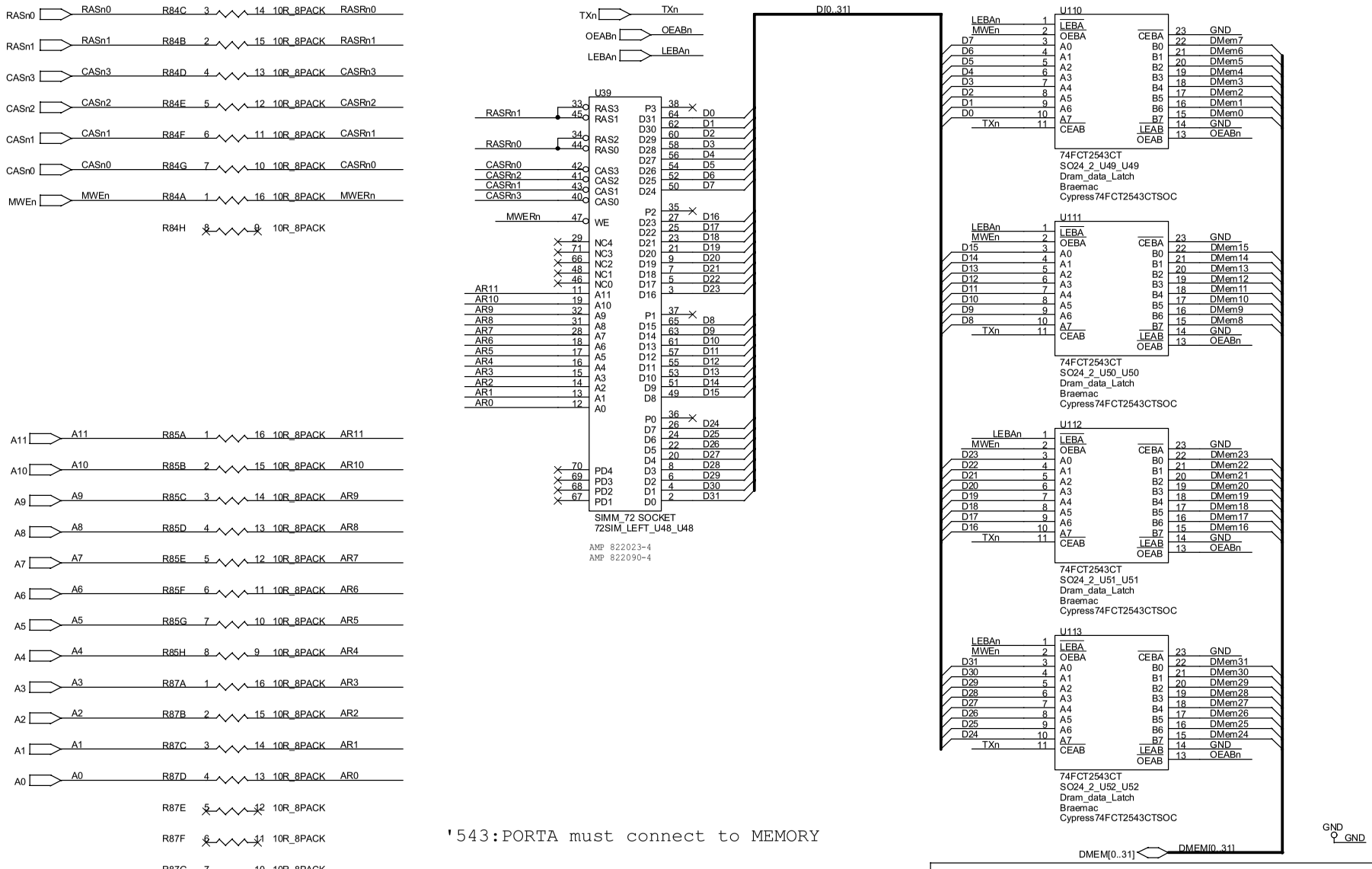
Title	ACLOCKS.sch
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place, Frenchs Forest 2086, Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 18 of 45


LAYOUT NOTE:
PLACE 0.1UF:
ON UNDERSIDE OF PCB, and
BETWEEN FB and PIN12
IE NOT ON FAR SIDE OF PIN
NOTE:
VALUE OF 22R RESISTORS
TO BE ADJUSTED IN DEBUG
FOR OPTIMAL SQUARENESS
U81
AV9107S_04
SO14_U75_U75
PLLClockGenerator
Zatek
ICST
FS 3 2 1 0 MHZOUT
0 0 0 0 80 40
0 0 0 1 66.66 33.33
0 0 1 0 50 25
0 0 1 1 40 20
0 1 0 0 100 50
0 1 0 1 33.33 16.67
0 1 1 0 32 16
0 1 1 1 25 12.5
1 0 0 0 64 32
1 0 0 1 2xIN IN
1 0 1 0 3xIN 1.5xIN
1 0 1 1 8xIN 4xIN
1 1 0 0 .5xIN .25xIN
1 1 0 1 .25Xin .125Xin
1 1 1 0 120 60MHZ
1 1 1 1 130 65MHZ
14M318 XTAL module
8DIP300_X2_X2
Ref_for_CPUCLK&PCICLK
IDT49FCT805
20QSOP_U100_U100
U29B
IDT49FCT805
20QSOP_U100_U100
IDT49FCT805
20QSOP_U101_U101
IDT49FCT805
20QSOP_U99_U99
U78B
IDT49FCT805
20QSOP_U99_U99
BLM41P600S
SM/L_1806
Filter
U29A
U78A
U48A
U48B
14M318_TSBD
14M318_IOD
14M318_CPUD
14M318_PCI1D
14M318_PCI2D
14M318_TSB
14M318_IO
14M318_CPU
14M318_PCI1
14M318_PCI2
PCLK_PXD
PCLK_PYD
PCLK_PX
PCLK_PY
BCLK_IO1
BCLK_IO
BCLK_BMCY
BCLK_PY
BCLK_YG
BCLK_EPCY
BCLK_EPCX
BCLK_PX
BCLK_BMCX
BCLK_XG
BCLK_74
CPUCLK
CPUCLKx2
CPUCLKV
VCC
GND
Title
CPUCLOCK.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: aic
Revision: 4
Date: Friday, May 05, 2000
Sheet: 3 of 45



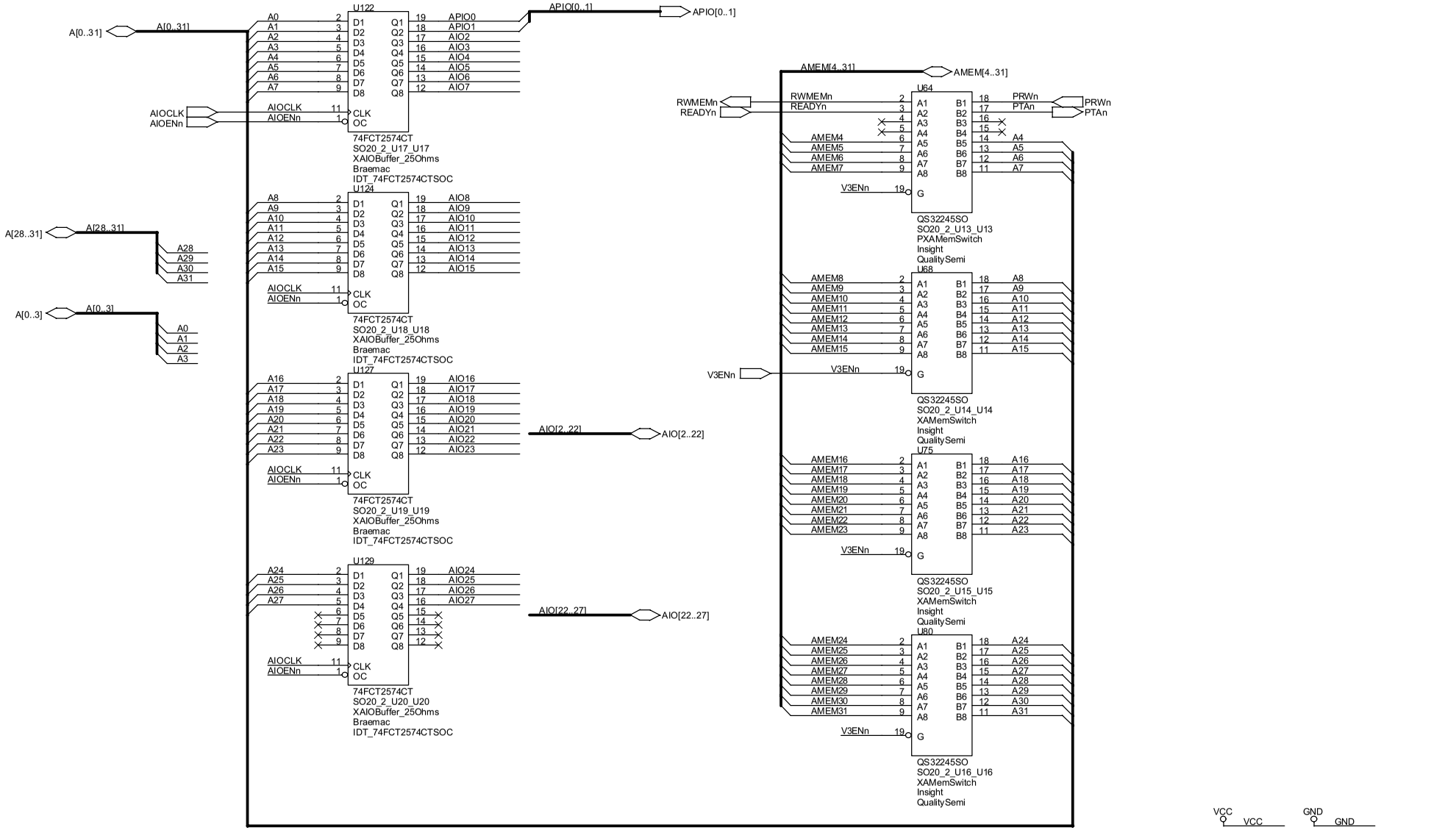
Title	PXASWIT.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	PXY
Design:	ajc
Revision:	4
Date:	Friday, May 05, 2000
Sheet:	30 of 45

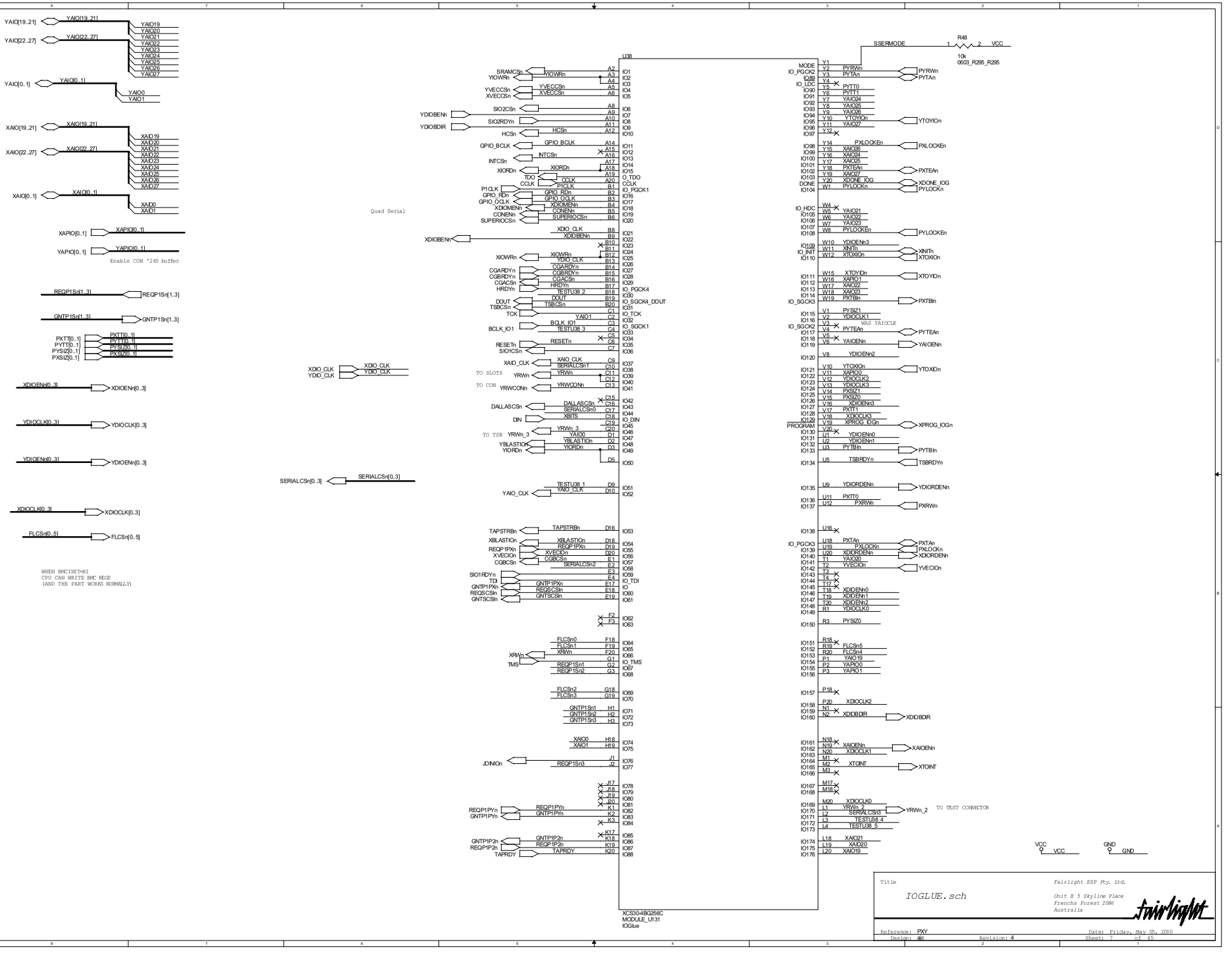

CG5A
CG5B
S3
S4
P2
P5
U94
U96
R107
R118
PCI32
PCI32_5V_SOCKET_S3_S3
XIO_Slot
Interconnections
AMP145167_1
PCI32_5V_SOCKET_S4_S4
DB15HD
DD15F_JK_P12_P12
FerriteVGAConnector
AMP869427_2
DD15F_JK_P13_P13
AMP869427_1
NC7SZ126
SOT23_5_U115_U115
JTAGLink
SOT23_5_U116_U116
BLM41P600S
SM/R_0805
Title
XIOSLOTS.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 14 of 45

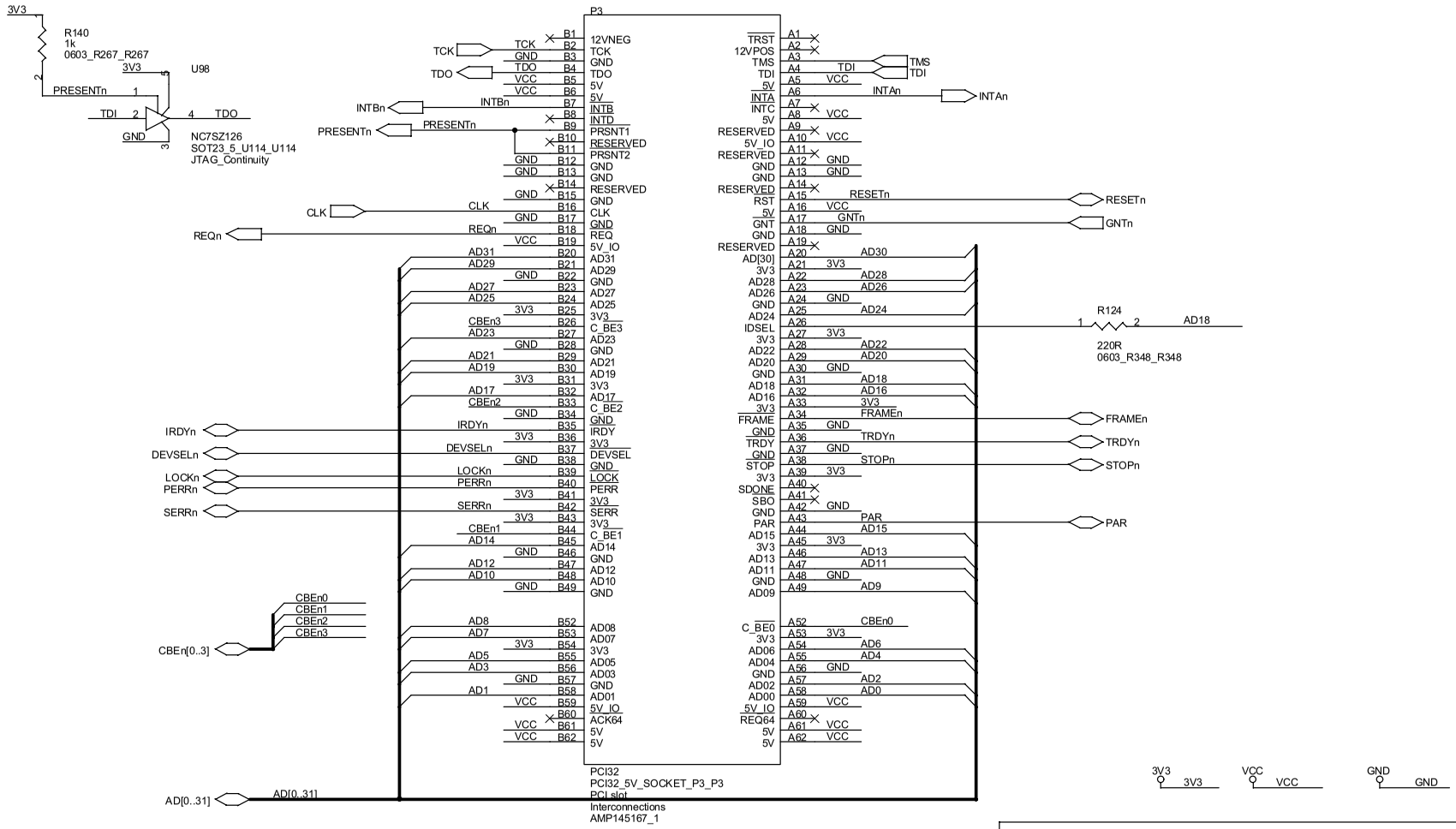


'543:PORTA must connect to MEMORY

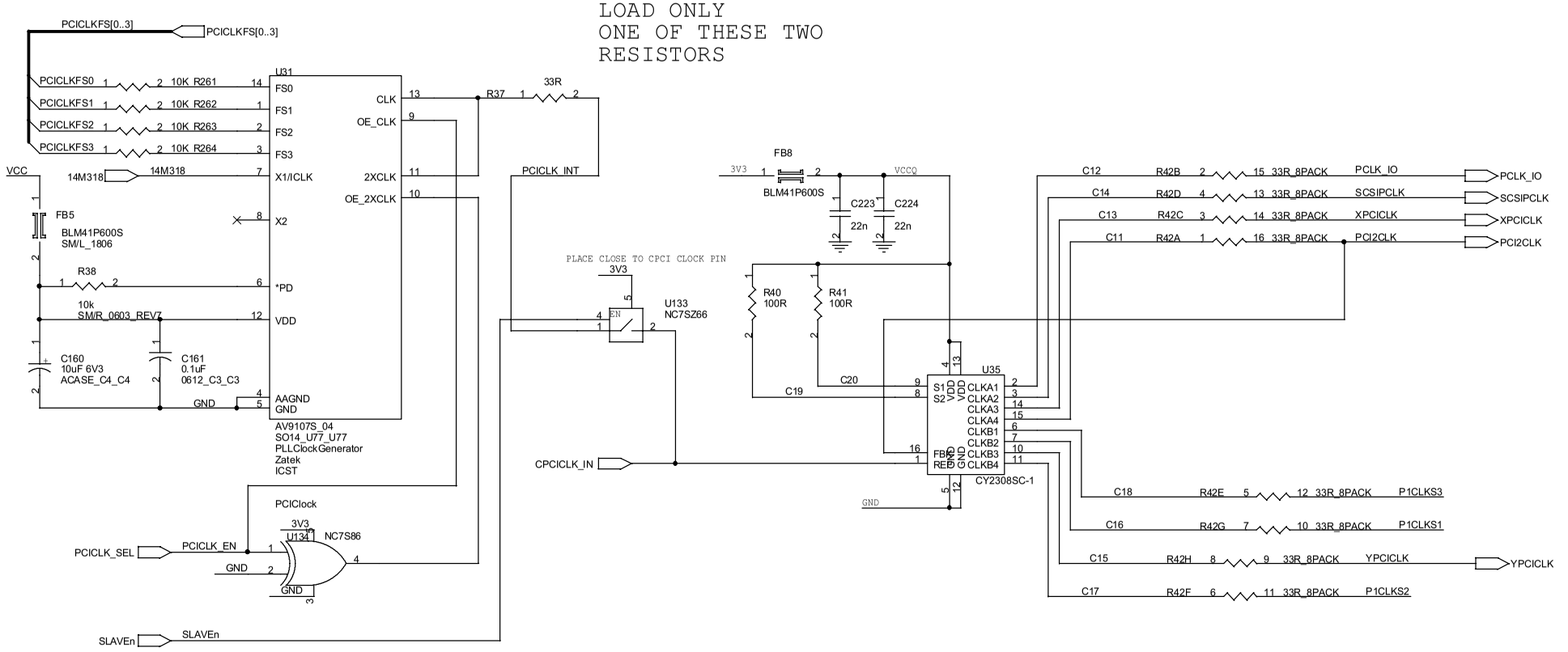
Title	*YODD_DIM.sch*	*Fairlight ESP Pty. Ltd.* *Unit B 5 Skyline Place* *Frenchs Forest 2086* *Australia*
Reference: PXY	Design: ajc	Revision: 4
Date: Friday, May 05, 2000	Sheet: 42 of 45	


A[0..31]
A[28..31]
A[0..3]
AIOCLK
AIOENn
U122
U124
U127
U129
74FCT2574CT
SO20_2_U17_U17
SO20_2_U18_U18
SO20_2_U19_U19
SO20_2_U20_U20
XAIOBuffer_25Ohms
Braemac
IDT_74FCT2574CTSOC
APIO[0..1]
AIO[2..22]
AIO[22..27]
AMEM[4..31]
RWMEMn
READYn
V3ENn
PRWn
PTAn
U64
U68
U75
U80
QS32245SO
SO20_2_U13_U13
PXAMemSwitch
SO20_2_U14_U14
XAMemSwitch
SO20_2_U15_U15
SO20_2_U16_U16
Insight
QualitySemi
VCC
GND
Title
PXASWIT.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 30 of 45


YAIO[19..21]
YAIO[22..27]
YAIO[0..1]
XAIO[19..21]
XAIO[22..27]
XAIO[0..1]
XAPIO[0..1]
YAPIO[0..1]
Enable CON '245 buffer
REQP1Sn[1..3]
GNTP1Sn[1..3]
PXTT[0..1]
PYTT[0..1]
PYSIZ[0..1]
PXSIZ[0..1]
XDIOENn[0..3]
YDIOCLK[0..3]
YDIOENn[0..3]
XDIOCLK[0..3]
FLCSn[0..5]
WHEN BMCINIT=HI
CPU CAN WRITE BMC REGS
(AND THE PART WORKS NORMALLY)
Quad Serial
XDIO_CLK
YDD_CLK
TO SLOTS
TO CON
TO TSB
SERIALCSn[0..3]
U38
XCS30-4BG256C
MODULE_U131
IOGlue
SSERMODE
R48
10k
0603_R295_R295
VCC
TO TEST CONNECTOR
GND
Title
IOGLUE.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: sic
Revision: 4
Date: Friday, May 05, 2000
Sheet: 7 of 45


NOTE: ONLY INTA* and INTB* CONNECTED
P3
R140
1k
0603_R267_R267
U98
NC7SZ126
SOT23_5_U114_U114
JTAG_Continuity
R124
220R
0603_R348_R348
PCI32
PCI32_5V_SOCKET_P3_P3
PCI slot
Interconnections
AMP145167_1
Title
PCI_S3.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 26 of 45

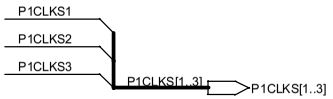
LOAD ONLY
ONE OF THESE TWO
RESISTORS

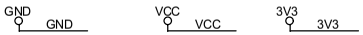


PCICLK will be enabled if

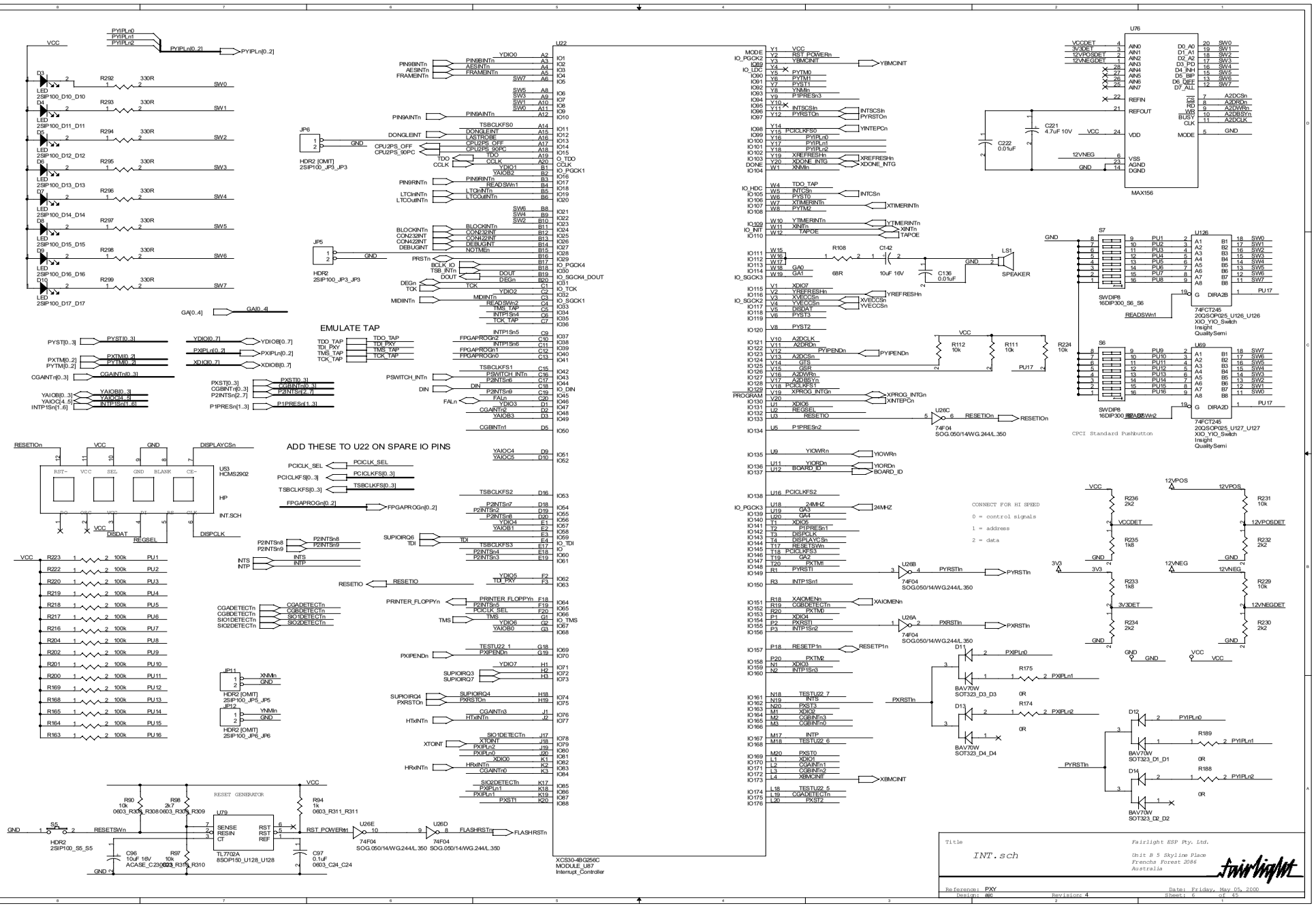
- INTGLUE isn't programmed, or
- PRESENTn is HI (not plugged in), or
- PRESENTn is LO and SYSTEMn is HI (SLAVE)

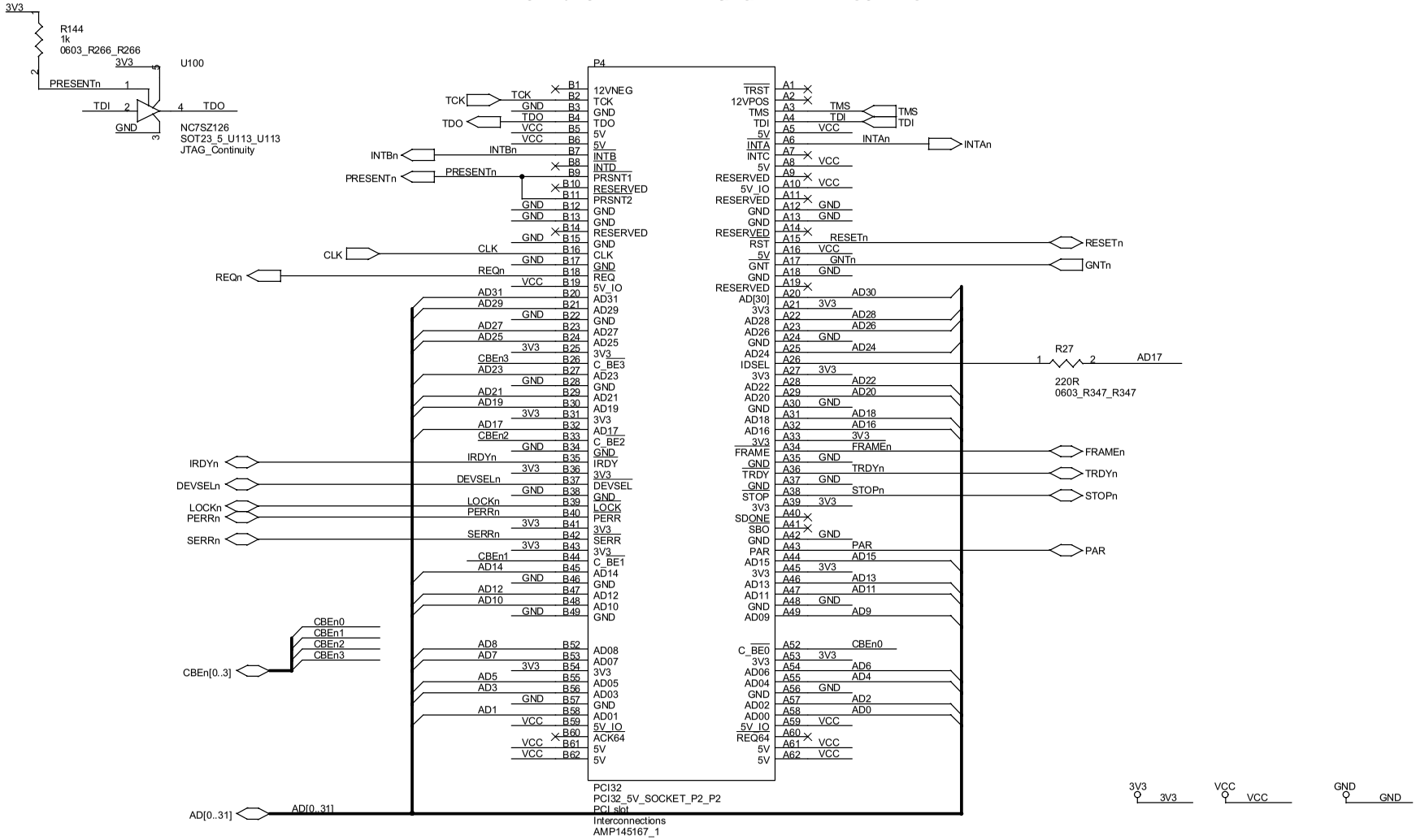
FS 3 2 1 0	MHZOUT	
0 0 0 0	80	40
0 0 0 1	66.66	33.33
0 0 1 0	50	25
0 0 1 1	40	20
0 1 0 0	100	50
0 1 0 1	33.33	16.67
0 1 1 0	32	16
0 1 1 1	25	12.5
1 0 0 0	64	32
1 0 0 1	2xIN	IN
1 0 1 0	3xIN	1.5xIN
1 0 1 1	8xIN	4xIN
1 1 0 0	.5xIN	.25xIN
1 1 0 1	.25Xin	.125Xin
1 1 1 0	120	60MHZ
1 1 1 1	130	65MHZ

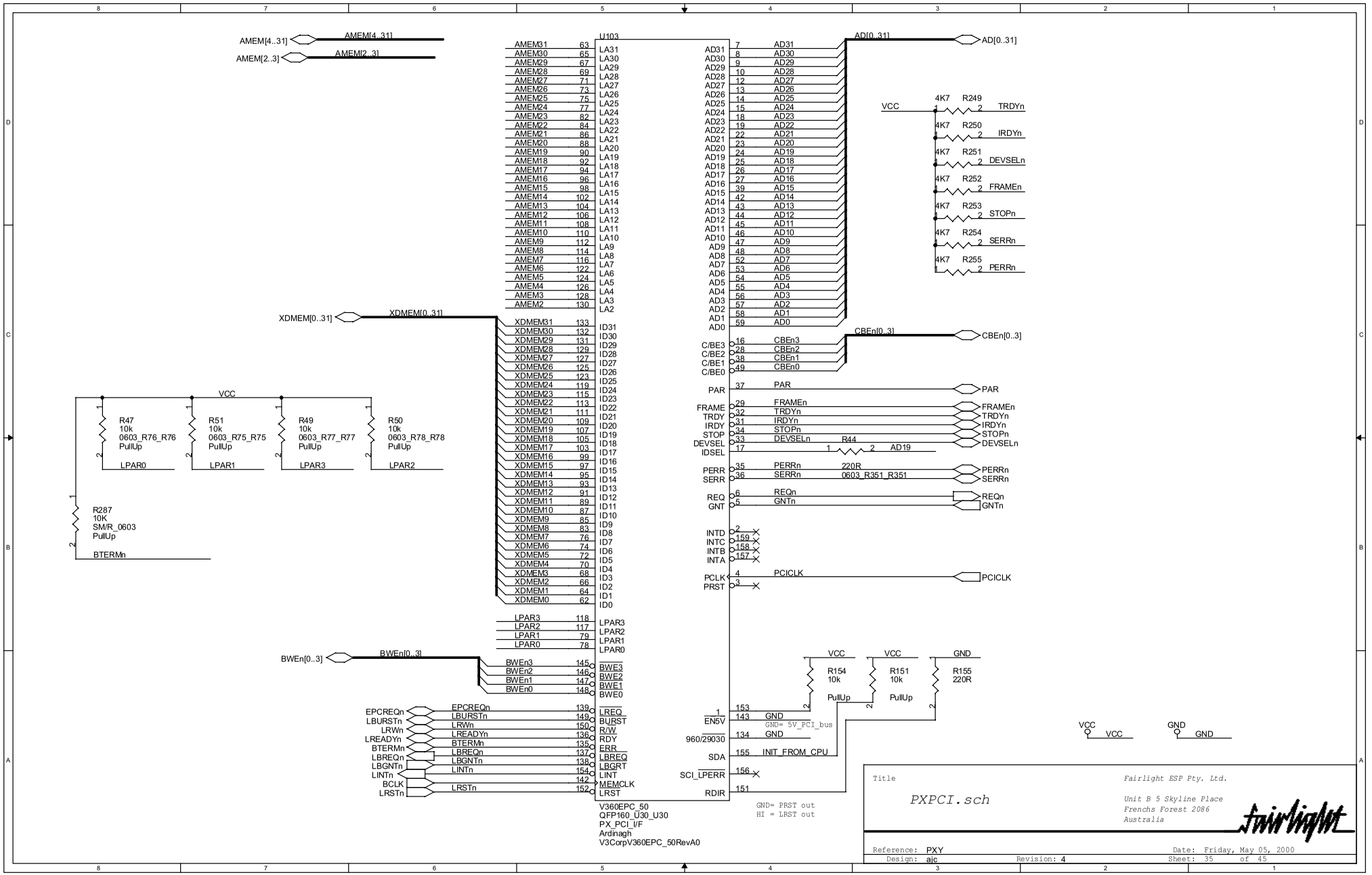




Title	PCICLOCK.sch	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference: PXY	Date: Friday, May 05, 2000	
Design: ajc	Revision: 4	Sheet: 4 of 45


EMULATE TAP
ADD THESE TO U22 ON SPARE IO PINS
U22
XC5304BG256C
MODULE_U87
Internupt_Controller
U76
MAX156
U53
HCMS29X2
INT.SCH
RESET GENERATOR
TL7702A
8SOP150_U128_U128
SWDIP8
16DIP300_S6_S6
SWDIP8
16DIP300_S7_S7
74FCT245
20QSOP025_U126_U126
XIO_YIO_Switch
Insight
QualitySemi
74FCT245
20QSOP025_U127_U127
XIO_YIO_Switch
Insight
QualitySemi
SPEAKER
CPCI Standard Pushbutton
CONNECT FOR HI SPEED
0 = control signals
1 = address
2 = data
BAV70W
SOT323_D3_D3
BAV70W
SOT323_D4_D4
BAV70W
SOT323_D1_D1
BAV70W
SOT323_D2_D2
Title
INT.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: aic
Revision: 4
Date: Friday, May 05, 2000
Sheet: 6 of 45


NOTE: ONLY INTA* and INTB* CONNECTED
R144
1k
0603_R266_R266
U100
NC7SZ126
SOT23_5_U113_U113
JTAG_Continuity
P4
PCI32
PCI32_5V_SOCKET_P2_P2
PCI slot
Interconnections
AMP145167_1
R27
220R
0603_R347_R347
Title
PCI_S2.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 25 of 45



Title: PXPCI.sch

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: PXY
Design: aic
Revision: 4
Date: Friday, May 05, 2000
Sheet: 35 of 45

YGLUE

A[28..31] A[28..31]

A[0..3] A[0..3]

SIZ[0..1] SIZ[0..1]

AMEM[2..3] AMEM[2..3]

TT[0..1] TT[0..1]

U72

BCLK BCLK 22 IO_GCK1
23 IO_GCK2
27 IO_GCK3
NOT ASSIGNED TEMP0 3 IO_GTS1
NOT ASSIGNED TEMP1 4 IO_GTS2
RESETn RESETn 99 IO_GSR

VIO1 26 VCC
VIO2 38
VIO3 51
VIO4 88

16 IO1
V3ENn V3ENn 13 IO2
18 IO3
SYSTEMn SYSTEMn 20 IO4
TSn TSn 14 IO5
VECIOn VECIOn 15 IO6
25 IO7
A31 17 IO8
IO9
REQn REQn 28
33 IO10
REFRESHn REFRESHn 36 IO11
EPCREQn EPCREQn 29 IO12
LBGNTn LBGNTn 39 IO13
30 IO14
RWn RWn 40 IO32
BWEn0 87 IO33
BRn BRn 94 IO34
BGn BGn 91 IO35
BWEn1 93 IO36
LOCKEn LOCKEn 95 IO37
A2 96 IO38
BWEn2 97 IO39
TEMP0 1 IO40
TEMP1 6 IO41
BWEn3 8 IO42
A29 9 IO43
BBn BBn 10 IO44
SIZ1 12 IO45
TIMEOUTn 92 IO46
FromBMC IO47

IO15 66
IO16 64 A28
IO17 71 BURSTn BURSTn
IO18 72
IO19 67 A1
IO20 76 VCC
IO21 77 AMem2
IO22 68 TAn TAn
IO23 70
IO24 81
IO25 74 A30
IO26 82 PTCIn PTCIn
IO27 85 AMem3
IO28 78
IO29 89 A0
IO30 86
IO31 90 TT0
IO66 79 MOD4 MOD4
IO48 41
IO49 32 TOYIOn TOYIOn
IO50 49
IO51 50
IO52 35 SIZ0
IO53 53 BTERMn BTERMn
IO54 54 TOXIOn TOXIOn
IO55 37
IO56 42 LBREQn LBREQn
IO57 60 PTBIn PTBIn
IO58 52 TT1
IO59 61
IO60 63 TEAn TEAn
IO61 55
IO62 56 LOCKn LOCKn
IO63 65
IO64 58 A3
IO65 59

TCK TCK 48 TCK
TDI TDI 45 TDI
TDO 83 TDO TDO
TMS TMS 47 TMS

XC9572-7TQ100C
100TQFP_U76_U76
CPLD_XDecode_MEMglue
ACD
Xilinx

CPU INITIATED
PCI AND DRAM
ACCESS

OUTPUT FROM BMC
(NO PARTICULAR USE)

PCI MASTER TO DRAM

68040 BUS ACCESS

SIZ[0..1] SIZ[0..1]

is BB REQUIRED?

VCC R227 10k SM/R_0603 EPCREQn 2

VCC R228 10k SM/R_0603 REQn 2

TO BMC TO FORCE
68040 MOD4 ADDRESSING DURING BURSTS

EPC PCI MASTER TO DRAM

BWEn[0..3] BWEn[0..3]

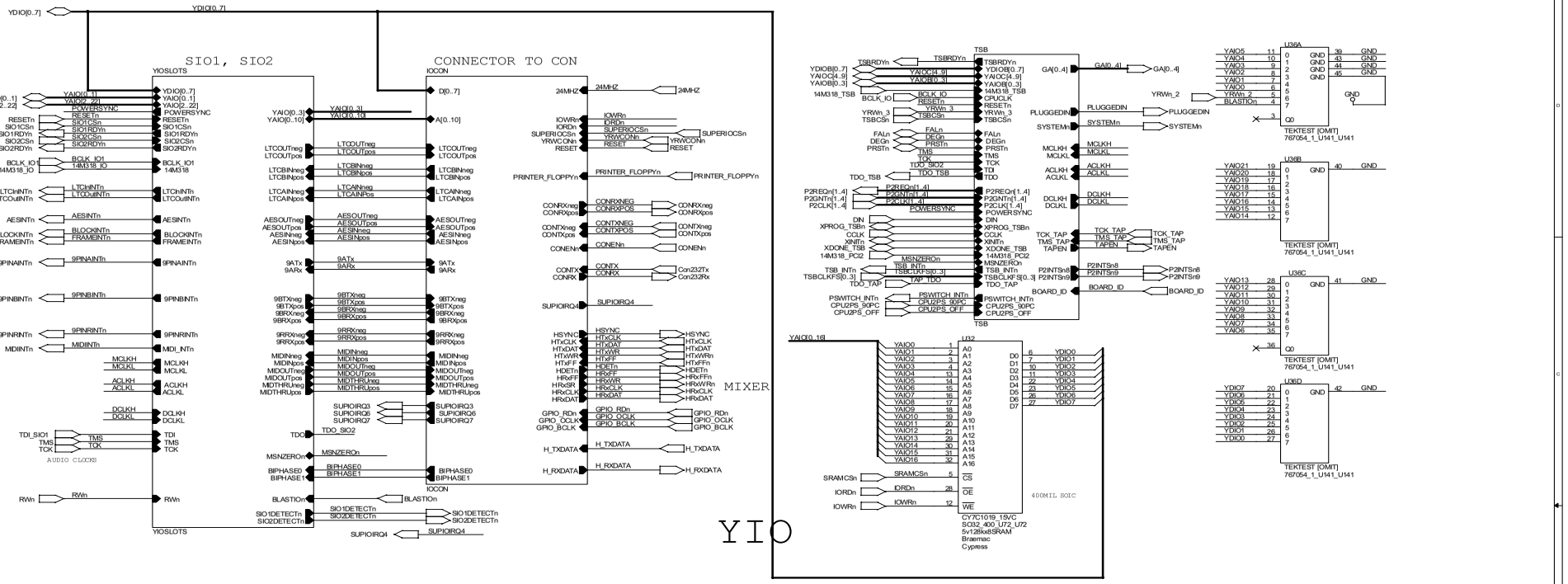
100 76
1 75
U23
25 51
26 50

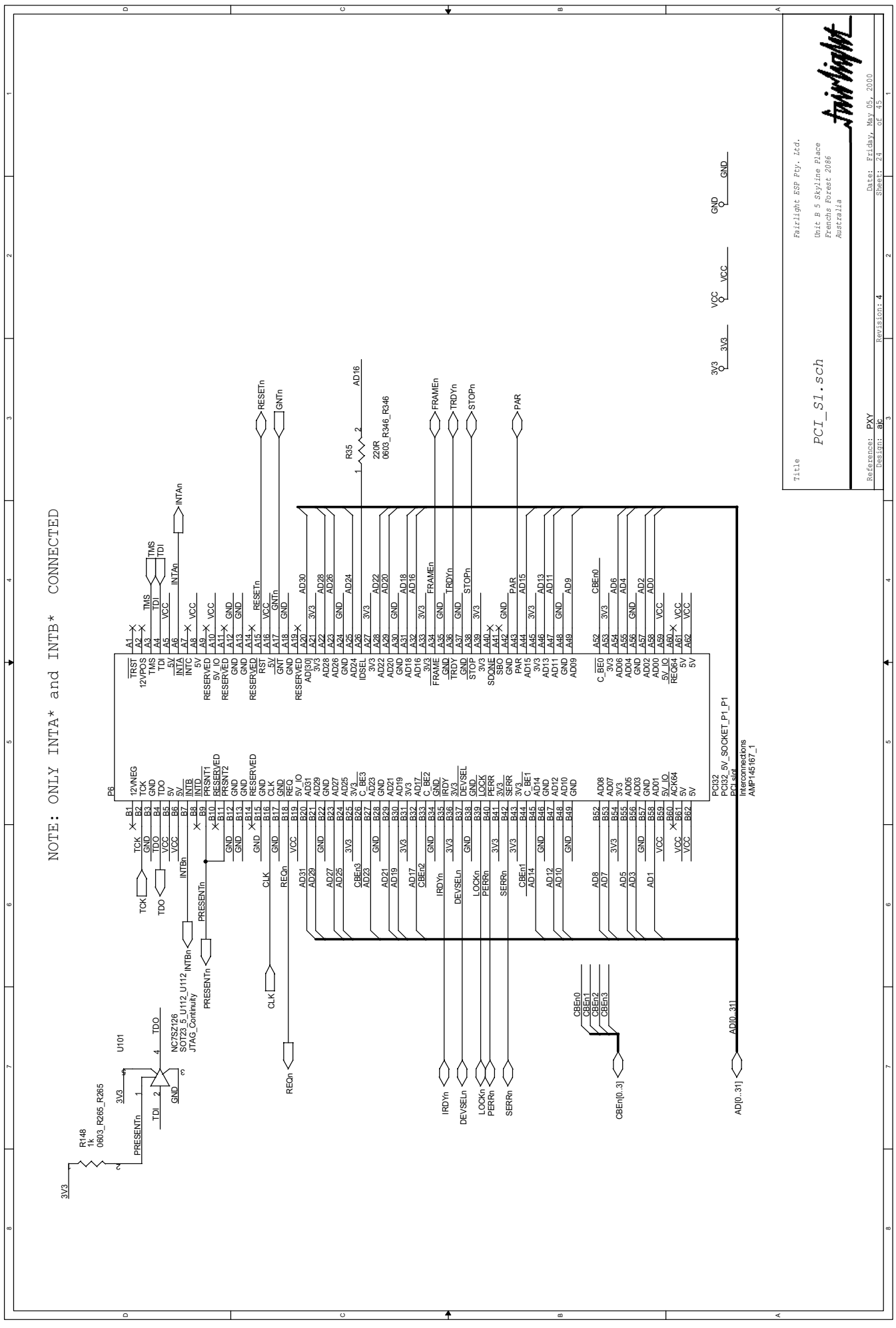
(CHECK WITH CHRIS)
MOD4
BR
BG

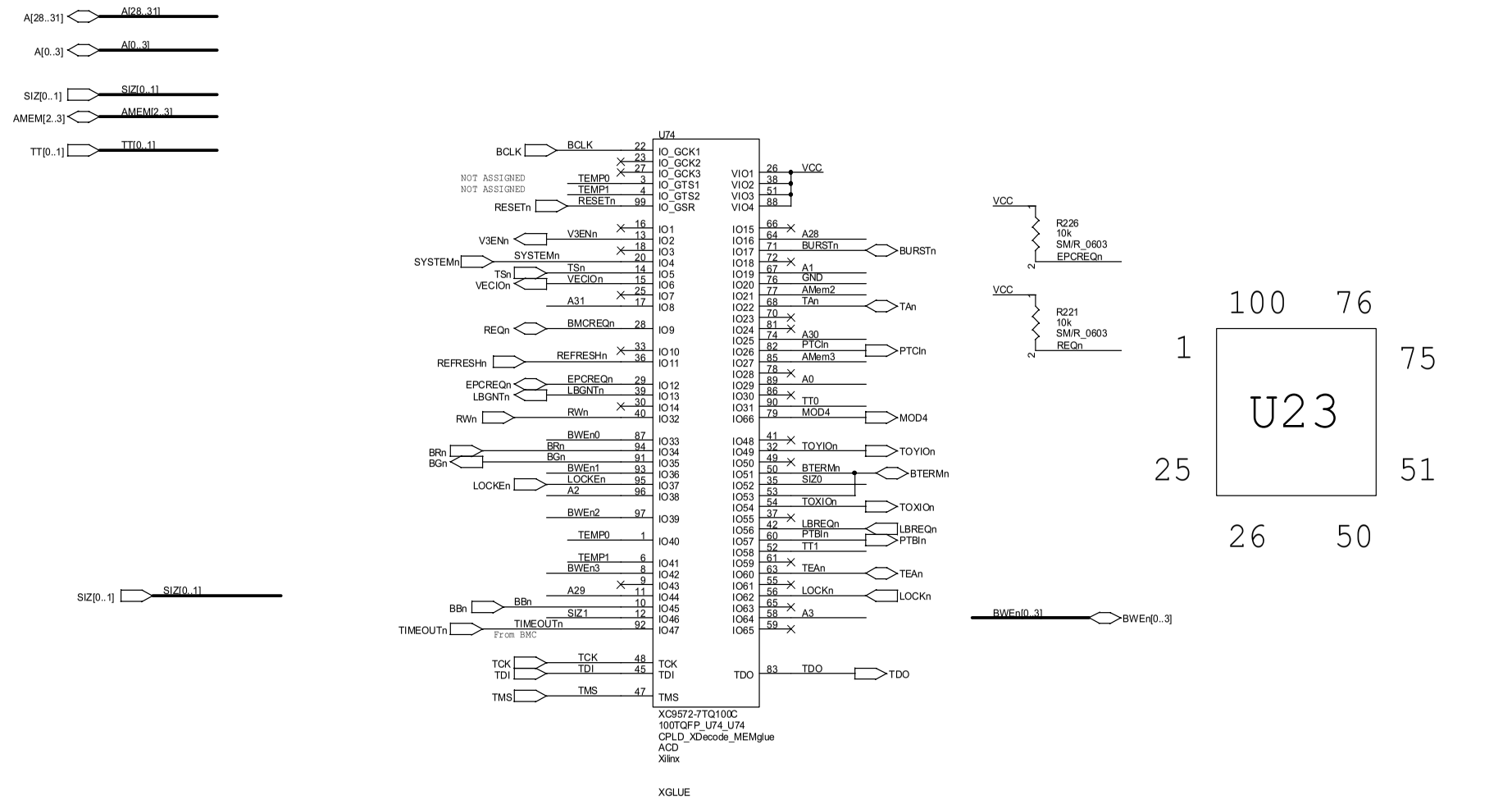
VCC VCC

GND GND

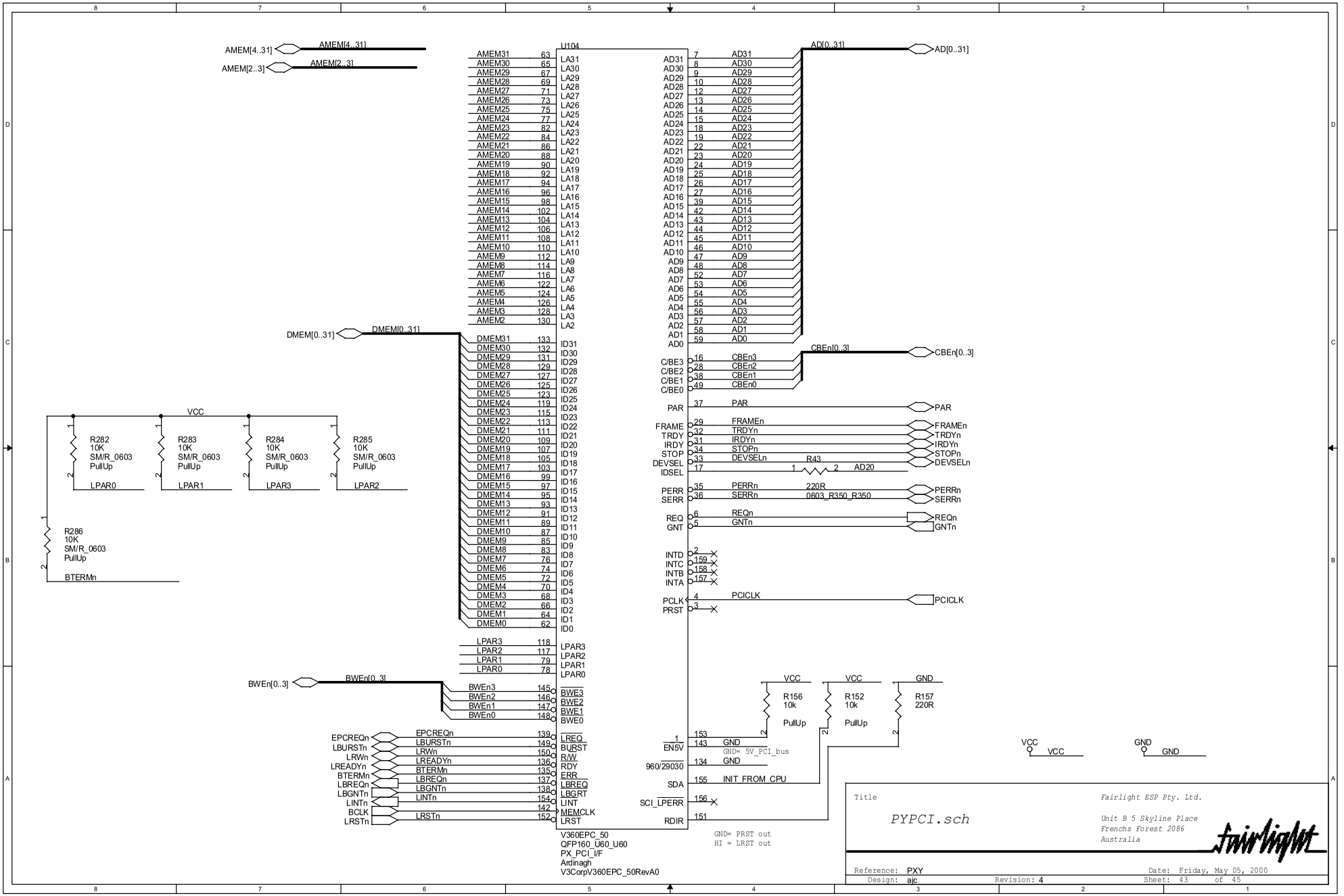
Title	YGLUE.sch	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference: PXY		Date: Friday, May 05, 2000
Design: ajc	Revision: 4	Sheet: 45 of 45

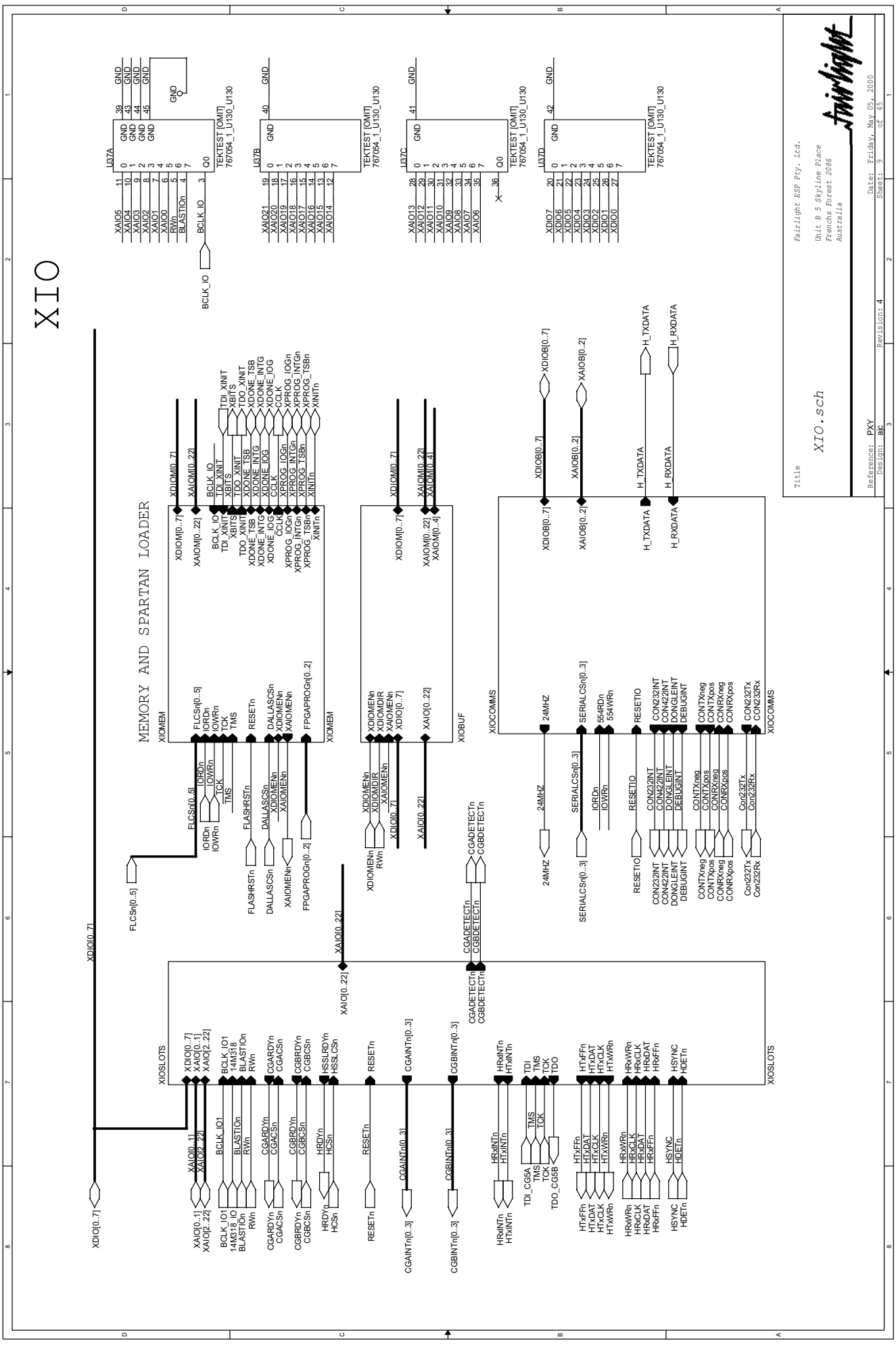

SIO1, SIO2
CONNECTOR TO CON
MIXER
YIO
AUDIO CLOCKS
400MIL SOIC
CY7C1019_15VC
SOJ2_400_U72_U72
5v128kx8SRAM
Braemac
Cypress
TSB
U32
U36A
U36B
U36C
U36D
TEKTEST [OMIT]
767054_1_U141_U141
Title
YIO.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: aic
Revision: 4
Date: Friday, May 05, 2000
Sheet: 15 of 45

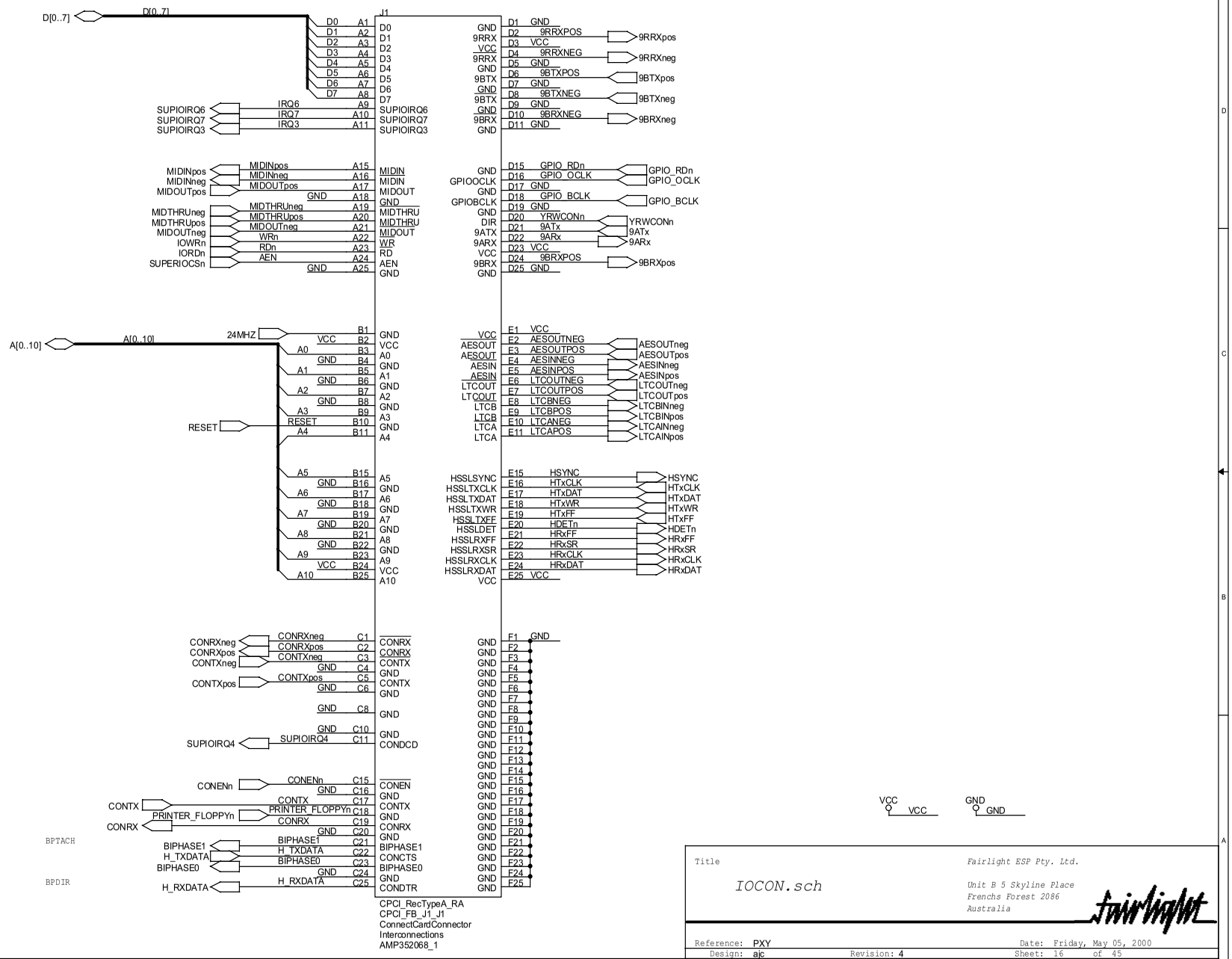

NOTE: ONLY INTA* and INTB* CONNECTED
P6
PCI32_5V_SOCKET_P1_P1
PCI slot
Interconnections
AMP145167_1
R148
1k
0603_R265_R265
U101
NC7SZ126
SOT23_5_U112_U112
JTAG_Continuity
R35
220R
0603_R346_R346
Title
PCI_S1.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: alc
Revision: 4
Sheet: 24 of 45
Date: Friday, May 05, 2000



Title	XGLUE.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4 Sheet: 36 of 45

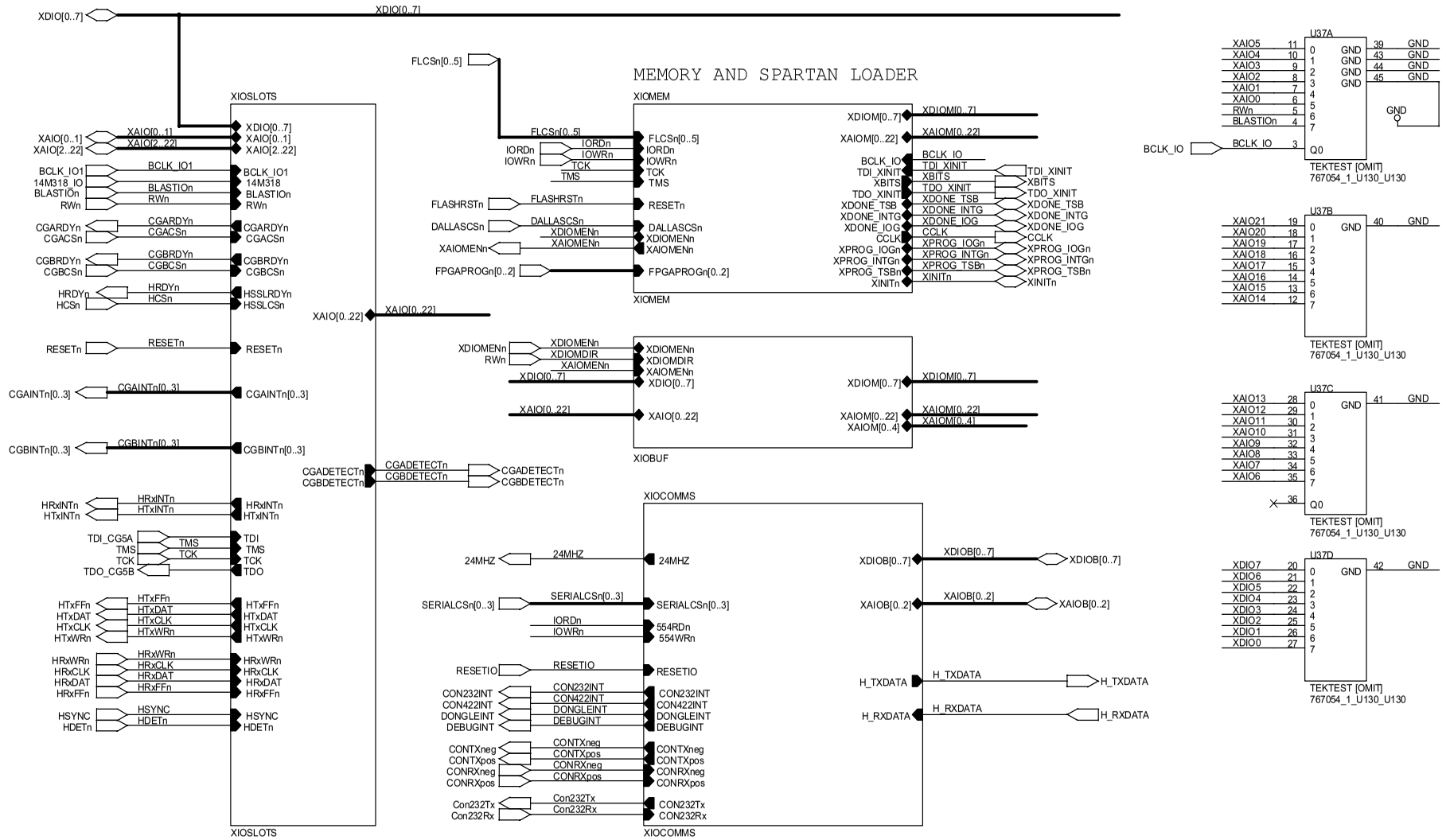

AMEM[4..31]
AMEM[2..3]
U104
DMEM[0..31]
AD[0..31]
CBEn[0..3]
VCC
R282 10K SM/R_0603 PullUp
R283 10K SM/R_0603 PullUp
R284 10K SM/R_0603 PullUp
R285 10K SM/R_0603 PullUp
R286 10K SM/R_0603 PullUp
LPAR0
LPAR1
LPAR3
LPAR2
BTERMn
BWEn[0..3]
EPCREQn
LBURSTn
LRWn
LREADYn
BTERMn
LBREQn
LBGNTn
LINTn
BCLK
LRSTn
R43 AD20
R220R 0603_R350_R350
PERRn
SERRn
REQn
GNTn
INTD
INTC
INTB
INTA
PCICLK
PRST
R156 10k PullUp
R152 10k PullUp
R157 220R
EN5V
960/29030
SDA
SCI_LPERR
RDIR
INIT_FROM_CPU
GND= 5V_PCI_bus
GND= PRST out
HI = LRST out
V360EPC_50
QFP160_U60_U60
PX_PCI_I/F
Ardinagh
V3CorpV360EPC_50RevA0
Title
PYPCI.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 43 of 45


XIO
MEMORY AND SPARTAN LOADER
XIO.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: aic
Revision: 4
Sheet: 9 of 45
Date: Friday, May 05, 2000
XIOMEM
XIOBUF
XIOCOMMS
XIOSLOTS
TEKTEST [OMIT]
767054_1_U130_U130
H_TXDATA
H_RXDATA
24MHZ
RESETIO
CON232INT
CON422INT
DONGLEINT
DEBUGINT
CONTXneg
CONTXpos
CONRXneg
CONRXpos
Con232Tx
Con232Rx
554RDn
554WRn
SERIALCSn[0..3]
BCLK_IO
XDIO[0..7]
XAIO[0..22]
FLCSn[0..5]
IORDn
IOWRn
TCK
TMS
TDI_XINIT
XBITS
TDO_XINIT
XDONE_TSB
XDONE_INTG
XDONE_IOG
CCLK
XPROG_IOGn
XPROG_INTGn
XPROG_TSBn
XINITn
FLASHRSTn
DALLASCSn
XDIOMENn
XAIOMENn
FPGAPROGn[0..2]
XDIOMDIR
RWn
CGADETECTn
CGBDETECTn
XDIOB[0..7]
XAIOB[0..2]
XDIOM[0..7]
XAIOM[0..22]
XAIOM[0..4]
XDIO[0..7]
XAIO[0..22]
BCLK_IO1
14M318_IO
BLASTIOn
RWn
CGARDYn
CGACSn
CGBRDYn
CGBCSn
HRDYn
HCSn
HSSLRDYn
HSSLCSn
RESETn
CGAINTn[0..3]
CGBINTn[0..3]
HRxINTn
HTxINTn
TDI
TMS
TCK
TDO
HTxFFn
HTxDAT
HTxCLK
HTxWRn
HRxWRn
HRxCLK
HRxDAT
HRxFFn
HSYNC
HDETn
U37A
U37B
U37C
U37D
GND
XAIO6
XAIO4
XAIO3
XAIO2
XAIO1
XAIO0
RWn
BLASTIOn
BCLK_IO
XAIO21
XAIO20
XAIO19
XAIO18
XAIO17
XAIO16
XAIO15
XAIO14
XAIO13
XAIO12
XAIO11
XAIO10
XAIO9
XAIO8
XAIO7
XAIO6
XDIO7
XDIO6
XDIO5
XDIO4
XDIO3
XDIO2
XDIO1
XDIO0

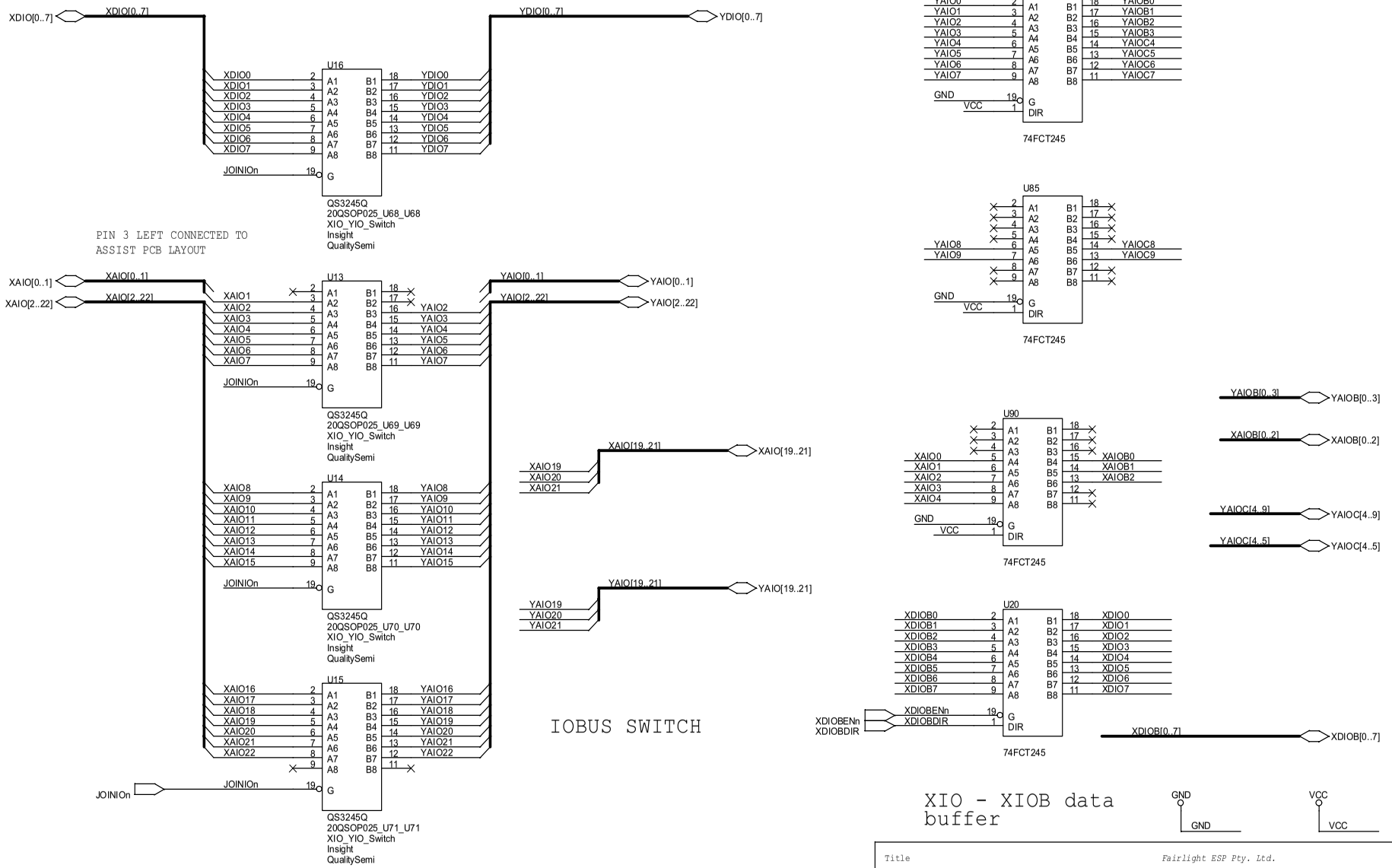


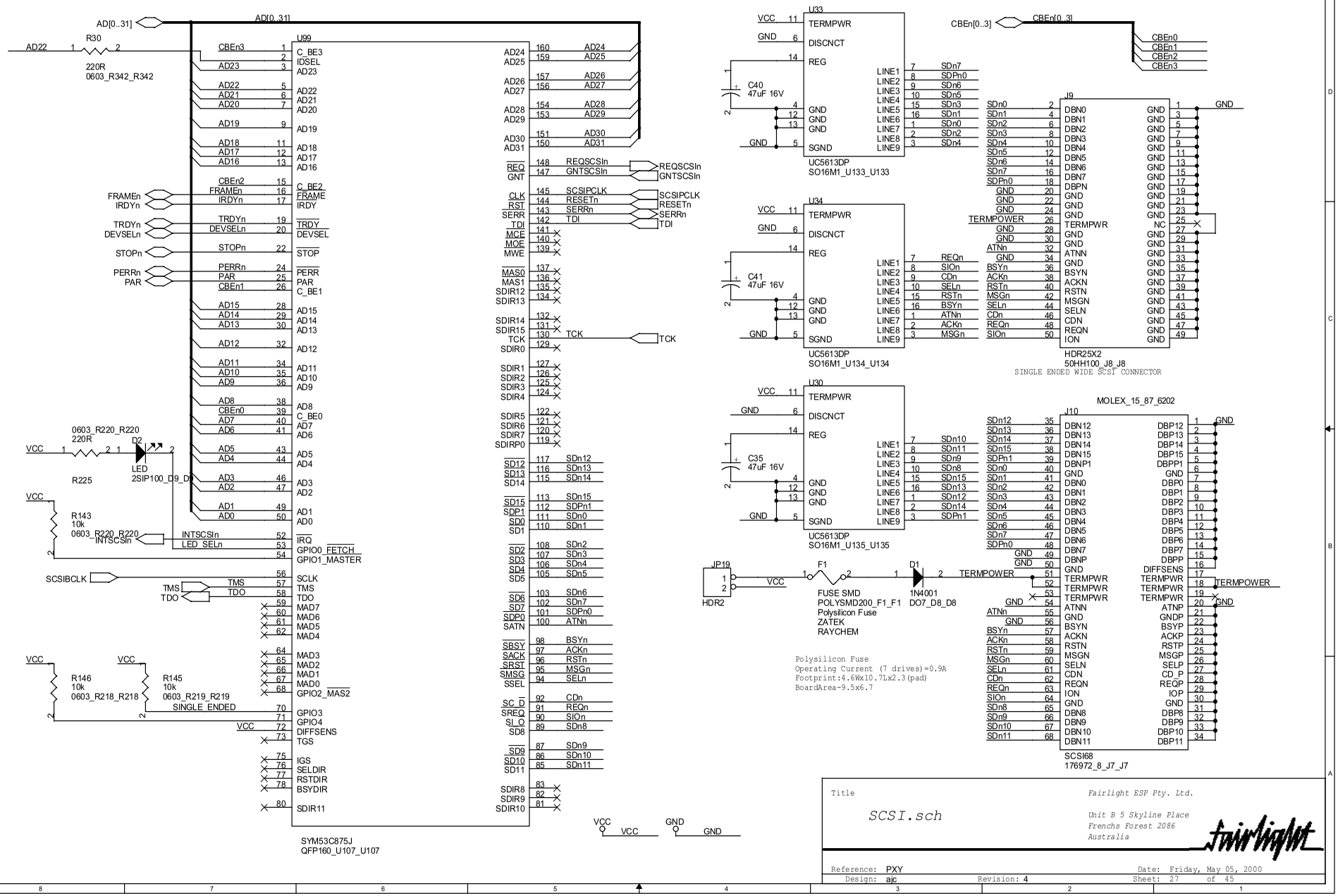
Title	IOCON.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	PXY
Design:	ajc
Revision:	4
Date:	Friday, May 05, 2000
Sheet:	16 of 45

XIO

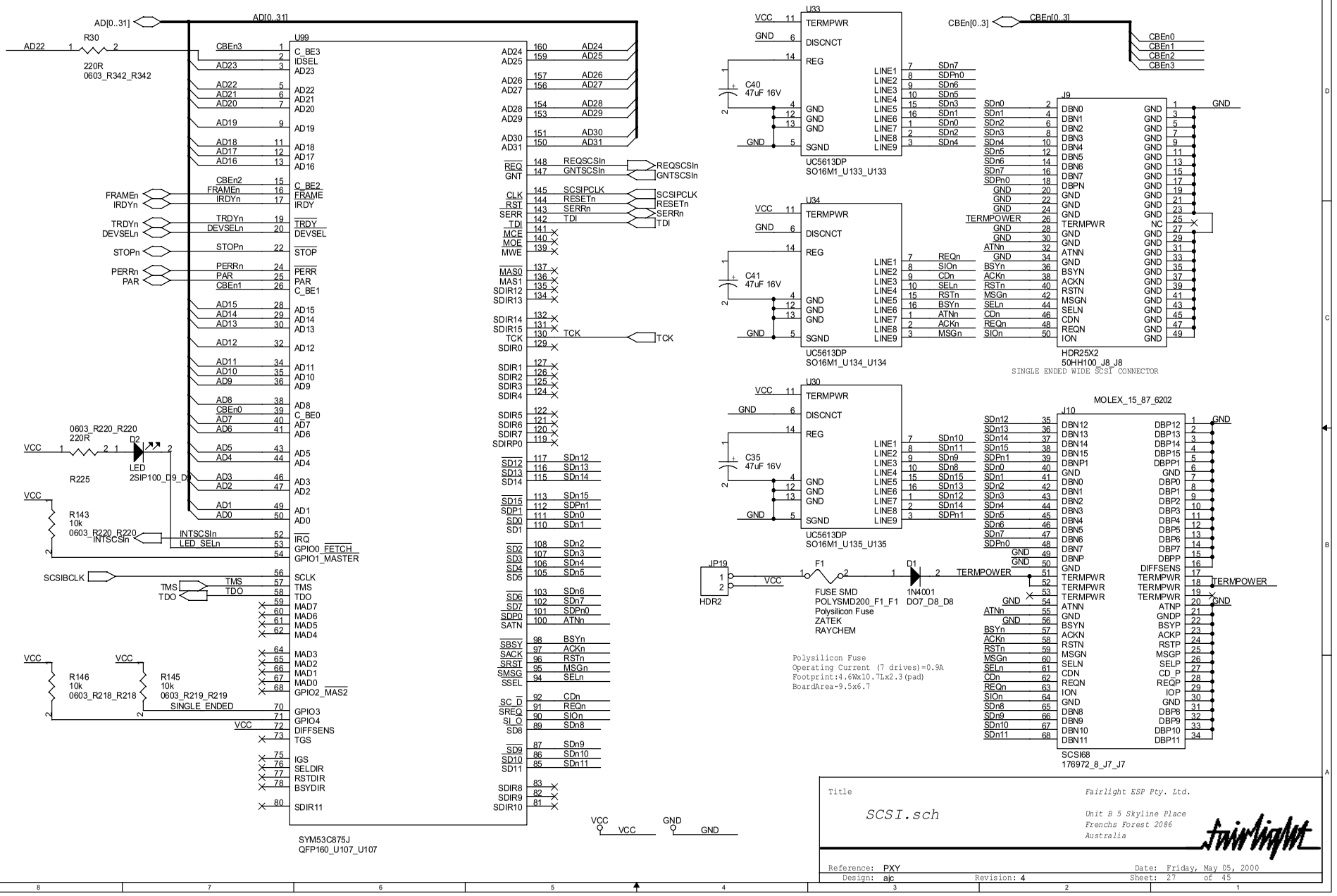


Title	XIO.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 9 of 45

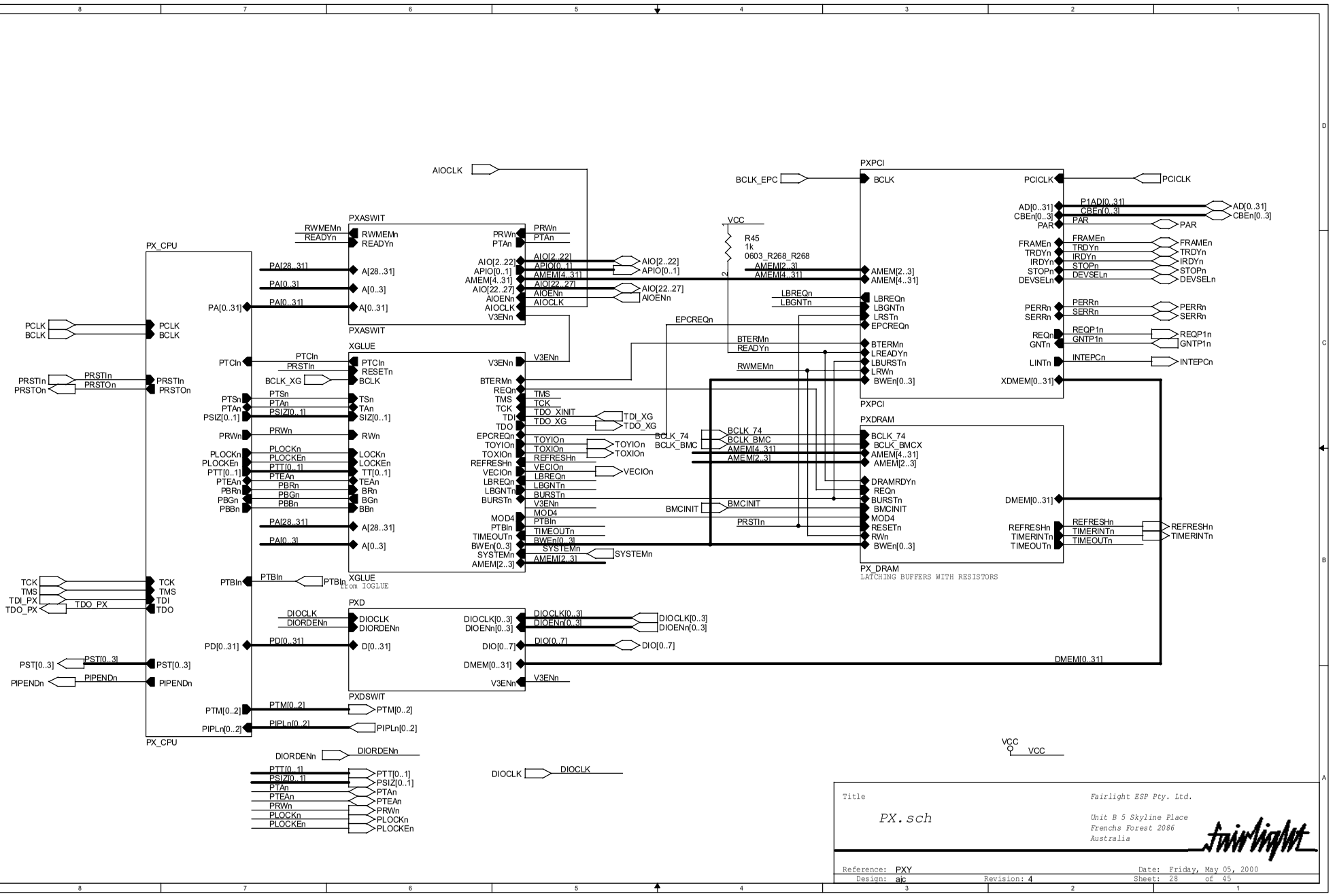

XDIO[0..7]
XDIO[0..7]
YDIO[0..7]
YDIO[0..7]
U16
XDIO0 2
XDIO1 3
XDIO2 4
XDIO3 5
XDIO4 6
XDIO5 7
XDIO6 8
XDIO7 9
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
18 YDIO0
17 YDIO1
16 YDIO2
15 YDIO3
14 YDIO4
13 YDIO5
12 YDIO6
11 YDIO7
JOINIOn 19
G
QS3245Q
20QSOP025_U68_U68
XIO_YIO_Switch
Insight
QualitySemi
PIN 3 LEFT CONNECTED TO
ASSIST PCB LAYOUT
XAIO[0..1]
XAIO[2..22]
XAIO[0..1]
XAIO[2..22]
YAIO[0..1]
YAIO[2..22]
YAIO[0..1]
YAIO[2..22]
U13
XAIO1 3
XAIO2 4
XAIO3 5
XAIO4 6
XAIO5 7
XAIO6 8
XAIO7 9
YAIO2 16
YAIO3 15
YAIO4 14
YAIO5 13
YAIO6 12
YAIO7 11
JOINIOn 19
G
QS3245Q
20QSOP025_U69_U69
XIO_YIO_Switch
Insight
QualitySemi
U14
XAIO8 2
XAIO9 3
XAIO10 4
XAIO11 5
XAIO12 6
XAIO13 7
XAIO14 8
XAIO15 9
YAIO8 18
YAIO9 17
YAIO10 16
YAIO11 15
YAIO12 14
YAIO13 13
YAIO14 12
YAIO15 11
JOINIOn 19
G
QS3245Q
20QSOP025_U70_U70
XIO_YIO_Switch
Insight
QualitySemi
U15
XAIO16 2
XAIO17 3
XAIO18 4
XAIO19 5
XAIO20 6
XAIO21 7
XAIO22 8
YAIO16 18
YAIO17 17
YAIO18 16
YAIO19 15
YAIO20 14
YAIO21 13
YAIO22 12
JOINIOn
JOINIOn 19
G
QS3245Q
20QSOP025_U71_U71
XIO_YIO_Switch
Insight
QualitySemi
XAIO[19..21]
XAIO19
XAIO20
XAIO21
XAIO[19..21]
YAIO[19..21]
YAIO19
YAIO20
YAIO21
YAIO[19..21]
IOBUS SWITCH
U12
YAIO0 2
YAIO1 3
YAIO2 4
YAIO3 5
YAIO4 6
YAIO5 7
YAIO6 8
YAIO7 9
A1 A2 A3 A4 A5 A6 A7 A8
B1 B2 B3 B4 B5 B6 B7 B8
18 YAIOB0
17 YAIOB1
16 YAIOB2
15 YAIOB3
14 YAIOC4
13 YAIOC5
12 YAIOC6
11 YAIOC7
GND 19
VCC 1
G
DIR
74FCT245
U85
YAIO8 6
YAIO9 7
14 YAIOC8
13 YAIOC9
GND 19
VCC 1
74FCT245
U90
XAIO0 5
XAIO1 6
XAIO2 7
XAIO3 8
XAIO4 9
15 XAIOB0
14 XAIOB1
13 XAIOB2
GND 19
VCC 1
74FCT245
YAIOB[0..3]
YAIOB[0..3]
XAIOB[0..2]
XAIOB[0..2]
YAIOC[4..9]
YAIOC[4..9]
YAIOC[4..5]
YAIOC[4..5]
U20
XDIOB0 2
XDIOB1 3
XDIOB2 4
XDIOB3 5
XDIOB4 6
XDIOB5 7
XDIOB6 8
XDIOB7 9
18 XDIO0
17 XDIO1
16 XDIO2
15 XDIO3
14 XDIO4
13 XDIO5
12 XDIO6
11 XDIO7
XDIOBENn 19
XDIOBDIR 1
XDIOBENn
XDIOBDIR
74FCT245
XDIOB[0..7]
XDIOB[0..7]
XIO - XIOB data
buffer
GND
GND
VCC
VCC
Title
IOSWITCH.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 8 of 45



Title	SCSI.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 27 of 45



Title	SCSI.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 27 of 45



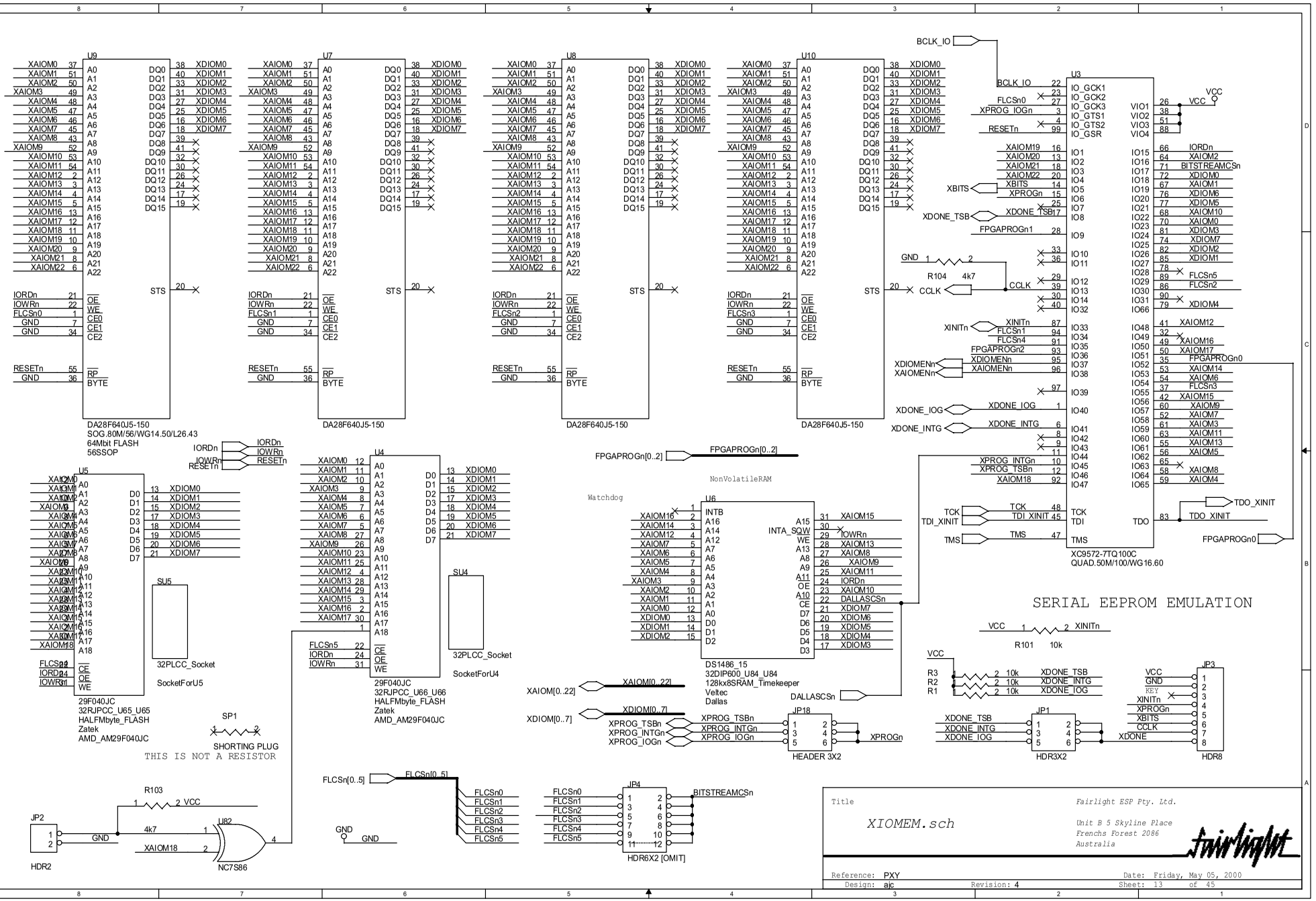
Title

PX.sch

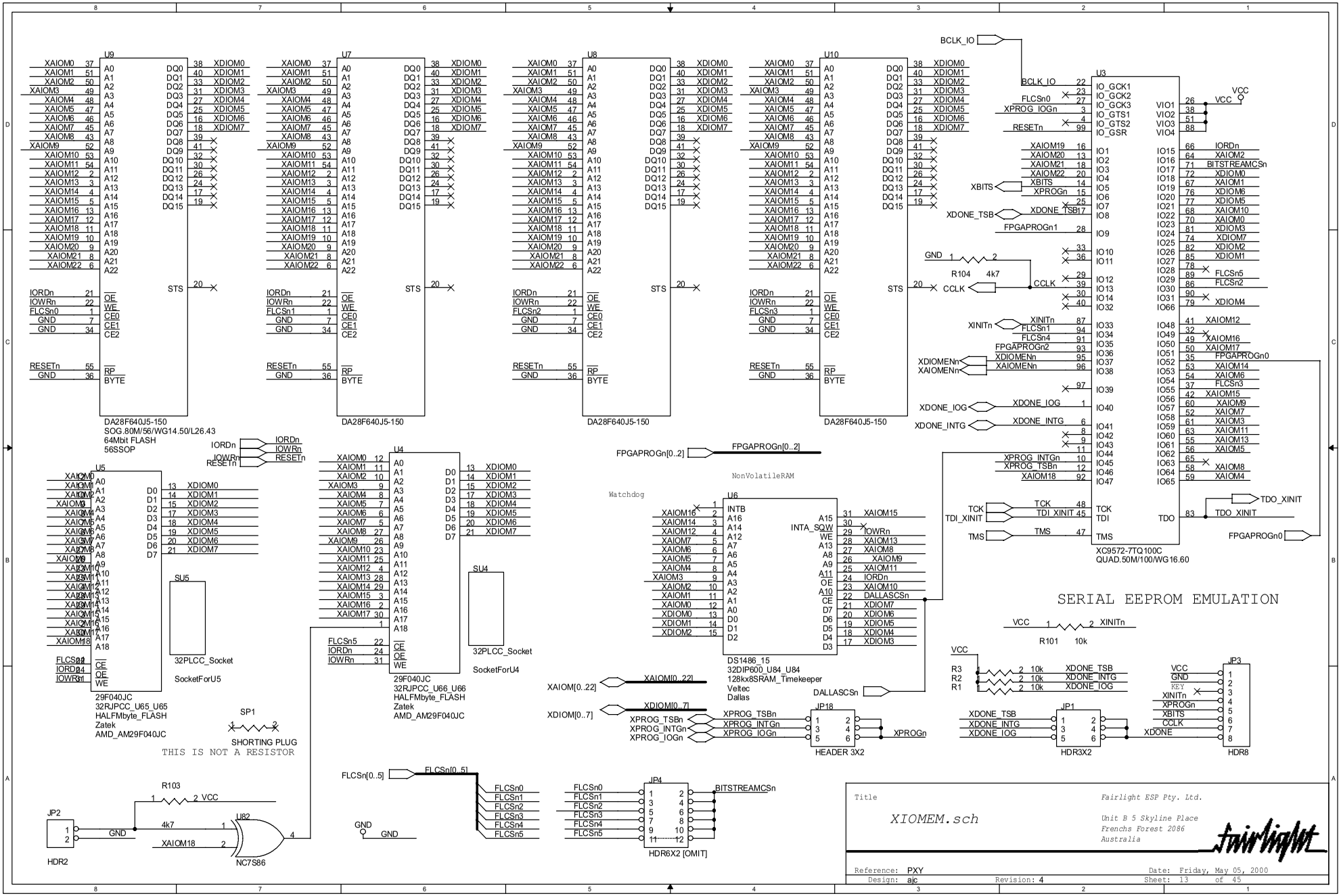
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

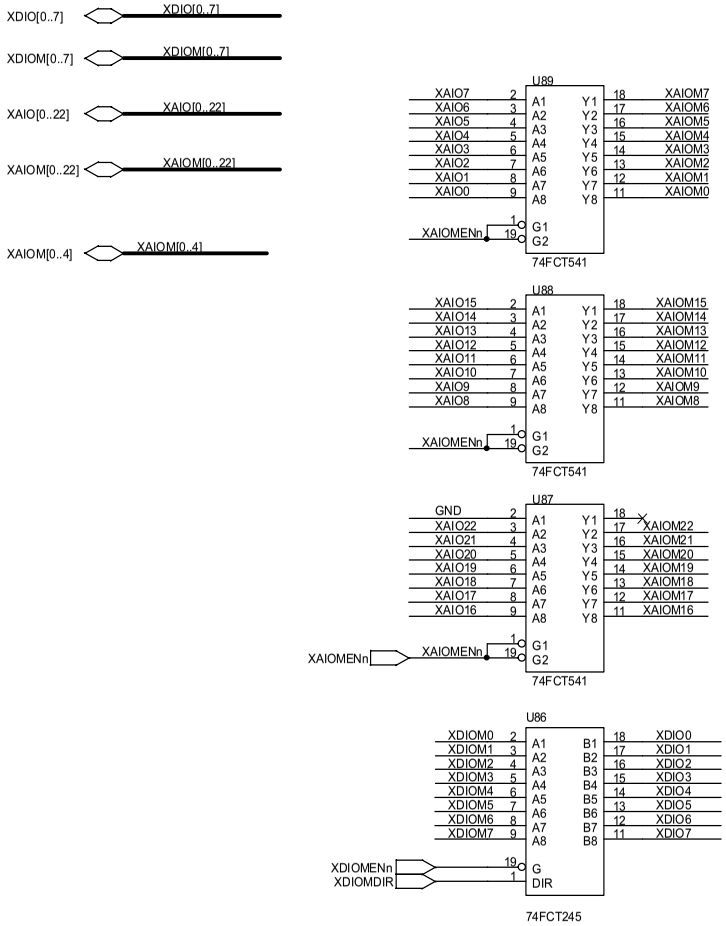
Reference: PXY
Date: Friday, May 05, 2000
Design: ajc
Revision: 4
Sheet: 28 of 45


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
PX.sch
Reference: PXY
Revision: 4
Design: ajc
Date: Friday, May 05, 2000
Sheet: 28 of 45

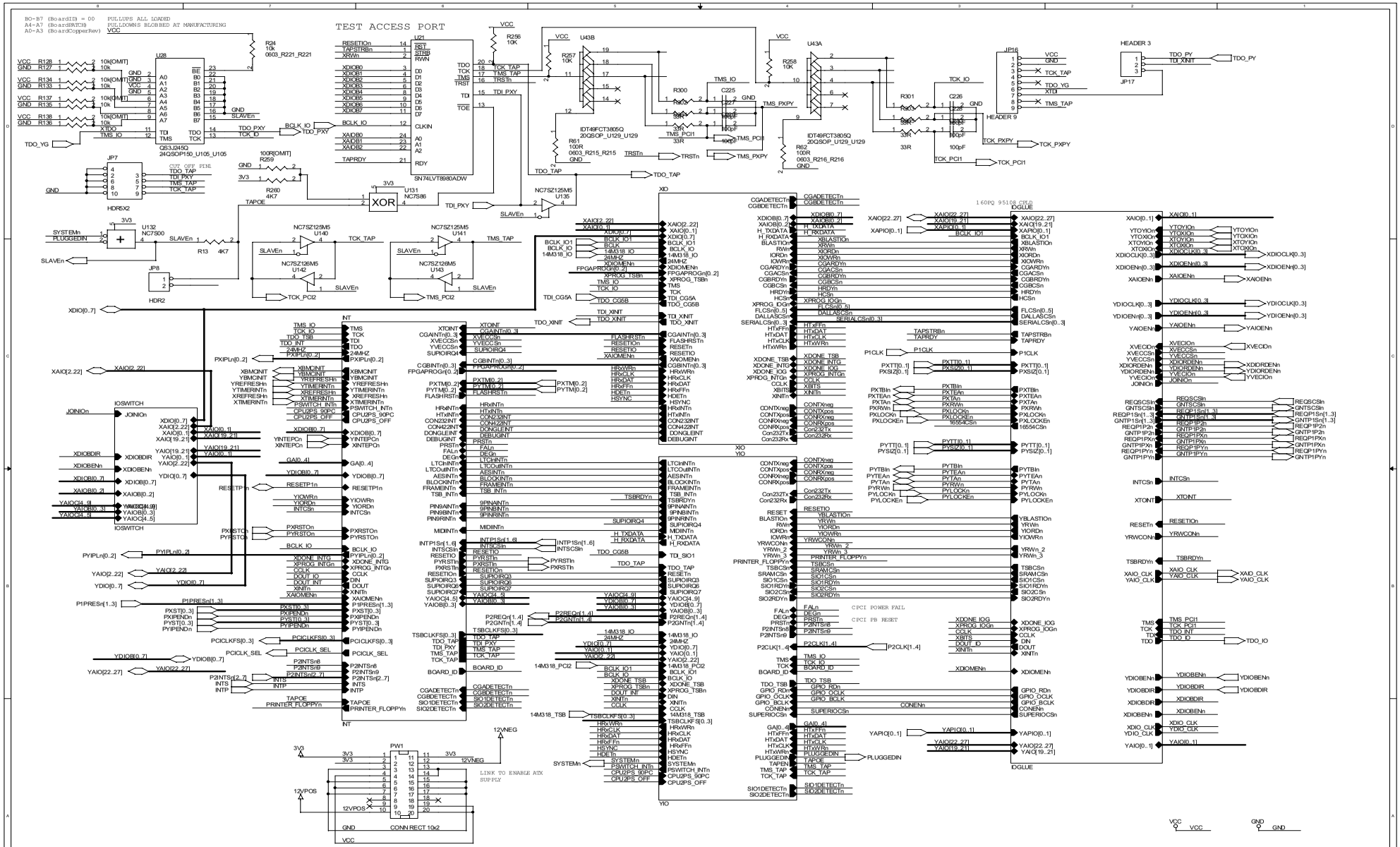

U9
U7
U8
U10
DA28F640J5-150
SOG.80M/56/WG14.50/L26.43
64Mbit FLASH
56SSOP
BCLK_IO
U3
XC9572-7TQ100C
QUAD.50M/100/WG16.60
SERIAL EEPROM EMULATION
U5
U4
U6
29F040JC
32RJPCC_U65_U65
HALFMbyte_FLASH
Zatek
AMD_AM29F040JC
32PLCC_Socket
SocketForU5
SocketForU4
SHORTING PLUG
THIS IS NOT A RESISTOR
NonVolatileRAM
DS1486_15
32DIP600_U84_U84
128kx8SRAM_Timekeeper
Veltec
Dallas
HEADER 3X2
HDR3X2
HDR8
HDR2
NC7S86
HDR6X2 [OMIT]
R101 10k
R104 4k7
R103 4k7
Title
XIOMEM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 13 of 45


PX.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Date: Friday, May 05, 2000
Sheet: 28 of 45
Reference: PXY
Design: abc
Revision: 4
PXPCI
PXDRAM
PX_DRAM
PXASWIT
XGLUE
PXD
PXDSWIT
PX_CPU
LATCHING BUFFERS WITH RESISTORS
R45
1K
0603_R268_R268
VCC
BCLK_EPC
AIOCLK
PCICLK
BCLK
AD[0..31]
CBEn[0..3]
PAR
FRAMEn
TRDYn
IRDYn
STOPn
DEVSELn
PERRn
SERRn
REQP1n
GNTP1n
INTEPCn
LINTn
XDMEM[0..31]
DMEM[0..31]
REFRESHn
TIMERINTn
TIMEOUTn
AMEM[2..3]
AMEM[4..31]
LBREQn
LBGNTn
LRSTn
EPCREQn
BTERMn
LREADYn
LBURSTn
LRWn
BWEn[0..3]
BCLK_74
BCLK_BMC
BCLK_BMCX
DRAMRDYn
REQn
BURSTn
BMCINIT
MOD4
RESETn
RWn
PRSTIn
AIO[2..22]
APIO[0..1]
AIO[22..27]
AIOENn
AIOCLK
V3ENn
SYSTEMn
TDI_XG
TDO_XG
TOYIOn
TOXIOn
VECIOn
DIOCLK[0..3]
DIOENn[0..3]
DIO[0..7]
PRWn
PTAn
BTERMn
REQn
TMS
TCK
TDO_XINIT
EPCREQn
TDI
REFRESHn
LBRESETn
PTBIn
TIMEOUTn
BWEn[0..3]
SYSTEMn
AMEM[2..3]
RWMEMn
READYn
A[28..31]
A[0..3]
PA[28..31]
PA[0..31]
PTCIn
RESETn
BCLK_XG
PTSn
PTAn
SIZ[0..1]
PRWn
LOCKn
LOCKENn
TT[0..1]
TEAn
BRn
BGn
BBn
PTBIn
DIOCLK
DIORDENn
D[0..31]
PD[0..31]
PTM[0..2]
PIPLn[0..2]
DIORDENn
PTT[0..1]
PSIZ[0..1]
PTAn
PTEAn
PRWn
PLOCKn
PLOCKENn
PCLK
BCLK
PRSTIn
PRSTOn
TCK
TMS
TDI
TDO
TDI_PX
TDO_PX
PST[0..3]
PIPENDn


U9
U7
U8
U10
DA28F640J5-150
SOG.80M/56/WG14.50/L26.43
64Mbit FLASH
56SSOP
U5
29F040JC
32RJPCC_U65_U65
HALFMbyte_FLASH
Zatek
AMD_AM29F040JC
32PLCC_Socket
SocketForU5
SU5
SP1
SHORTING PLUG
THIS IS NOT A RESISTOR
U4
29F040JC
32RJPCC_U66_U66
HALFMbyte_FLASH
Zatek
AMD_AM29F040JC
32PLCC_Socket
SocketForU4
SU4
U3
XC9572-7TQ100C
QUAD.50M/100/WG16.60
U6
DS1486_15
32DIP600_U84_U84
128kx8SRAM_Timekeeper
Veltec
Dallas
NonVolatileRAM
Watchdog
SERIAL EEPROM EMULATION
R101 10k
R104 4k7
R103 4k7
JP2
HDR2
U82
NC7S86
JP4
HDR6X2 [OMIT]
JP18
HEADER 3X2
JP1
HDR3X2
JP3
HDR8
BCLK_IO
VCC
GND
CCLK
XINITn
XBITS
XDONE_TSB
XDONE_IOG
XDONE_INTG
TDI_XINIT
TDO_XINIT
FPGAPROGn0
XPROG_TSBn
XPROG_INTGn
XPROG_IOGn
XPROGn
XDONE
DALLASCSn
FPGAPROGn[0..2]
XAIOM[0..22]
XDIOM[0..7]
FLCSn[0..5]
BITSTREAMCSn
Title
XIOMEM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 13 of 45



Title	XIOBUF.sch
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 10 of 45


TEST ACCESS PORT
IO.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ABC
Revision: 4
Date: Friday, May 05, 2000
Sheet 5 of 45
DRAFT
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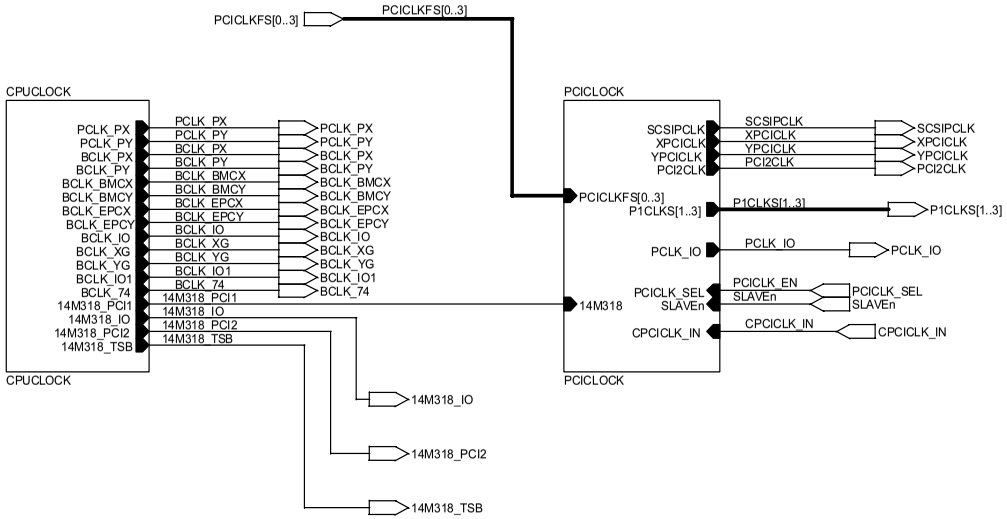
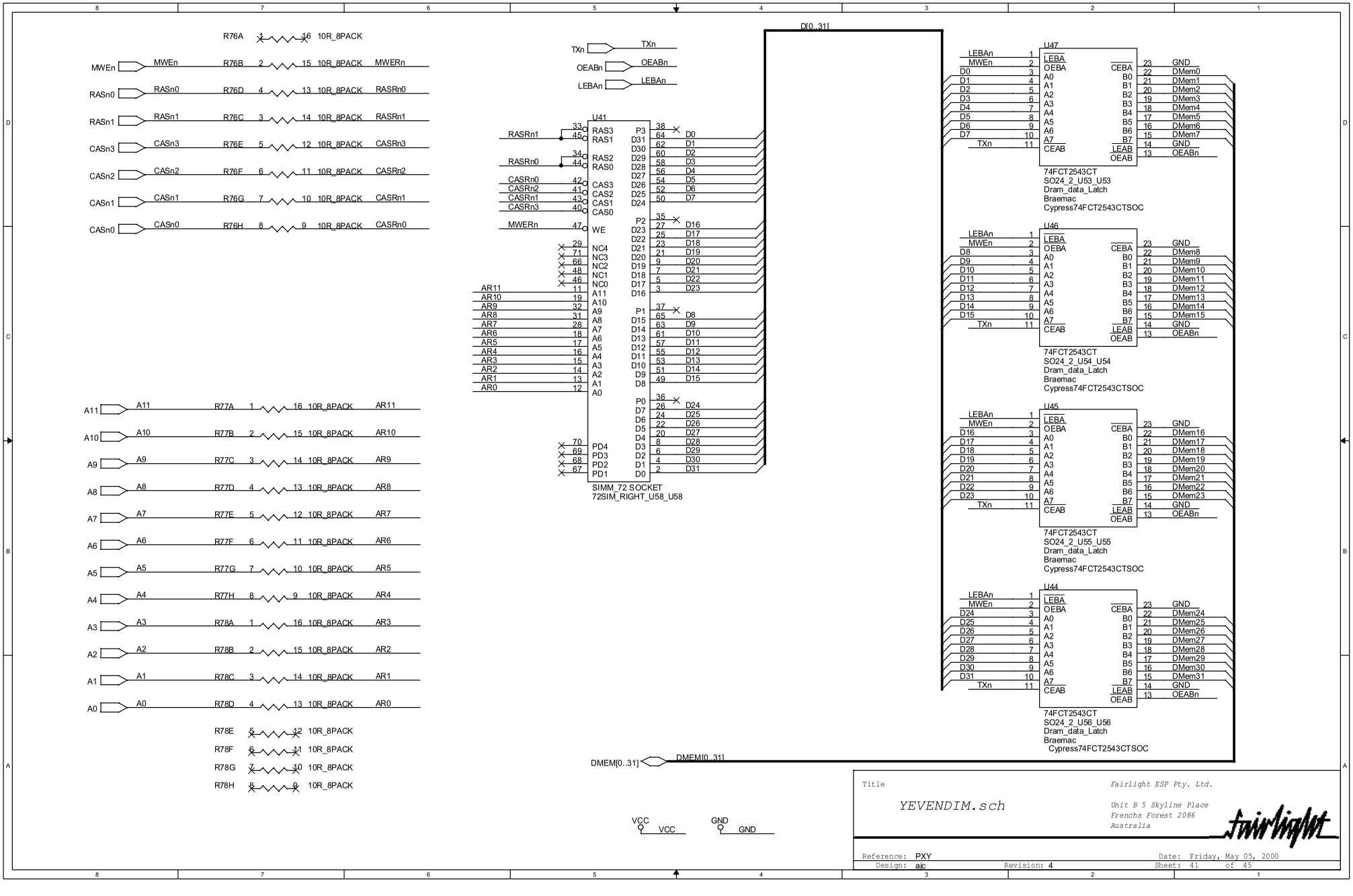
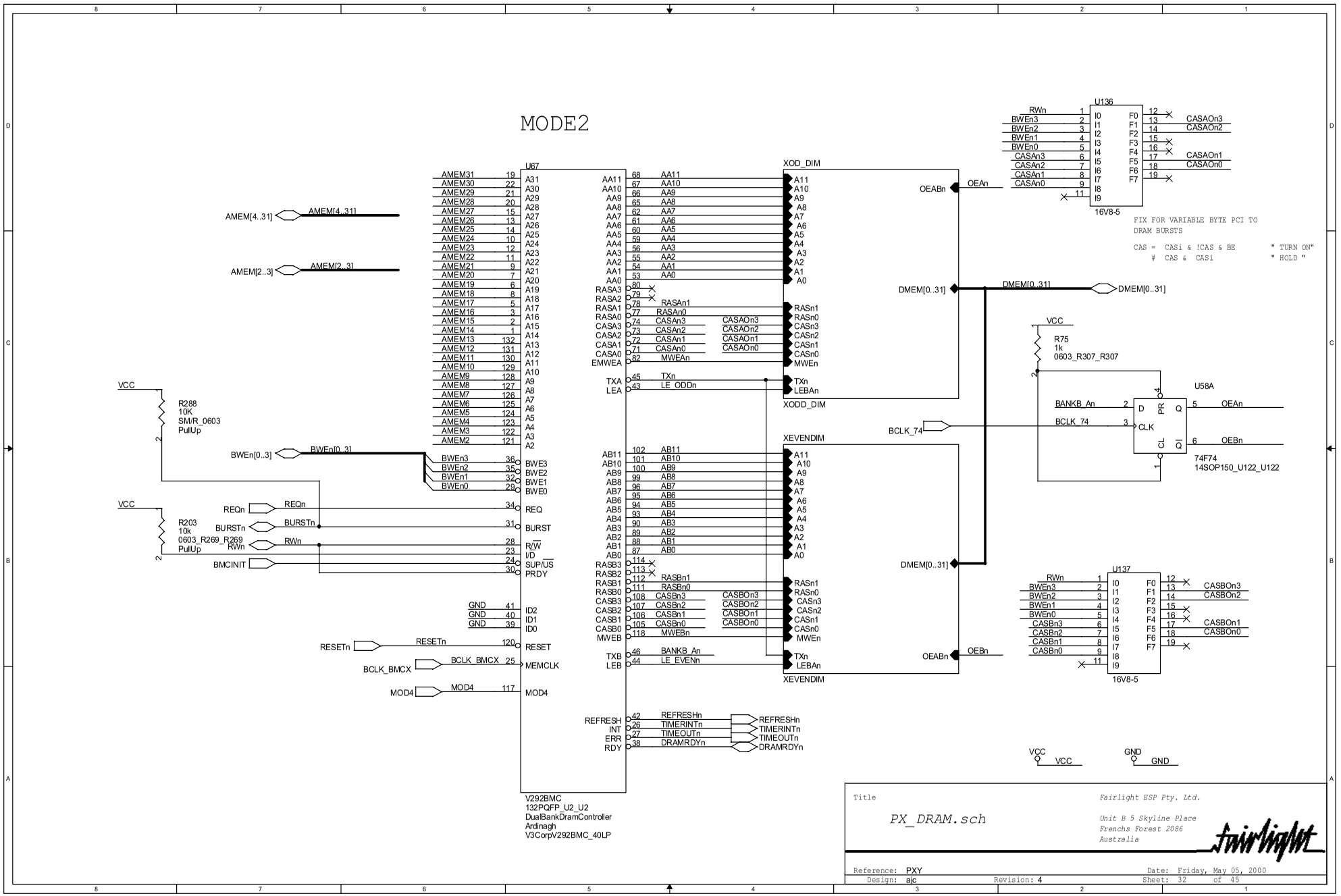
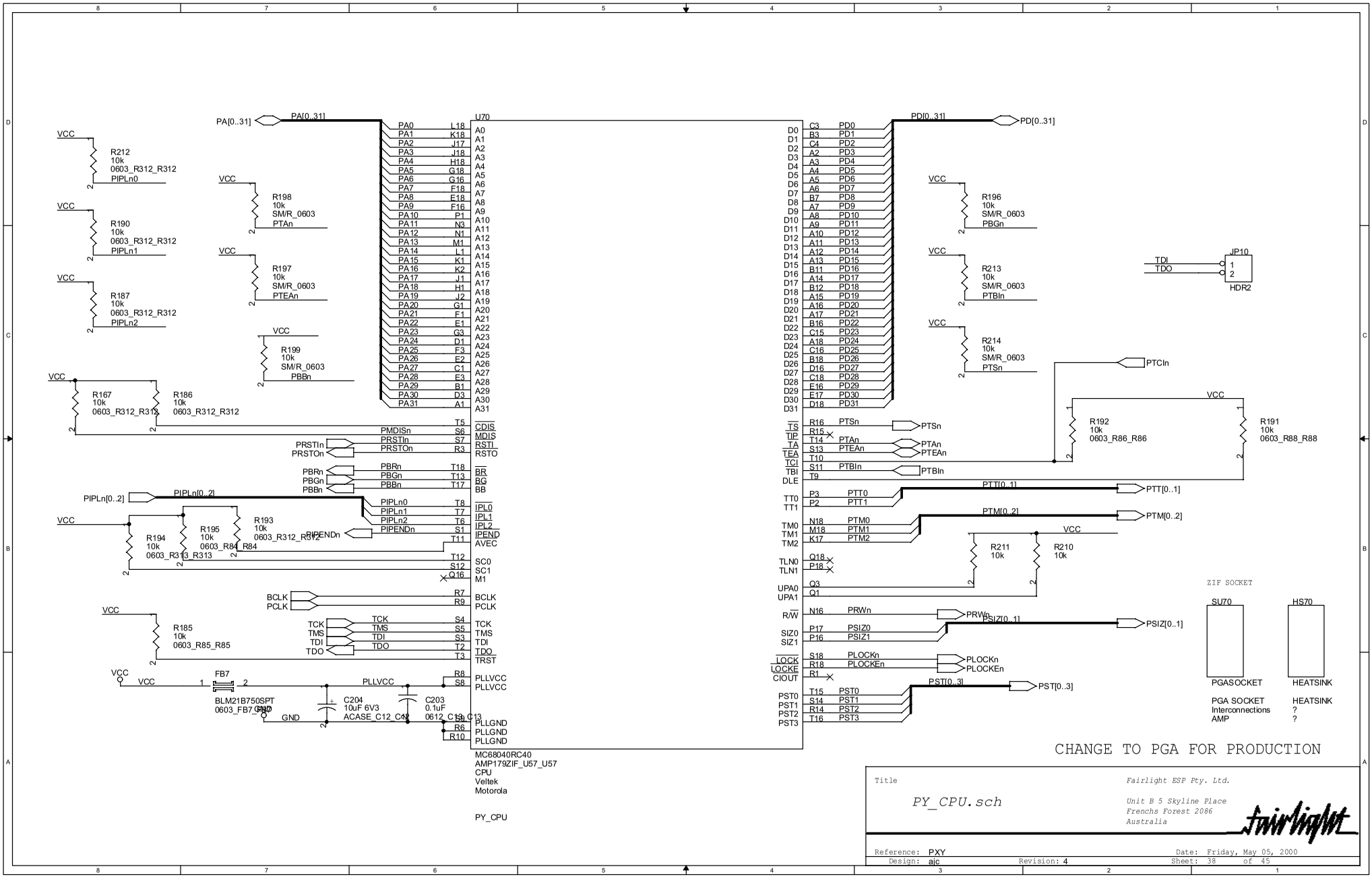
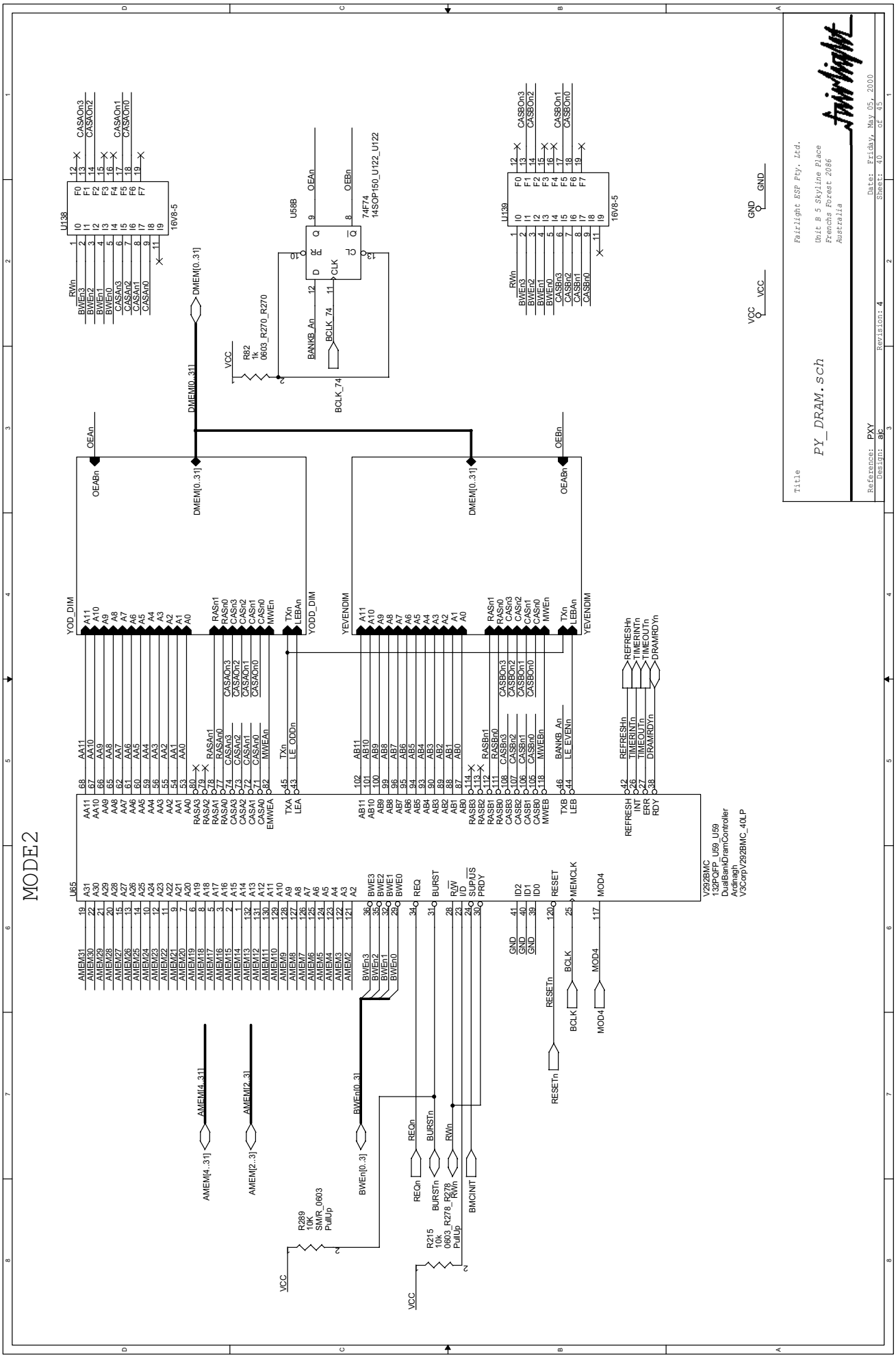


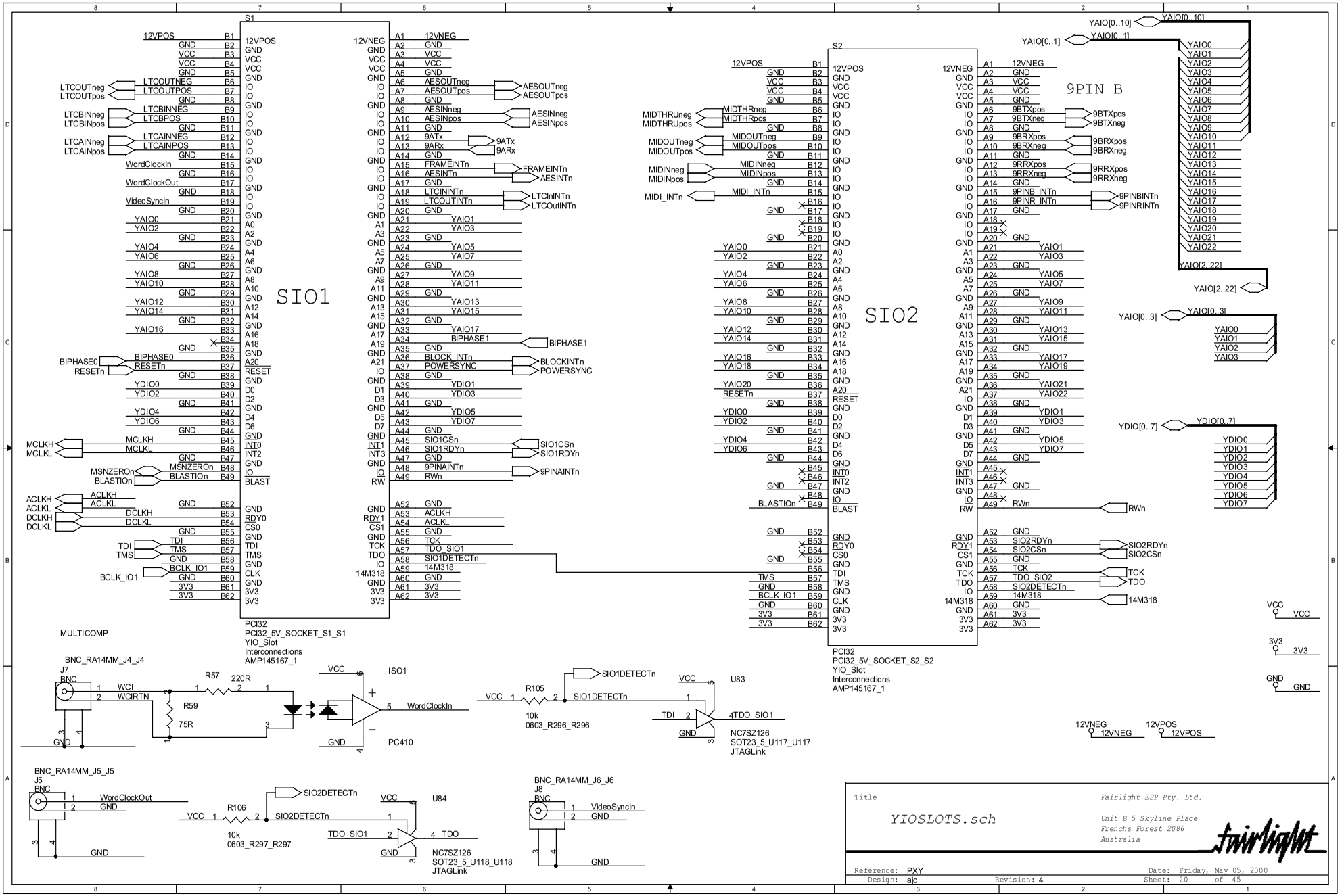
Title	CLOCKS.sch	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia	
Reference: PXY			Date: Friday, May 05, 2000
Design: ajc	Revision: 4		Sheet: 2 of 45

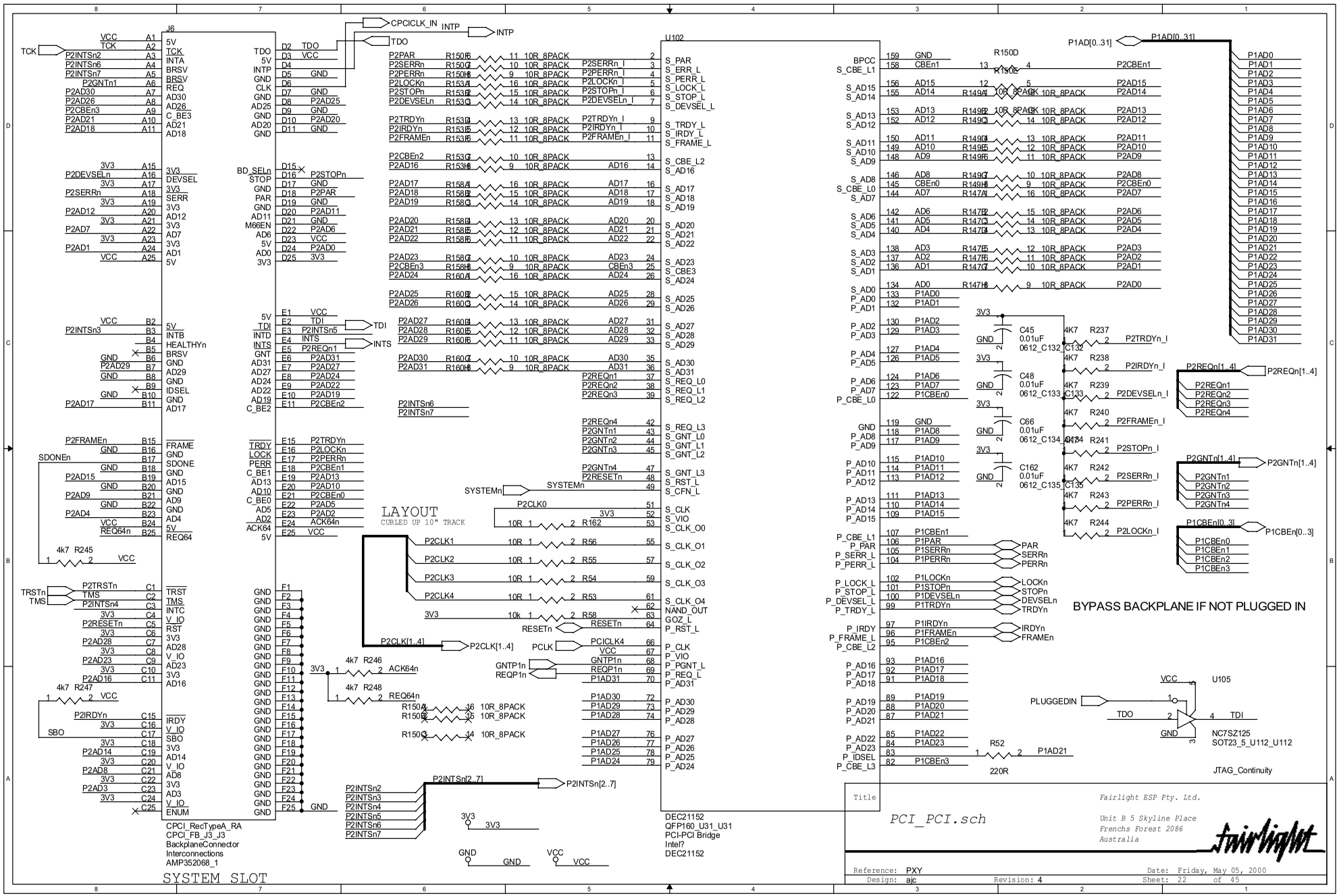

R76A 1 16 10R_8PACK
MWEn MWEn R76B 2 15 10R_8PACK MWERn
RASn0 RASn0 R76D 4 13 10R_8PACK RASRn0
RASn1 RASn1 R76C 3 14 10R_8PACK RASRn1
CASn3 CASn3 R76E 5 12 10R_8PACK CASRn3
CASn2 CASn2 R76F 6 11 10R_8PACK CASRn2
CASn1 CASn1 R76G 7 10 10R_8PACK CASRn1
CASn0 CASn0 R76H 8 9 10R_8PACK CASRn0
A11 A11 R77A 1 16 10R_8PACK AR11
A10 A10 R77B 2 15 10R_8PACK AR10
A9 A9 R77C 3 14 10R_8PACK AR9
A8 A8 R77D 4 13 10R_8PACK AR8
A7 A7 R77E 5 12 10R_8PACK AR7
A6 A6 R77F 6 11 10R_8PACK AR6
A5 A5 R77G 7 10 10R_8PACK AR5
A4 A4 R77H 8 9 10R_8PACK AR4
A3 A3 R78A 1 16 10R_8PACK AR3
A2 A2 R78B 2 15 10R_8PACK AR2
A1 A1 R78C 3 14 10R_8PACK AR1
A0 A0 R78D 4 13 10R_8PACK AR0
R78E 5 12 10R_8PACK
R78F 6 11 10R_8PACK
R78G 7 10 10R_8PACK
R78H 8 9 10R_8PACK
TXn TXn
OEABn OEABn
LEBAn LEBAn
U41
RASRn1 RASRn0 CASRn0 CASRn2 CASRn1 CASRn3 MWERn
RAS3 RAS1 RAS2 RAS0 CAS3 CAS2 CAS1 CAS0 WE
NC4 NC3 NC2 NC1 NC0
AR11 AR10 AR9 AR8 AR7 AR6 AR5 AR4 AR3 AR2 AR1 AR0
A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
PD4 PD3 PD2 PD1
P3 P2 P1 P0
D31 D30 D29 D28 D27 D26 D25 D24 D23 D22 D21 D20 D19 D18 D17 D16 D15 D14 D13 D12 D11 D10 D9 D8 D7 D6 D5 D4 D3 D2 D1 D0
SIMM_72 SOCKET
72SIM_RIGHT_U58_U58
D[0..31]
U47
U46
U45
U44
LEBAn MWEn D0 D1 D2 D3 D4 D5 D6 D7 TXn
LEBA OEBA A0 A1 A2 A3 A4 A5 A6 A7 CEAB
CEBA B0 B1 B2 B3 B4 B5 B6 B7 LEAB OEAB
GND DMem0 DMem1 DMem2 DMem3 DMem4 DMem5 DMem6 DMem7 GND OEABn
LEBAn MWEn D8 D9 D10 D11 D12 D13 D14 D15 TXn
GND DMem8 DMem9 DMem10 DMem11 DMem12 DMem13 DMem14 DMem15 GND OEABn
LEBAn MWEn D16 D17 D18 D19 D20 D21 D22 D23 TXn
GND DMem16 DMem17 DMem18 DMem19 DMem20 DMem21 DMem22 DMem23 GND OEABn
LEBAn MWEn D24 D25 D26 D27 D28 D29 D30 D31 TXn
GND DMem24 DMem25 DMem26 DMem27 DMem28 DMem29 DMem30 DMem31 GND OEABn
74FCT2543CT
SO24_2_U53_U53
Dram_data_Latch
Braemac
Cypress74FCT2543CTSOC
74FCT2543CT
SO24_2_U54_U54
Dram_data_Latch
Braemac
Cypress74FCT2543CTSOC
74FCT2543CT
SO24_2_U55_U55
Dram_data_Latch
Braemac
Cypress74FCT2543CTSOC
74FCT2543CT
SO24_2_U56_U56
Dram_data_Latch
Braemac
Cypress74FCT2543CTSOC
DMEM[0..31]
DMEM[0..31]
VCC VCC
GND GND
Title
YEVENDIM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 41 of 45

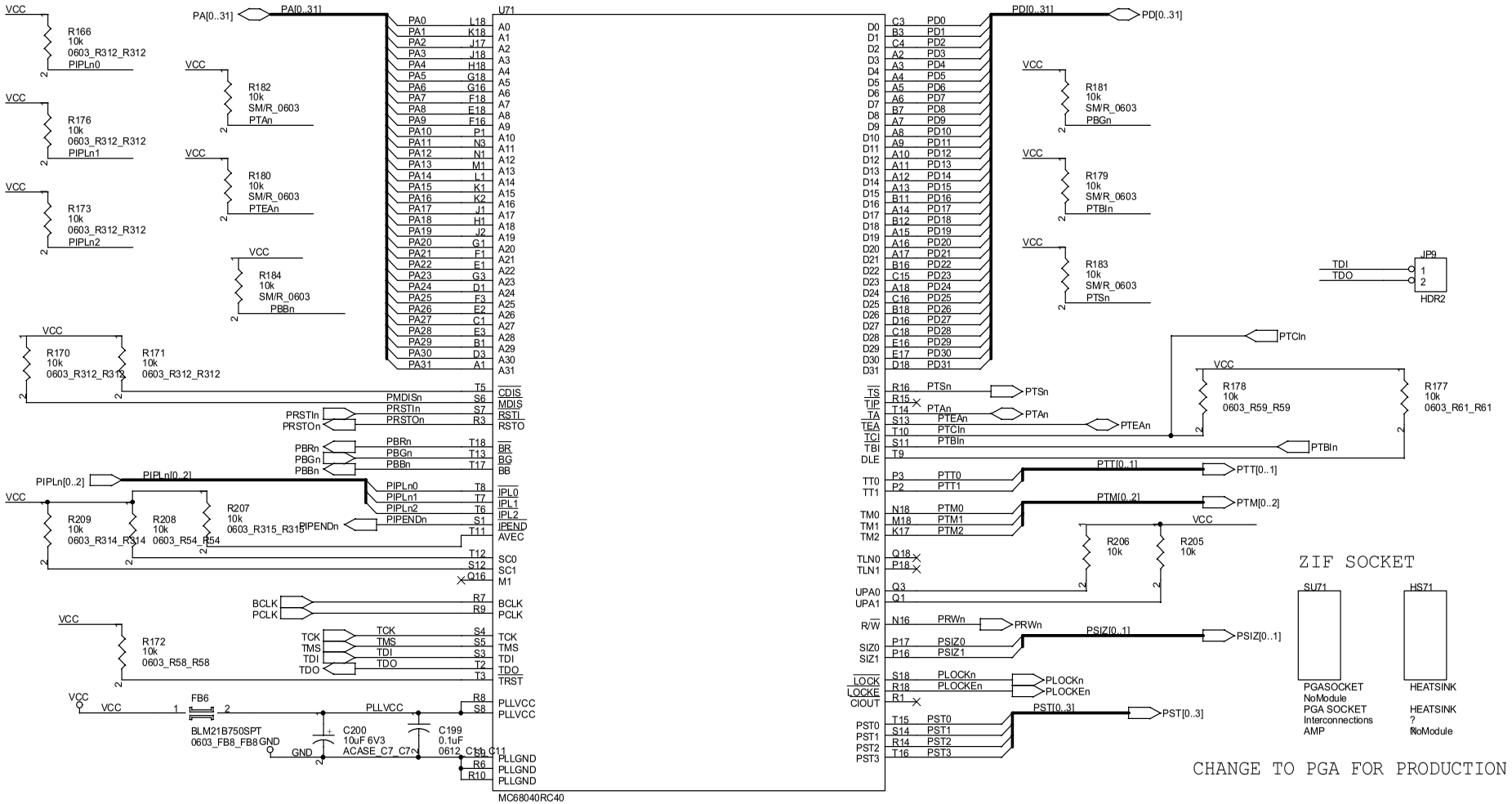

MODE2
U67
V292BMC
132PQFP_U2_U2
DualBankDramController
Ardinagh
V3CorpV292BMC_40LP
XOD_DIM
XEVENDIM
U136
16V8-5
U137
16V8-5
U58A
74F74
14SOP150_U122_U122
R288
10K
SM/R_0603
PullUp
R203
10k
0603_R269_R269
PullUp
R75
1k
0603_R307_R307
FIX FOR VARIABLE BYTE PCI TO
DRAM BURSTS
CAS = CASi & !CAS & BE " TURN ON"
# CAS & CASi " HOLD "
Title
PX_DRAM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 32 of 45


U70
MC68040RC40
AMP179ZIF_U57_U57
CPU
Veltek
Motorola
PY_CPU
PA[0..31]
PD[0..31]
R212 10k 0603_R312_R312 PIPLn0
R190 10k 0603_R312_R312 PIPLn1
R187 10k 0603_R312_R312 PIPLn2
R198 10k SM/R_0603 PTAn
R197 10k SM/R_0603 PTEAn
R199 10k SM/R_0603 PBBn
R167 10k 0603_R312_R312
R186 10k 0603_R312_R312
R196 10k SM/R_0603 PBGn
R213 10k SM/R_0603 PTBIn
R214 10k SM/R_0603 PTSn
R192 10k 0603_R86_R86
R191 10k 0603_R88_R88
R194 10k 0603_R313_R313
R195 10k 0603_R84_R84
R193 10k 0603_R312_R312
R211 10k
R210 10k
R185 10k 0603_R85_R85
FB7
BLM21B750SPT 0603_FB7_GND
C204 10uF 6V3 ACASE_C12_C42
C203 0.1uF 0612_C13_C13
JP10
HDR2
TDI
TDO
PTCIn
PTSn
PTAn
PTEAn
PTBIn
PTT[0..1]
PTM[0..2]
PSIZ[0..1]
PLOCKn
PLOCKEn
PST[0..3]
PIPLn[0..2]
PIPENDn
PBRn
PBGn
PBBn
PRSTIn
PRSTOn
PMDISn
BCLK
PCLK
TCK
TMS
TDI
TDO
PLLVCC
PLLGND
VCC
GND
ZIF SOCKET
SU70
HS70
PGASOCKET
HEATSINK
PGA SOCKET Interconnections AMP
HEATSINK ? ?
CHANGE TO PGA FOR PRODUCTION
Title
PY_CPU.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 38 of 45

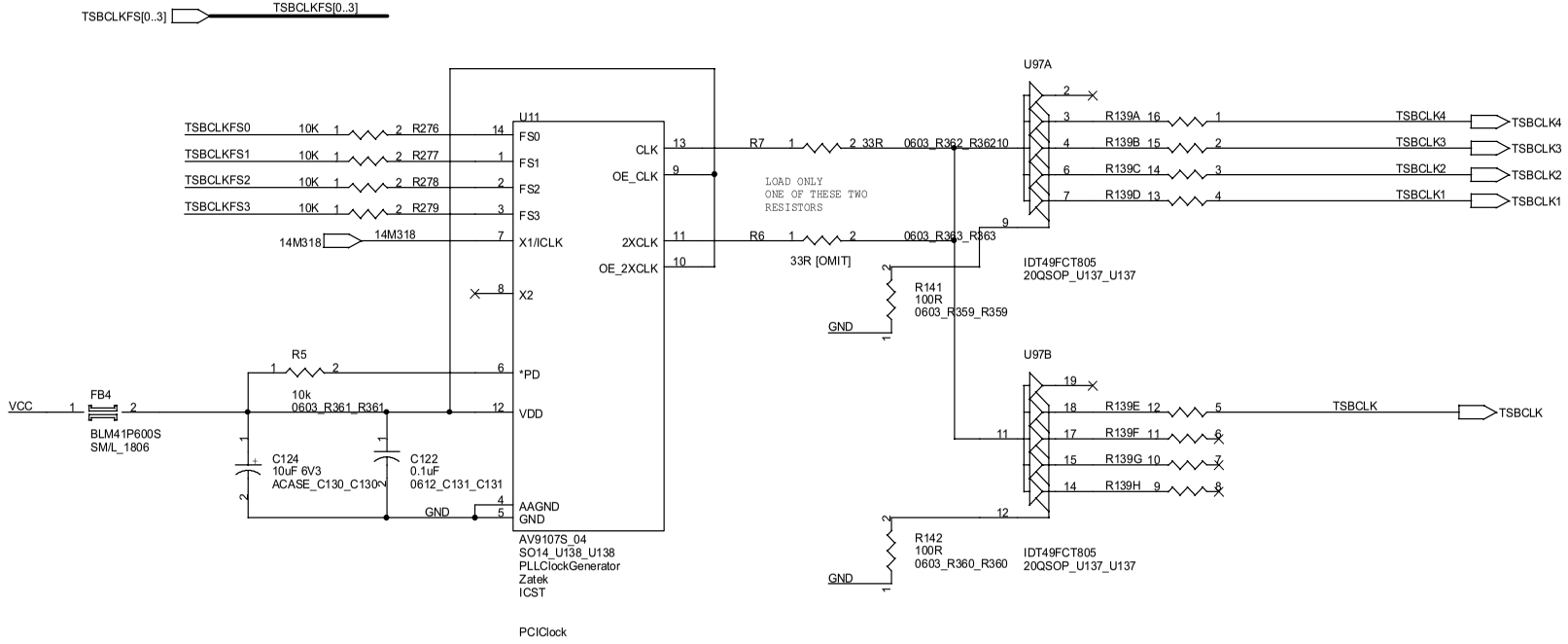

MODE2
PY_DRAM.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: alc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 40 of 45
V292BMC
132PQFP_U59_U59
DualBankDramController
Ardmagh
V3CorpV292BMC_40LP
74F74
14SOP150_U122_U122
16V8-5
R82
1k
0603_R270_R270
R289
10k
SMR_0603
PullUp
R215
10k
0603_R278_R278
PullUp
VCC
GND
DMEM[0..31]
AMEM[4..31]
AMEM[2..3]
BWEn[0..3]
REQn
BURSTn
RWn
BMCINT
RESETn
BCLK
MOD4
MEMCLK
OEAn
OEBn
OEABn
YOD_DIM
YODD_DIM
YEVENDIM
BANKB_An
BCLK_74
LE_ODDn
LE_EVENn
REFRESHn
TIMERINTn
TIMEOUTn
DRAMRDYn


SIO1
SIO2
9PIN B
PCI32
PCI32_5V_SOCKET_S1_S1
YIO_Slot
Interconnections
AMP145167_1
PCI32_5V_SOCKET_S2_S2
MULTICOMP
BNC_RA14MM_J4_J4
BNC_RA14MM_J5_J5
BNC_RA14MM_J6_J6
PC410
NC7SZ126
SOT23_5_U117_U117
JTAGLink
SOT23_5_U118_U118
10k
0603_R296_R296
0603_R297_R297
Title
YIOSLOTS.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 20 of 45


SYSTEM SLOT
CPCI_RecTypeA_RA
CPCI_FB_J3_J3
BackplaneConnector
Interconnections
AMP352068_1
LAYOUT
CURLED UP 10" TRACK
DEC21152
QFP160_U31_U31
PCI-PCI Bridge
Intel?
DEC21152
BYPASS BACKPLANE IF NOT PLUGGED IN
JTAG_Continuity
NC7SZ125
SOT23_5_U112_U112
PCI_PCI.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 22 of 45


U71
MC68040RC40
AMP179ZIF_U21_U21
CPU
Veltek
Motorola
ZIF Socket Wells Electronics 51-18043110179
PGA Socket Robinson Nugen
ZIF SOCKET
SU71
HS71
PGASOCKET
NoModule
PGA SOCKET
Interconnections
AMP
HEATSINK
HEATSINK
?
NoModule
CHANGE TO PGA FOR PRODUCTION
LAYOUT NOTE
CUT U SHAPE IN GND PLANE
TO SHIELD PLLGND PINS
FROM CIRCULATING CURRENTS
JP9
HDR2
TDI
TDO
PX_CPU.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 29 of 45

LAYOUT NOTE:



FS 3 2 1 0	MHZOUT	
0 0 0 0	80	40
0 0 0 1	66.66	33.33
0 0 1 0	50	25
0 0 1 1	40	20
0 1 0 0	100	50
0 1 0 1	33.33	16.67
0 1 1 0	32	16
0 1 1 1	25	12.5
1 0 0 0	64	32
1 0 0 1	2xIN	1N
1 0 1 0	3xIN	1.5xIN
1 0 1 1	8xIN	4xIN
1 1 0 0	.5xIN	.25xIN
1 1 0 1	.25Xin	.125Xin
1 1 1 0	120	60MHZ
1 1 1 1	130	65MHZ

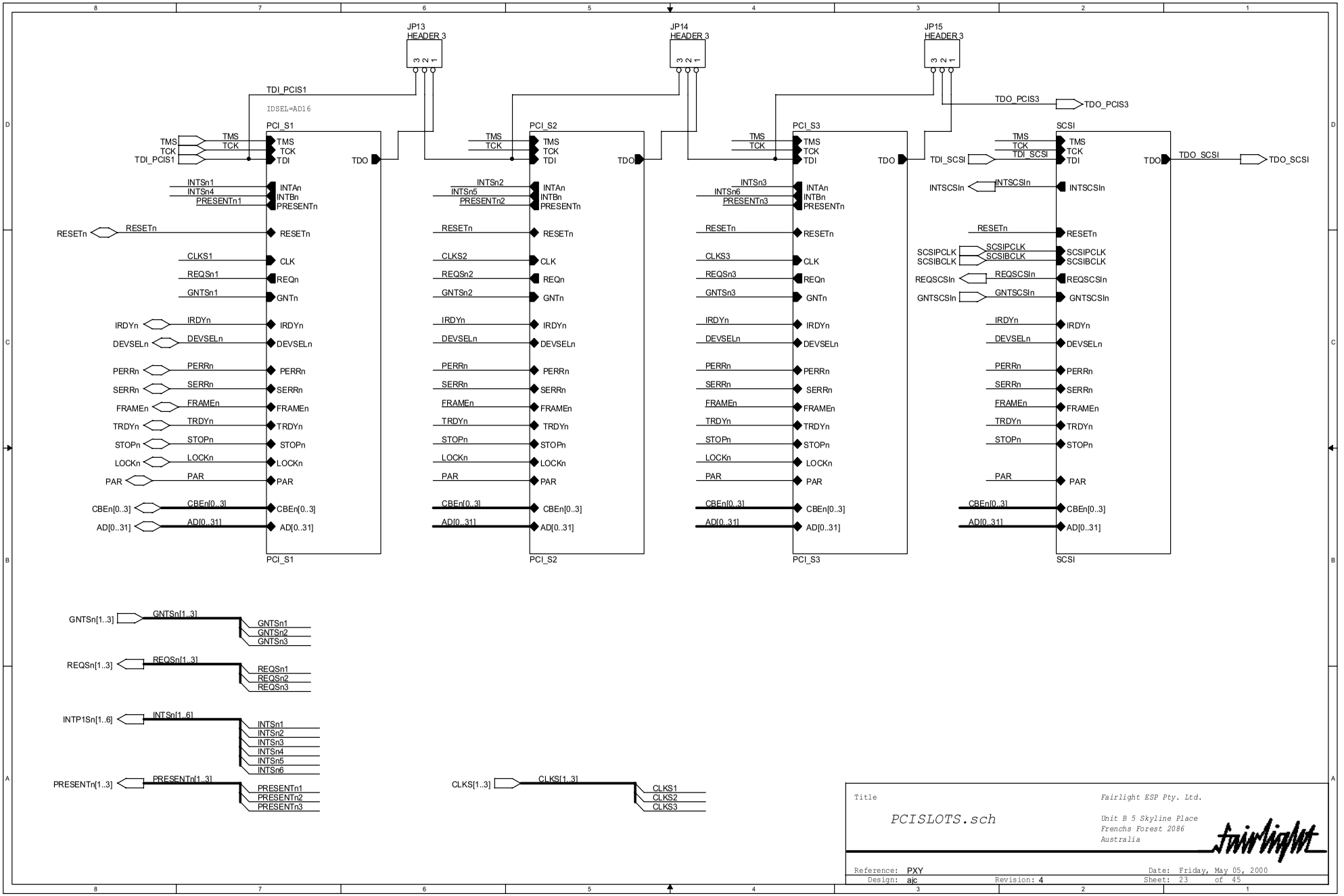
NOTE:

VALUE OF 22R RESISTORS
TO BE ADJUSTED IN DEBUG
FOR OPTIMAL SQUARENESS

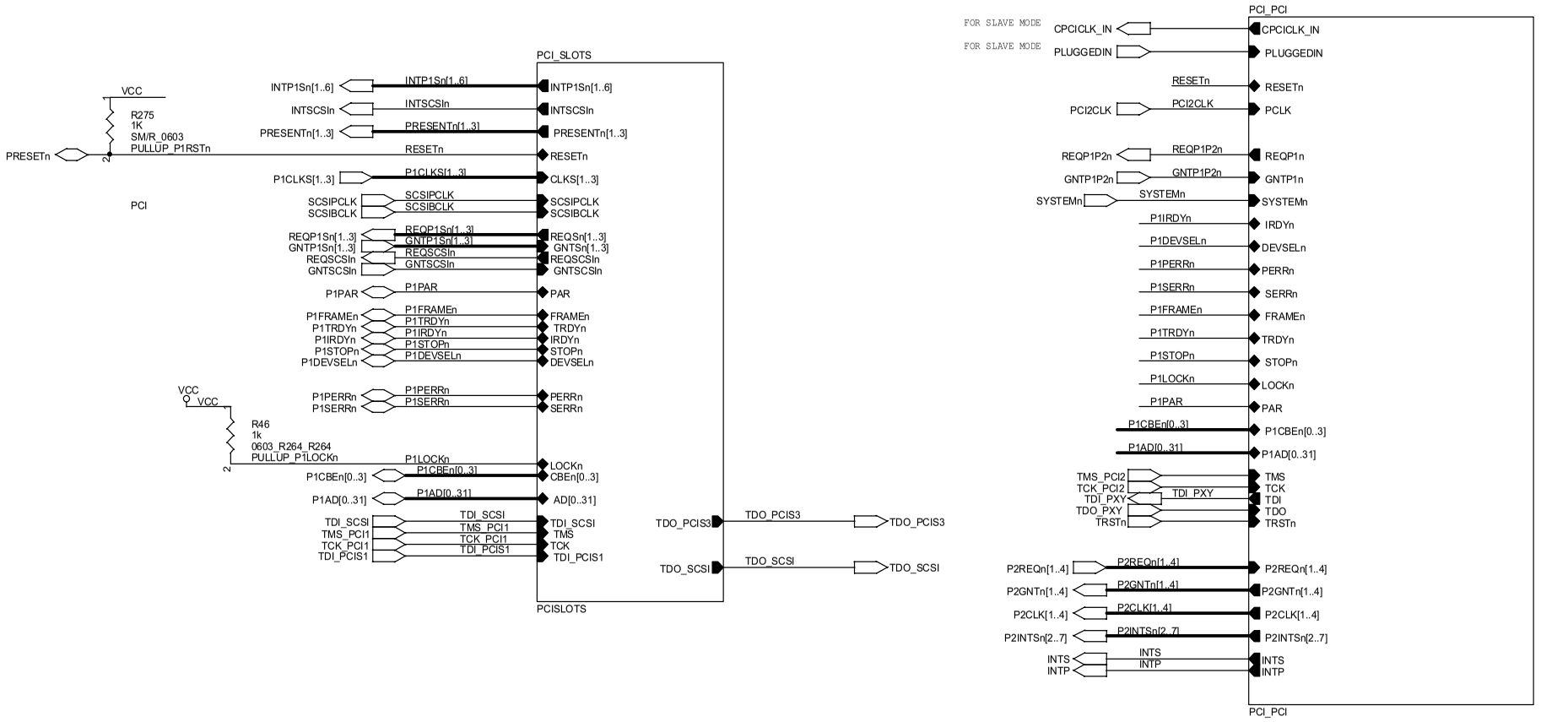
GND GND

VCC VCC

Title	*Fairlight ESP Pty. Ltd.*	
TSBCLOCK.sch	*Unit B 5 Skyline Place* *Frenchs Forest 2086* *Australia*	
Reference: PXY		Date: Friday, May 05, 2000
Design: ajc	Revision: 4	Sheet: 19 of 45



Title	PCISLOTS.sch
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place, Frenchs Forest 2086, Australia
Reference: PXY	Date: Friday, May 05, 2000
Design: ajc	Revision: 4
	Sheet: 23 of 45



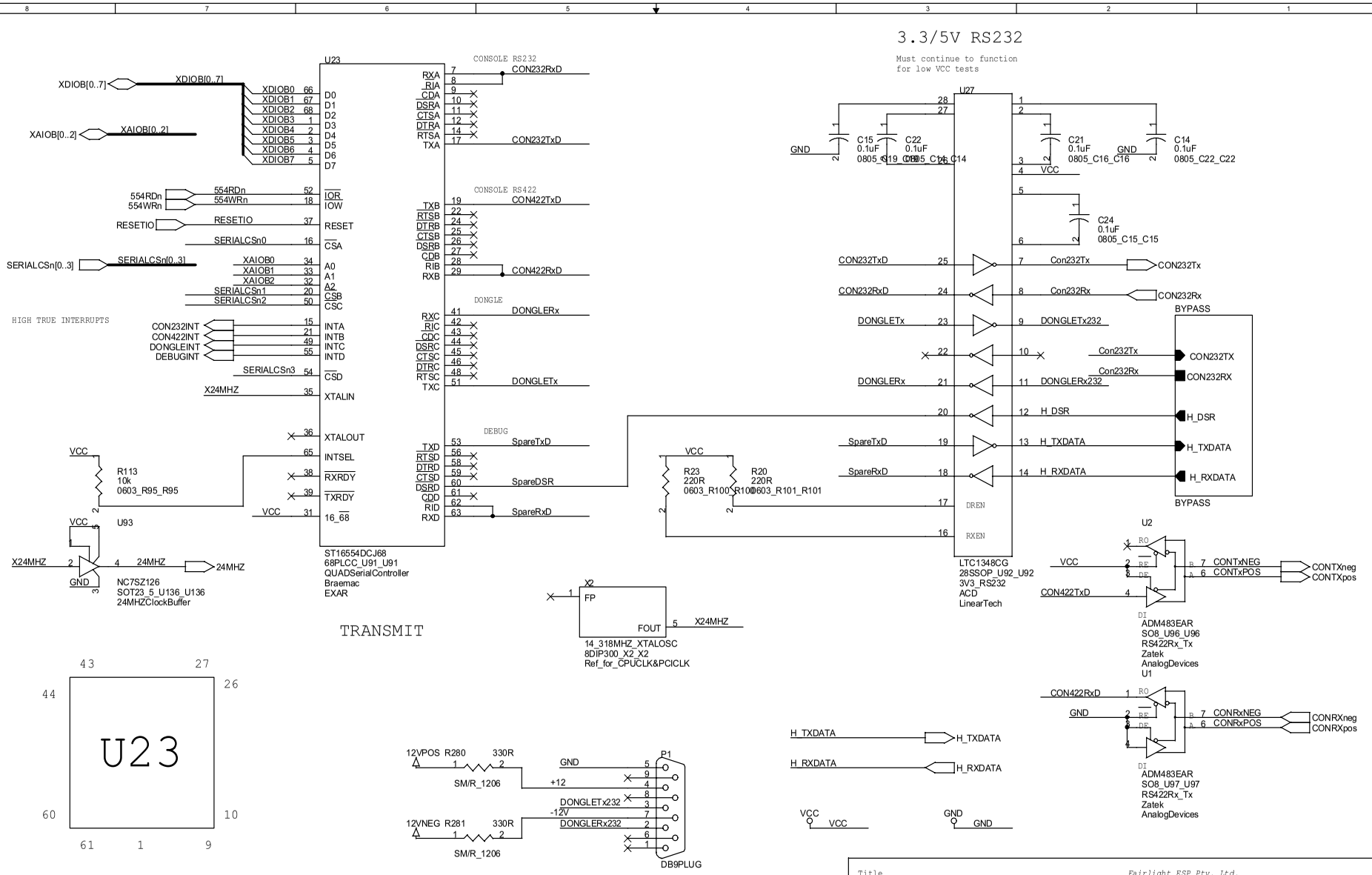
Title

PCI.sch

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 21 of 45


3.3/5V RS232
Must continue to function
for low VCC tests
U23
CONSOLE RS232
CONSOLE RS422
DONGLE
DEBUG
HIGH TRUE INTERRUPTS
ST16554DCJ68
68PLCC_U91_U91
QUADSerialController
Braemac
EXAR
TRANSMIT
U27
LTC1348CG
28SSOP_U92_U92
3V3_RS232
ACD
LinearTech
BYPASS
U2
ADM483EAR
SO8_U96_U96
RS422Rx_Tx
Zatek
AnalogDevices
U1
ADM483EAR
SO8_U97_U97
RS422Rx_Tx
Zatek
AnalogDevices
U93
NC7SZ126
SOT23_5_U136_U136
24MHZClockBuffer
X2
14_318MHZ_XTALOSC
8DIP300_X2_X2
Ref_for_CPUCLK&PCICLK
P1
DB9PLUG
DONGLE
Title
XIOCOMMS.sch
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: PXY
Design: ajc
Revision: 4
Date: Friday, May 05, 2000
Sheet: 11 of 45

9MW410C1 - Back Panel Connector Card

Terminology

IOC1	MW4-IOC1 IO connector card
PXY	MW4-PXY dual processor card

Signal names are in italics.
Signal names postfixed with n are active low.

1. Introduction

The IOC1 card provides all of the synchronisation connectors which were present on the MFX3 SIO cards.

In addition to the above, the IOC1 has two serial ports (SERIAL and MODEM), PC style parallel port (PARALLEL). The hardware for the general purpose IO (GPIO) is also on IOC1.

2. Functional Description

2.1 Edge connector (sheet 1)

The connecor at J1 mates with the connector J1 on the PXY.

A buffer at U1 (74FCT245) isolates the data bus from this card to the PXY. When an access to the IOC1 is made, the CONENn signal is asserted low. If the access is a read, the DIR signal will be high; for writes, it is low.

All connectors are EMC isolated with BLA3216A600SG4 inductors.

U12 (74FCT541) buffers the BPI_TACH,BIPDIR) signals. These signals are a two wire biphase interface to old style film machines.

2.2 GPIO (sheet 2)

The GPIO interface has an output port latched by U5 (74FCT574), an input port U4 (74FCT541) and a bank select latched by U3 (74FCT574).

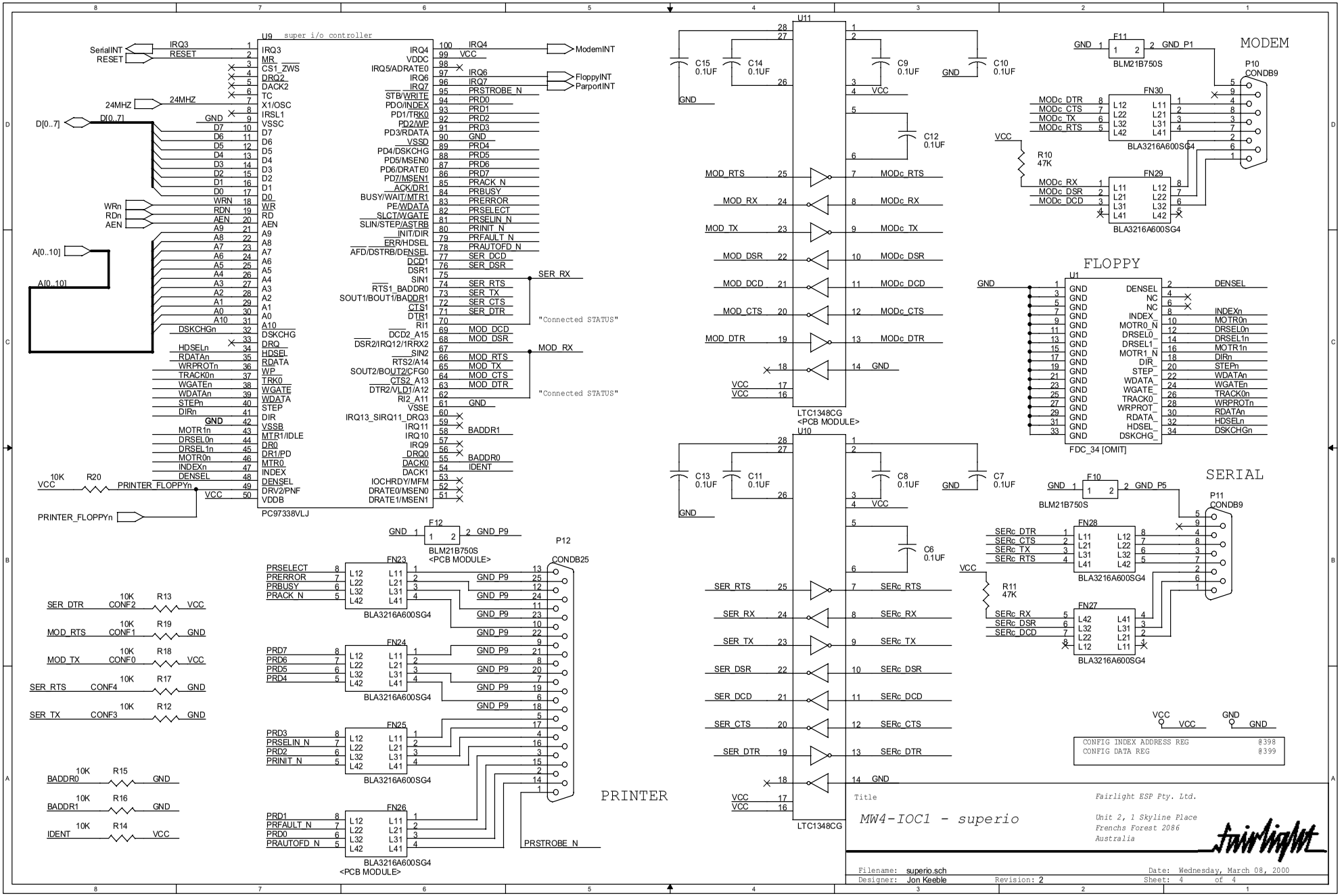
All connections are EMC isolated with BLA3216A600SG4 inductors to connector P3.

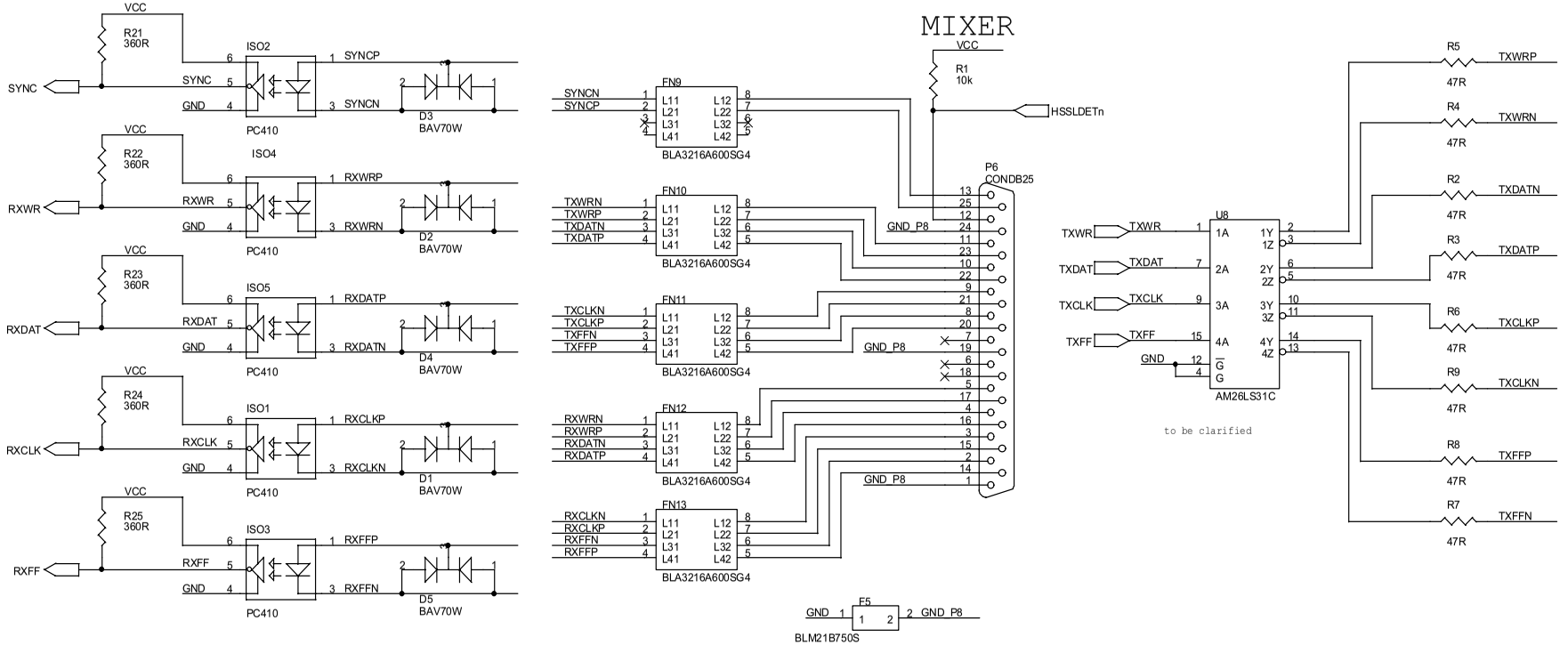
2.3 Mixer Interface (sheet 3)

ISO1 to ISO5 optically isolate all inputs. As these devices are open-collector output, they all have a 390R pullup resistor on their outputs. BAV90 diodes are used to protect the opto-isolators against large voltages.

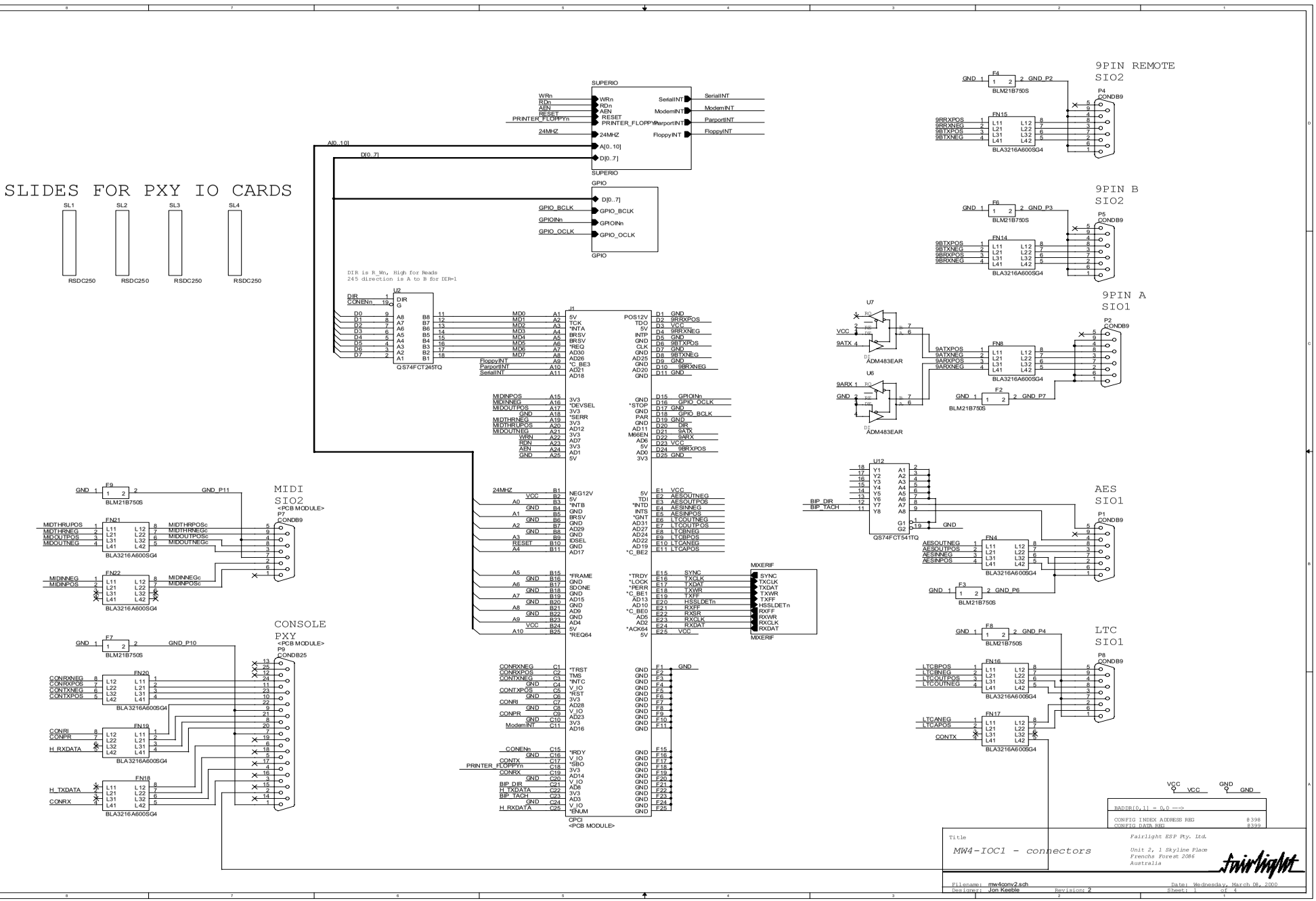
U8 (AM26C31) differentially buffers all of the output signals which feed a 100R line.

The mixer interface connects to the CG5 card placed in the CGA slot on


U9 super i/o controller
PC97338VLJ
SerialINT
RESET
24MHZ
D[0..7]
A[0..10]
WRn
RDn
AEN
DSKCHGn
HDSELn
RDATAn
WRPROTn
TRACK0n
WGATEn
WDATAn
STEPn
DIRn
MOTR1n
DRSEL0n
DRSEL1n
MOTR0n
INDEXn
DENSEL
PRINTER_FLOPPYn
ModemINT
FloppyINT
ParportINT
SER_RX
MOD_RX
"Connected STATUS"
BADDR1
BADDR0
IDENT
PRSTROBE_N
U11
LTC1348CG
<PCB MODULE>
MODc_RTS
MODc_RX
MODc_TX
MODc_DSR
MODc_DCD
MODc_CTS
MODc_DTR
MODEM
P10
CONDB9
BLM21B750S
BLA3216A600SG4
FLOPPY
FDC_34 [OMIT]
U10
SERc_RTS
SERc_RX
SERc_TX
SERc_DSR
SERc_DCD
SERc_CTS
SERc_DTR
SERIAL
P11
P12
CONDB25
PRINTER
FN23
FN24
FN25
FN26
FN27
FN28
FN29
FN30
F10
F11
F12
R10 47K
R11 47K
R12 10K CONF3
R13 10K CONF2
R14 10K
R15 10K
R16 10K
R17 10K CONF4
R18 10K CONF0
R19 10K CONF1
R20 10K
CONFIG INDEX ADDRESS REG 0398
CONFIG DATA REG 0399
Title
MW4-IOC1 - superio
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: superio.sch
Designer: Jon Keeble
Revision: 2
Date: Wednesday, March 08, 2000
Sheet: 4 of 4



Title	*MW4-IOC1 - mixer I/F*
Fairlight ESP Pty. Ltd.	*Unit 2, 1 Skyline Place, Frenchs Forest 2086, Australia*
Filename: mixerif.sch	Date: Thursday, March 09, 2000
Designer: Jon Keeble	Revision: 2
	Sheet: 3 of 4


SLIDES FOR PXY IO CARDS
SL1
SL2
SL3
SL4
RSDC250
RSDC250
RSDC250
RSDC250
SUPERIO
WRn
RDn
AEN
RESET
PRINTER_FLOPPYn
24MHZ
A[0..10]
D[0..7]
SerialINT
ModemINT
ParportINT
FloppyINT
GPIO
GPIO_BCLK
GPIOINn
GPIO_OCLK
DIR is R_Wn, High for Reads
245 direction is A to B for DIR=1
U2
QS74FCT245TQ
J1
GPCI
<PCB MODULE>
MIXERIF
9PIN REMOTE
SIO2
P4
CONDB9
BLM21B750S
BLA3216A600SG4
9PIN B
SIO2
P5
9PIN A
SIO1
P2
U7
U6
ADM483EAR
AES
SIO1
P1
U12
QS74FCT541TQ
LTC
SIO1
P8
MIDI
SIO2
<PCB MODULE>
P7
CONSOLE
PXY
P9
CONDB25
VCC
GND
BADDR[0..1] = 0,0 ---->
CONFIG INDEX ADDRESS REG 0398
CONFIG DATA REG 0399
Title
MW4-IOC1 - connectors
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: mw4conv2.sch
Designer: Jon Keeble
Revision: 2
Date: Wednesday, March 08, 2000
Sheet: 1 of 4

DRAFT

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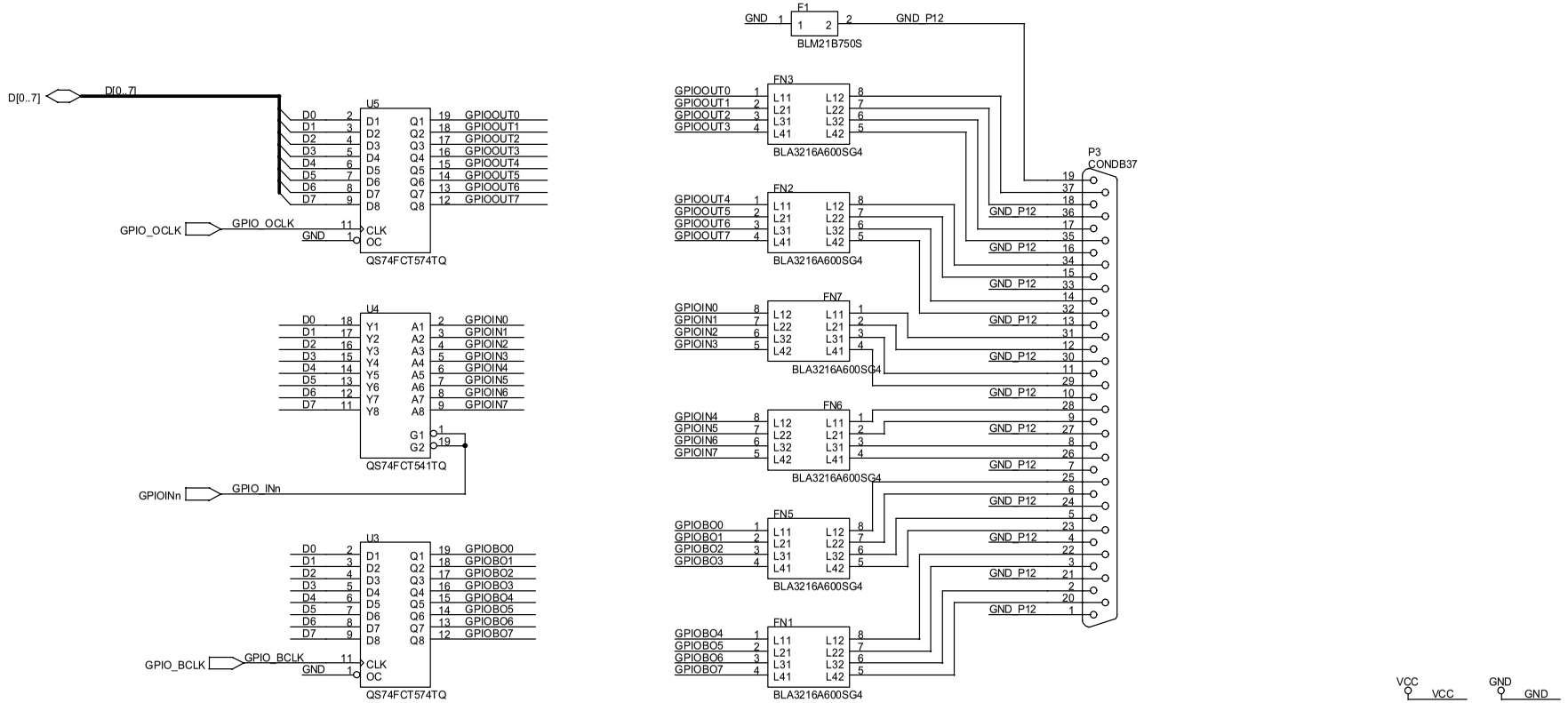
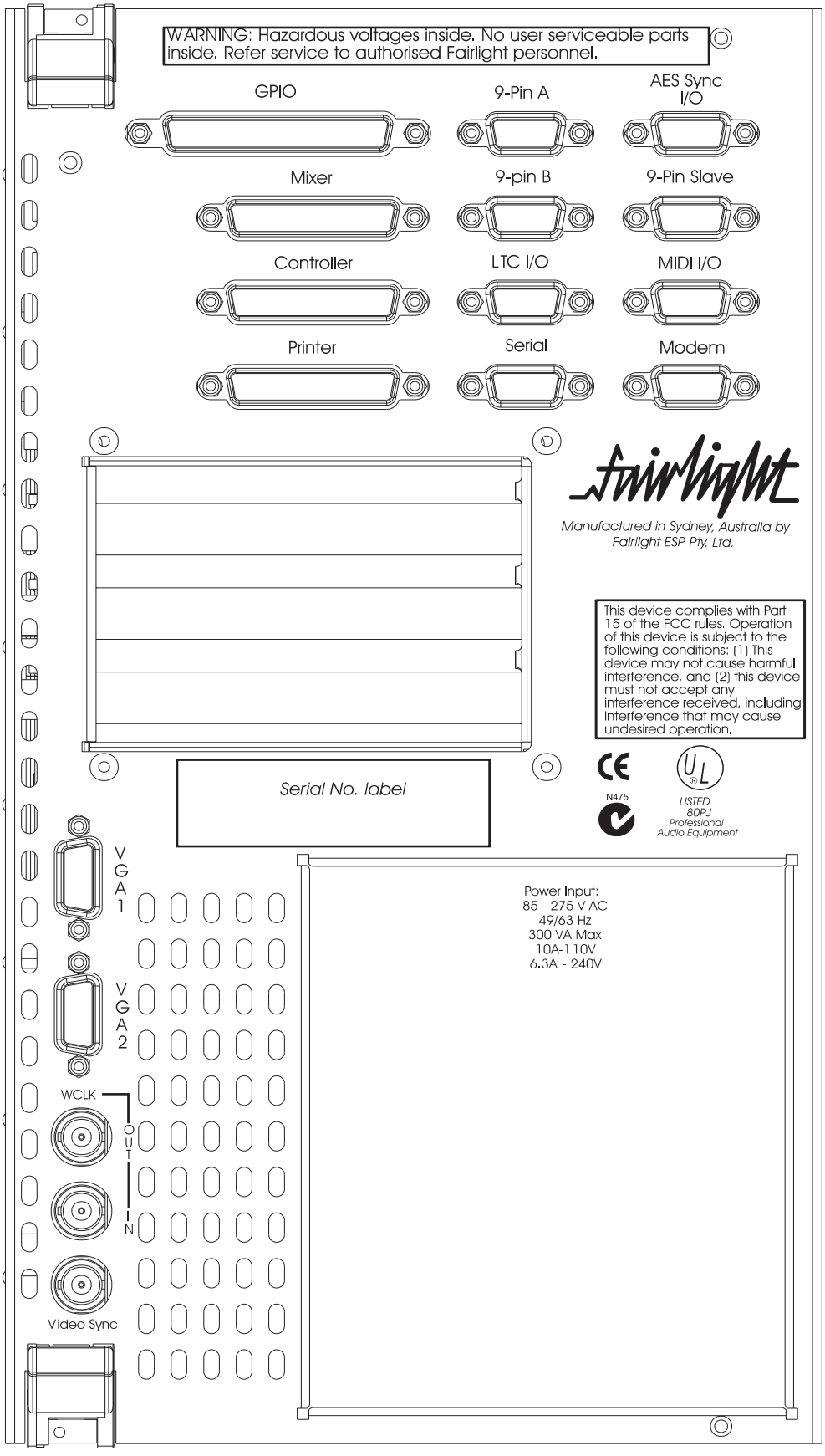
GPIO



Title			*Fairlight ESP Pty. Ltd.*
MW4-IOC1 - GPIO			*Unit 2, 1 Skyline Place* *Frenchs Forest 2086* *Australia*
Filename: gpio.sch		Date: Wednesday, March 08, 2000	
Designer: Jon Keeble	Revision: 2	Sheet: 2 of 4	

A2 CONTROL & REFERENCE PINOUTS



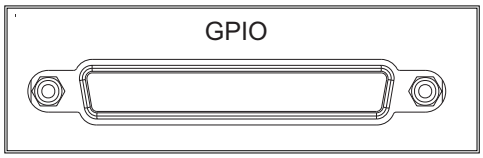
Engine System I/O Panel

A3 General Purpose Interface

Connector 37 Pin D Male

Input TTL (1 LS Load)

Output/Bank TTL (max 5 TTL loads)



1	GND
2	GPIO6
3	GPIO5
4	GND
5	GPIOBO2
6	GPIOBO1
7	GND
8	GPIOIN6
9	GPIOIN5
10	GND
11	GPIOIN2
12	GPIOIN1
13	GND
14	GPIOOUT6
15	GPIOOUT5
16	GND
17	GPIOOUT2
18	GPIOOUT1
19	GND
20	GPI0B07
21	GND
22	GPI
23	GPIOBO3
24	GND
25	GPIOBO0
26	GPIOIN7
27	GND
28	GPIOIN4
29	GPIOIN3
30	GND
31	GPIOINO
32	GPIOOUT7
33	GND
34	GPIOOUT4
35	GPIOOUT3
36	GND
37	GPIOOUT0

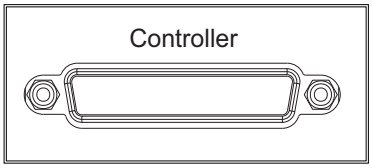
A4 Mixer

Connector 25 pin D Female

1	GND
2	RxFFN
3	RxCLKN
4	RxDATN
5	RxWRN
6	NC
7	NC
8	TxFFN
9	TxCLKN
10	TxDATN
11	TxWRPN
12	HSSLDETn
13	SYNCN
14	RxFFP
15	RxCLKP
16	RxDATP
17	RxWRP
18	NC
19	GND
20	TxFFP
21	TXxCLKP
22	TxDATP
23	TxWRP
24	GND
25	SYNCP

A5 Controller

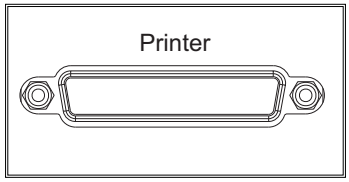
Connector 25 pin D Male



PIN 1	GND
PIN 2	CONTx
PIN 3	CONRx
PIN 4	NC
PIN 5	H_TxDATA
PIN 6	CONPR
PIN 7	GNDC
PIN 8	NC
PIN 9	GNDC
PIN 10	CONTxPOS
PIN 11	CONRxPOS
PIN 12	NC
PIN 13	NC
PIN 14	NC
PIN 15	NC
PIN 16	NC
PIN 17	NC
PIN 18	NC
PIN 19	NC
PIN 20	H_RxDATA
PIN 21	CONPR
PIN 22	CONPR
PIN 23	CONRI
PIN 24	CONRxNEG
PIN 25	NC

A6 PRINTER

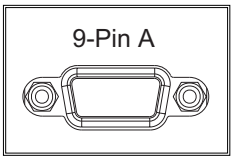
Connector Standard 25 pin D female



PIN 1	PSTROBEn
PIN 2	PDR0
PIN 3	PDR1
PIN 4	PDR2
PIN 5	PDR3
PIN 6	PDR4
PIN 7	PDR5
PIN 8	PDR6
PIN 9	PDR7
PIN 10	PRACKn
PIN 11	PRBUSYn
PIN 12	PRERROR
PIN 13	PRSELECT
PIN 14	PRAUTOFDn
PIN 15	PRFAULTn
PIN 16	PRINTITn
PIN 17	PRSELINn
PIN 18	GND
PIN 19	GND
PIN 20	GND
PIN 21	GND
PIN 22	GND
PIN 23	GND
PIN 24	GND
PIN 25	GND

A8 9-Pin A

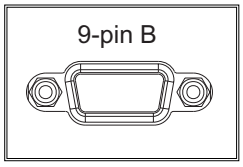
Connector 9 pin D Female



PIN 1	GND
PIN 2	9ARxA
PIN 3	9ATxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9ARxB
PIN 8	9ATxA
PIN 9	NC

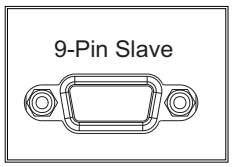
A9 9-Pin B

Connector 9 pin D Female



PIN 1	GND
PIN 2	9BRxA
PIN 3	9BTxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9BRxB
PIN 8	9BTxA
PIN 9	NC

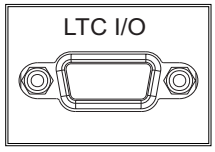
A10 9-Pin Slave



Connector 9 pin D Female

PIN 1	GND
PIN 2	9BTxA
PIN 3	9RRxB
PIN 4	GND
PIN 5	NC
PIN 6	GND
PIN 7	9BTxB
PIN 8	9BRxA
PIN 9	GND

A11 LTC - I/O



Connector 9 pin D Male

Input Level -20dbm to +10dbm

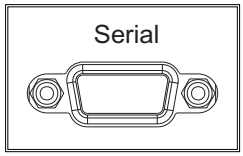
Output Level 0dbm

Important note: Unbalanced loads connected to LTC OUT should NOT ground the LTC OUT NEGATIVE signal.

PIN 1	GND
PIN 2	LTC A NEGATIVE
PIN 3	LTC OUT NEGATIVE
PIN 4	GND
PIN 5	LTC B POSITIVE
PIN 6	LTC A POSITIVE
PIN 7	GND
PIN 8	LTC OUT POSITIVE
PIN 9	LTC B NEGATIVE

A12 Serial Port

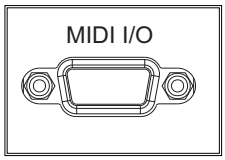
Connector Standard 9 pin D male



PIN 1	SER_DCD
PIN 2	SER_Rx
PIN 3	SER_Tx
PIN 4	SER_DTR
PIN 5	GND
PIN 6	SER_DSR
PIN 7	SER_RTS
PIN 8	SER_CTS
PIN 9	NC

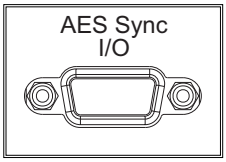
A13 Midi I/O

Connector 9 pin D female



PIN 1	NOT CONNECTED		
PIN 2	MIDI IN NEGATIVE	MIDI IN	DIN PIN 5
PIN 3	MIDI OUT NEGATIVE	MIDI OUT	DIN PIN 5
PIN 4	GND	MIDI THROUGH	DIN PIN 2
PIN 5	MIDI THROUGH POSITIVE	MIDI THROUGH	DIN PIN 4
PIN 6	MIDI POSITIVE	MIDI IN	DIN PIN 4
PIN 7	GND	MIDI OUT	DIN PIN 2
PIN 8	MIDI OUT POSITIVE	MIDI OUT	DIN PIN 4
PIN 9	MIDI THROUGH NEGATIVE	MIDI THROUGH	DIN PIN 5

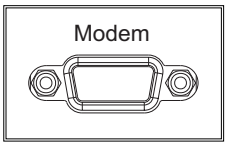
A14 AES Sync I/O



Connector 9 pin D Male

PIN 1	GND
PIN 2	AES IN NEGATIVE
PIN 3	AES OUT POSITIVE
PIN 4	BIPHASE TACH
PIN 5	BIP DIRECTION
PIN 6	AES IN POSITIVE
PIN 7	GND
PIN 8	AES OUT NEGATIVE
PIN 9	NOT CONNECTED

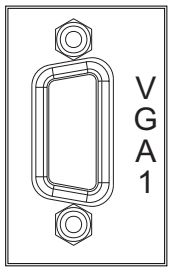
A15 Modem



Connector 9 pin D Male

PIN 1	MOD_DCD
PIN 2	MOD_RX
PIN 3	MOD_TX
PIN 4	MOD_DTR
PIN 5	GND
PIN 6	MOD_DSR
PIN 7	MOD_RTS
PIN 8	MOS_CTS
PIN 9	NC

A16 VGA



Connector 15 pin High Density D Female

Resolution 1024(H) x 768(V)

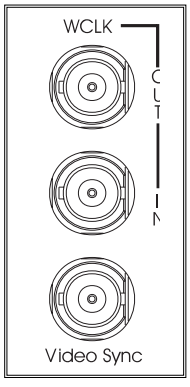
Frequency HSYNC: 60khz VSYNC: 75hz SVGA STANDARD

PIN 1	RED
PIN 2	GREEN
PIN 3	BLUE
PIN 4	GND
PIN 5	GND
PIN 6	GND
PIN 7	GND
PIN 8	GND
PIN 10	GND
PIN 11	GND
PIN 12	NC
PIN 13	HSYNC
PIN 14	VSYNC
PIN 15	NC

A17 Video Sync - In

Connector BNC

Input Level 1V p-p 75 Ohms Terminated Internally



A18 Word Clock - In

Connector BNC

Input Optically Isolated

Output Impedence 75 Ohms

A19 Word Clock - Out

Connector BNC

Output Level > 4.3V TTL

Output Impendence 75 Ohms

9MW4SIO1- Sync Generator and 9Pin Card

SIO1 Testing

1. Connect the power supply to the PXY board.

2. Connect the Xilinx pod to the PXY as follows:

   VCC: JP16 - 1 (vcc)
   GND: JP16 -2 (gnd)
   TDI TDO TMS TCK to JP7 as shown below

JP7 0 0 0 0 0
. 0 0 0 0
TDI TDO TMS TCK

3. Plug the SIO1 under test into the PXY SIO1 slot.

4. Switch on PSU.

5. Open a DOS window on the PC and 'CD' to C:\Mw4\jtag-pxy
   (Use SIO JTAG shortcut)

6. Run the command: jtag -v sio1test
   This will do the jtag testing:

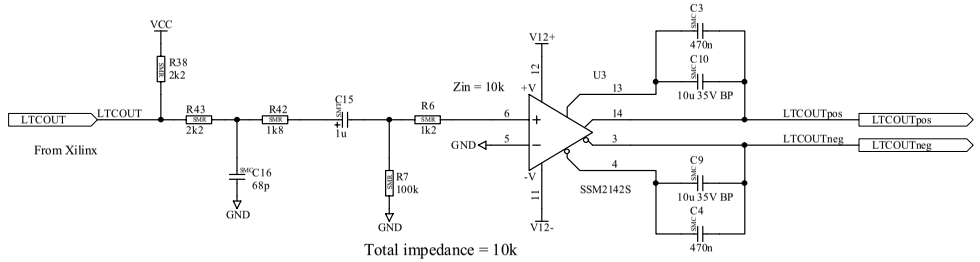
7. Open a DOS window on the PC and 'CD' to C:\Mw4\jtag
   (use SIO1 PROG shortcut)

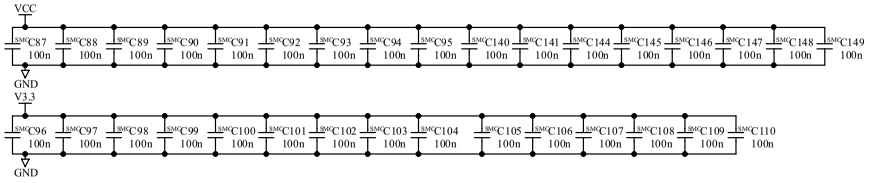
8. Run the command: jtag -v +sio1prog
   This will program the cplds.

9. Turn Off PSU and remove SI01

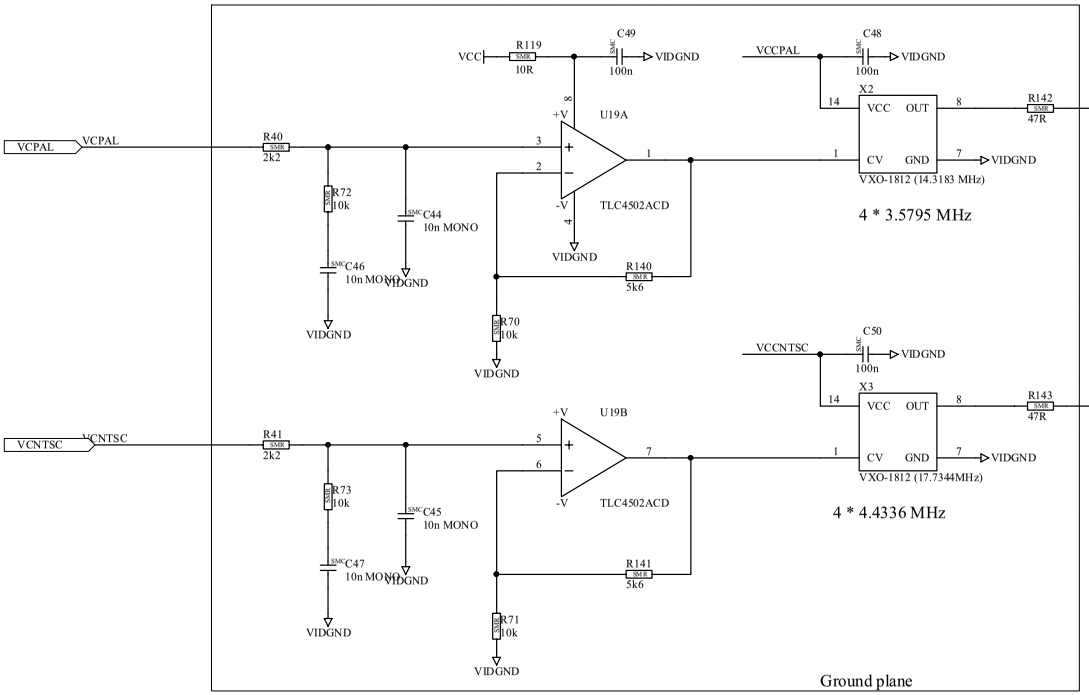
Title: ***SIO1 - Main Synch. I/O for MW4***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number: sio1.prj	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:07	Sheet 1 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\Sio1.prj			

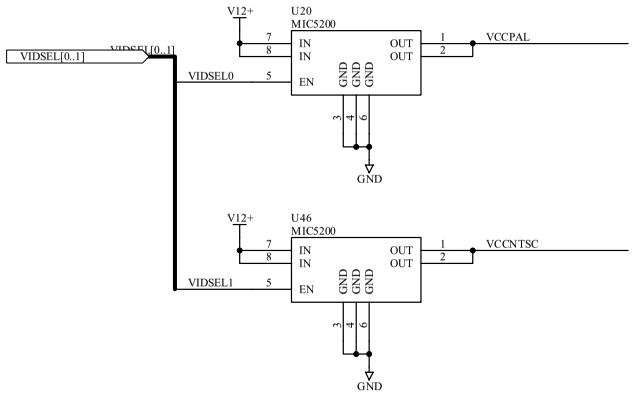
DRAFT





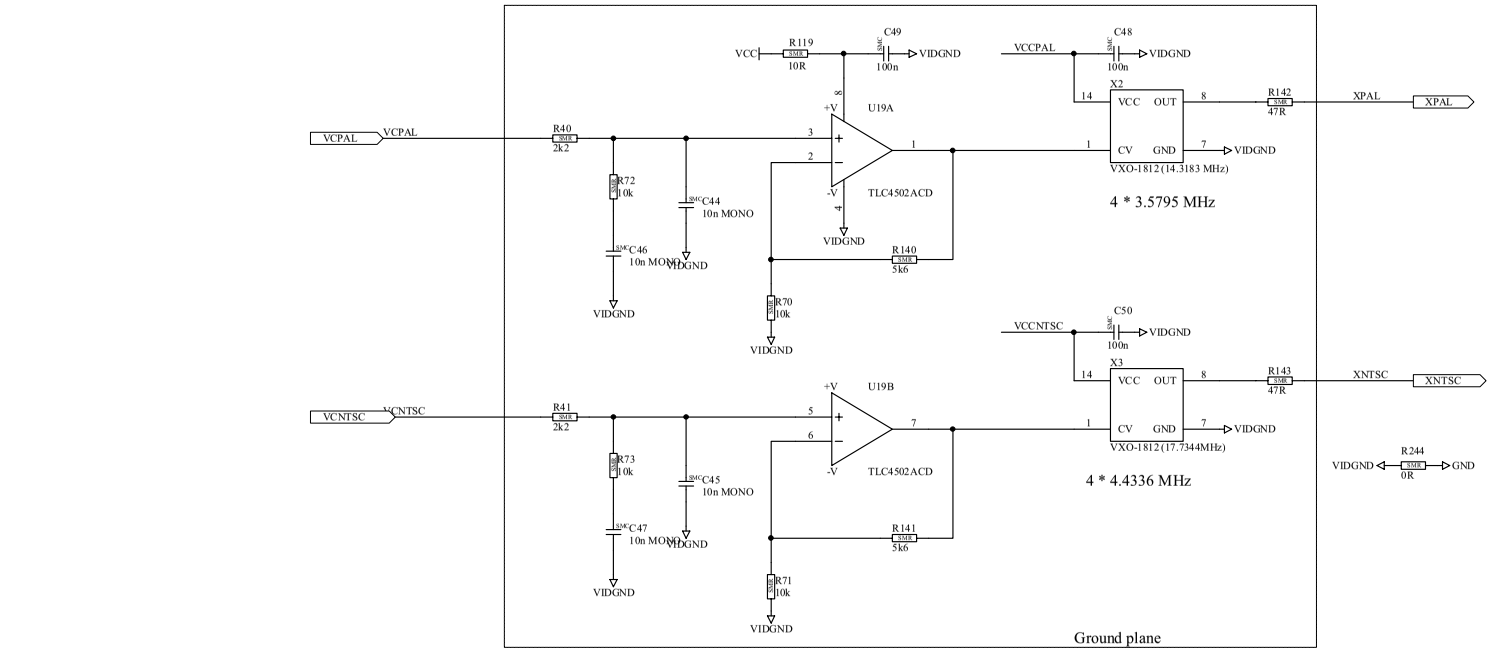
Title *SIO1 - LTC Output*			*Fairlight ESP Pty Ltd*
Size: A3	Number ltcout.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000 Time: 12:23:09		Sheet 2 of 19	*Frenchs Forest*
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\LTCOUT.SCH			*NSW*
			Australia 2086

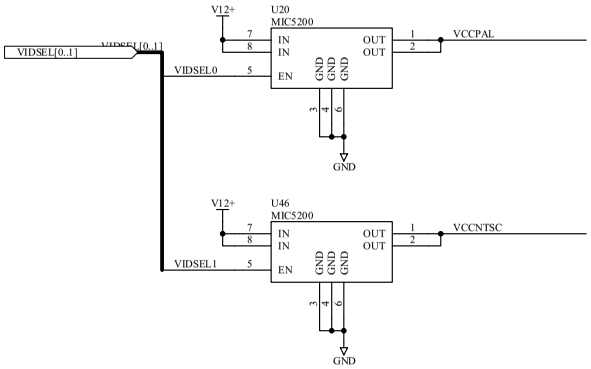




When power is switched on, the board starts up with both video VCXOs disabled.
By writing to the VIDCTRL register it is possible to turn on one, the other or both VCXOs.

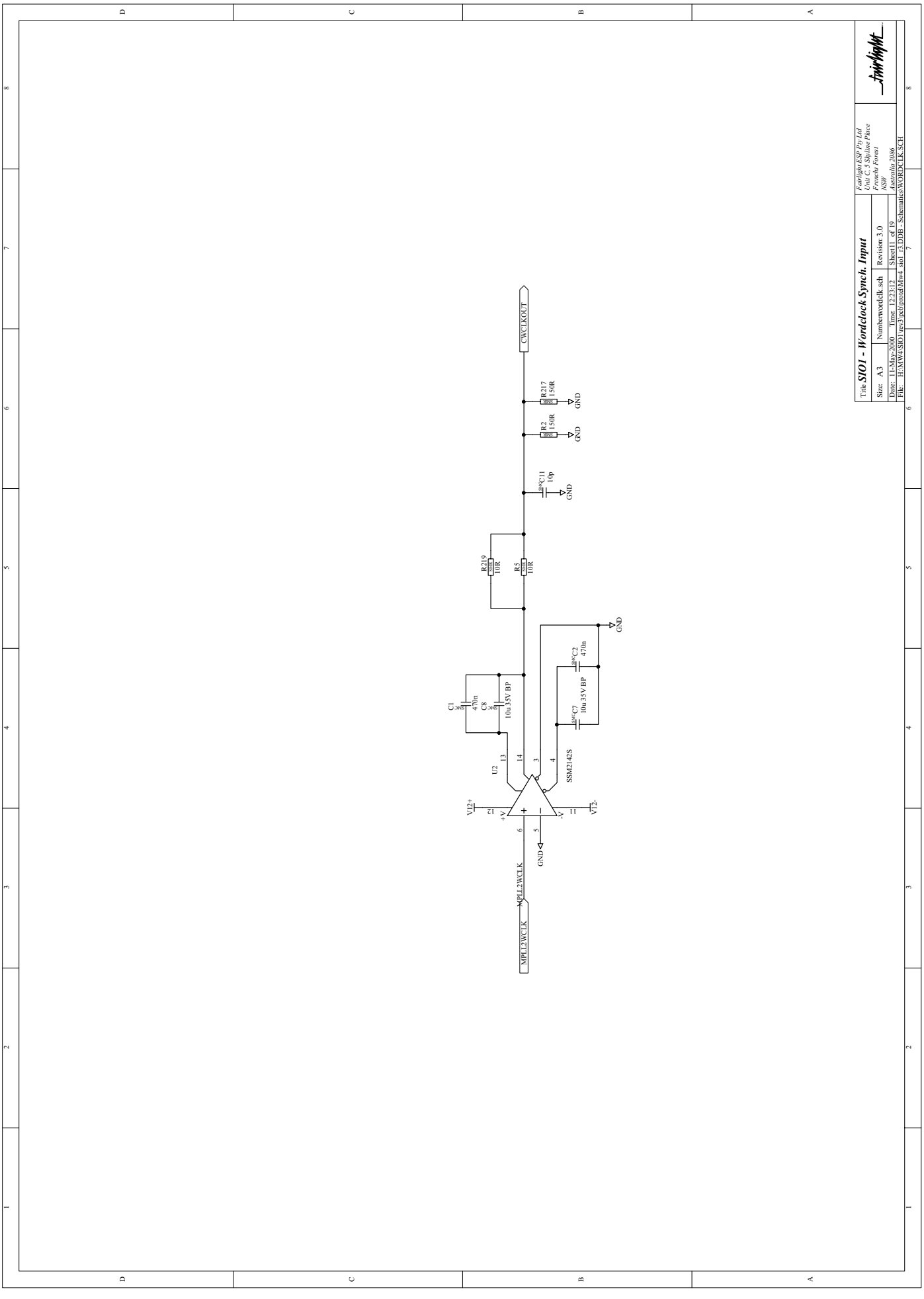
Title *SIO1- Video Synch PLLs*			*Fairlight ESP Pty Ltd*
Size: A3	Number vidvcxo.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000	Time: 12:23:11	Sheet 4 of 19	*Frenchs Forest*
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VIDVCXO.SCH			*NSW*
			Australia 2086



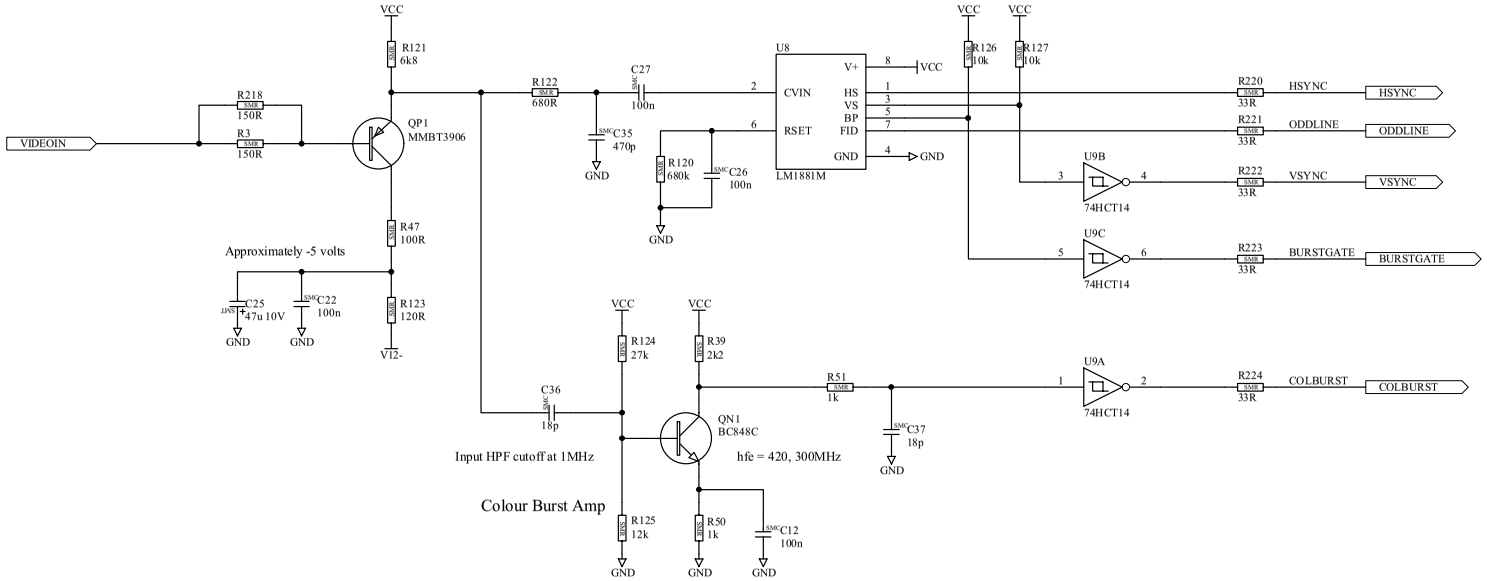


When power is switched on, the board starts up with both video VCXOs disabled.
By writing to the VIDCTRL register it is possible to turn on one, the other or both VCXOs.

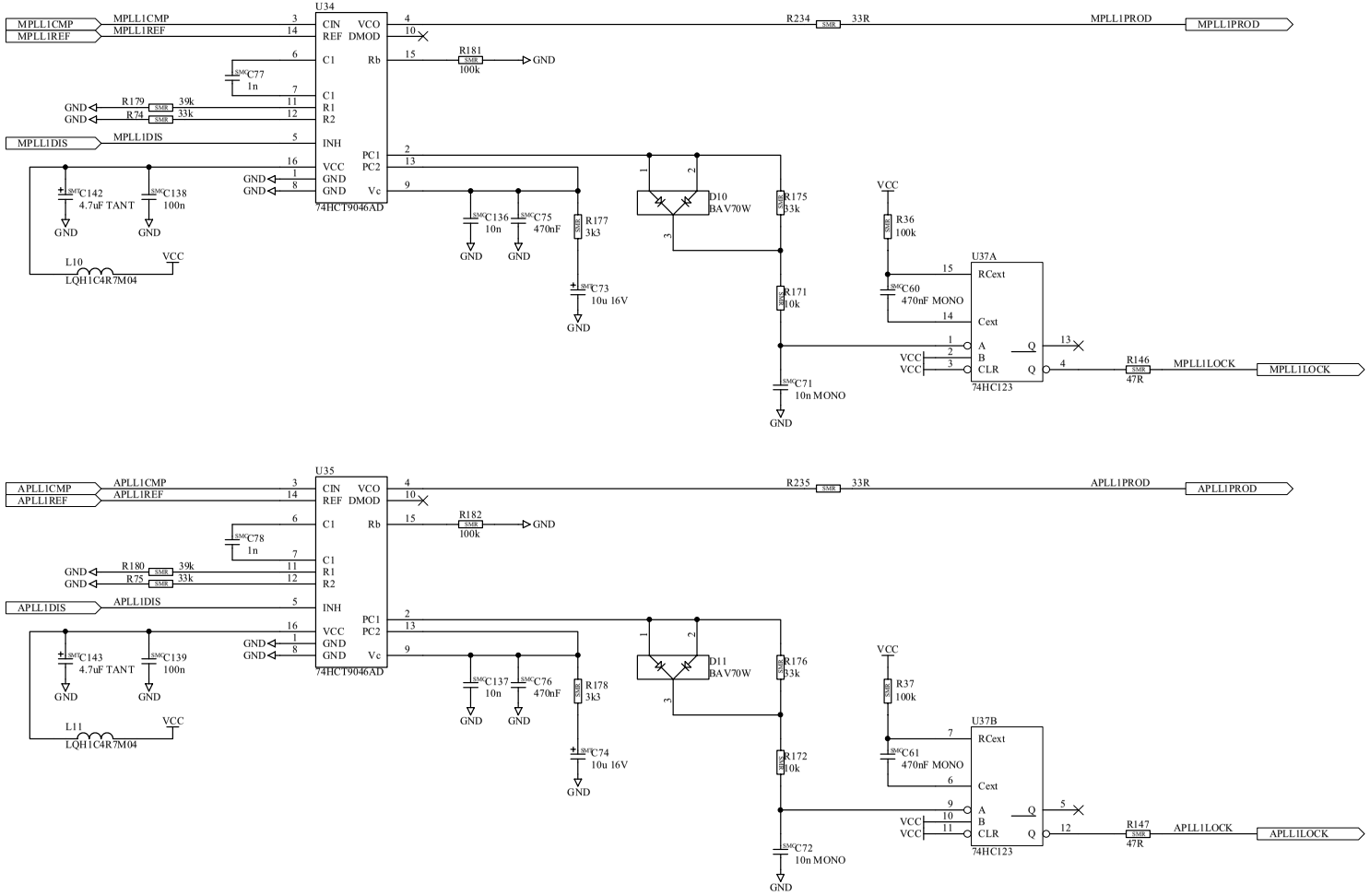
Title *SIO1- Video Synch PLLs*			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number vidvcxo.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:11	Sheet 4 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VIDVCXO.SCH			


Title SIO1 - Wordclock Synch. Input
Size: A3
Numberwordclk.sch
Revision: 3.0
Date: 11-May-2000 Time: 12:23:12
Sheet 11 of 19
File: H:\MW4\SIO1\new3-pcb\protel\Mw4_sio1_r3.DDB - Schematics\WORDCLK.SCH
Fairlight ESP Pty Ltd
Unit C, 5 Skyline Place
French's Forest
NSW
Australia 2086
CWCLKOUT
R217 150R
R2 150R
C11 10p
R219 10R
R5 10R
C2 470n
C7 10u 35V BP
C1 470n
C8 10u 35V BP
U2
SSM2142S
V12+
V12-
GND
MPLL2WCLK

DRAFT



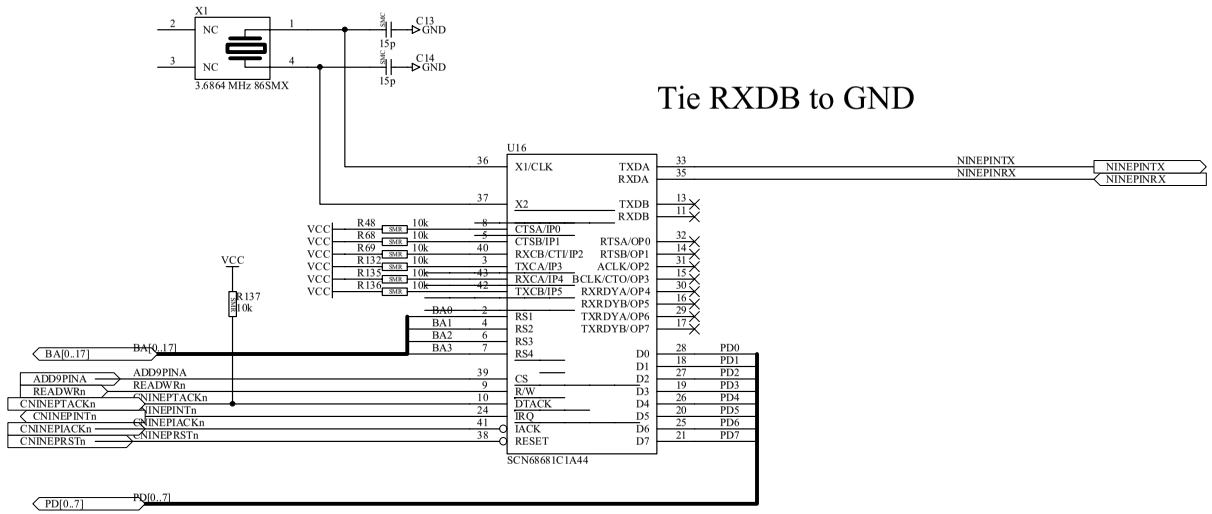
Title ***SIO1 - Video Synch. Input***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number video.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:13	Sheet 12 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VIDEO.SCH			



Title **SIO1 - Audio Clock IF PLLs**			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number pll.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:14	Sheet 13 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\PLL.SCH			

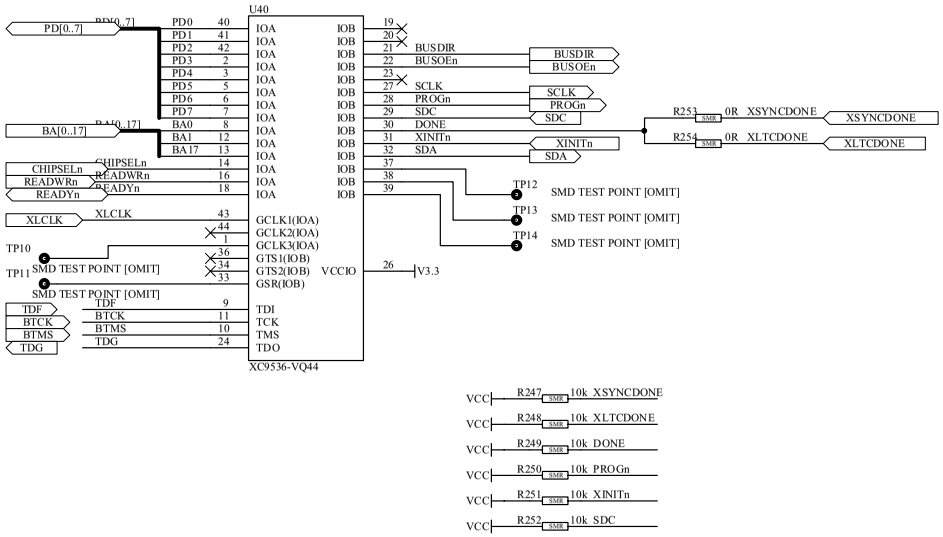
DRAFT

Place close and surround with GND plane

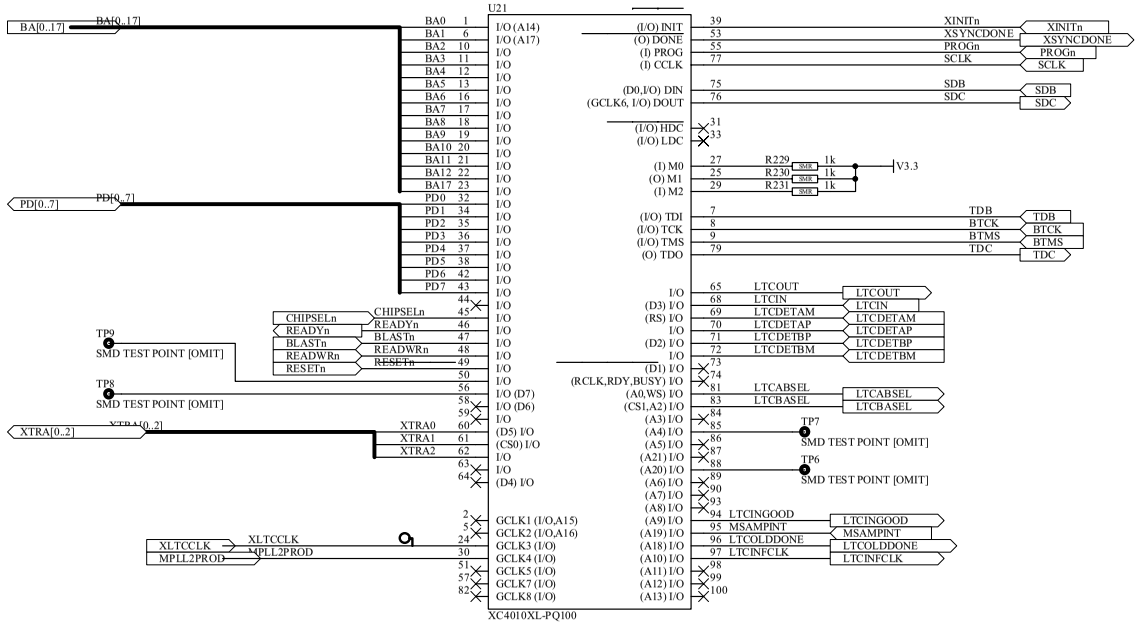


Title *SIO1 - Nine Pin Machine Control*			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number ninepin.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:15	Sheet 14 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\NINEPIN.SCH			

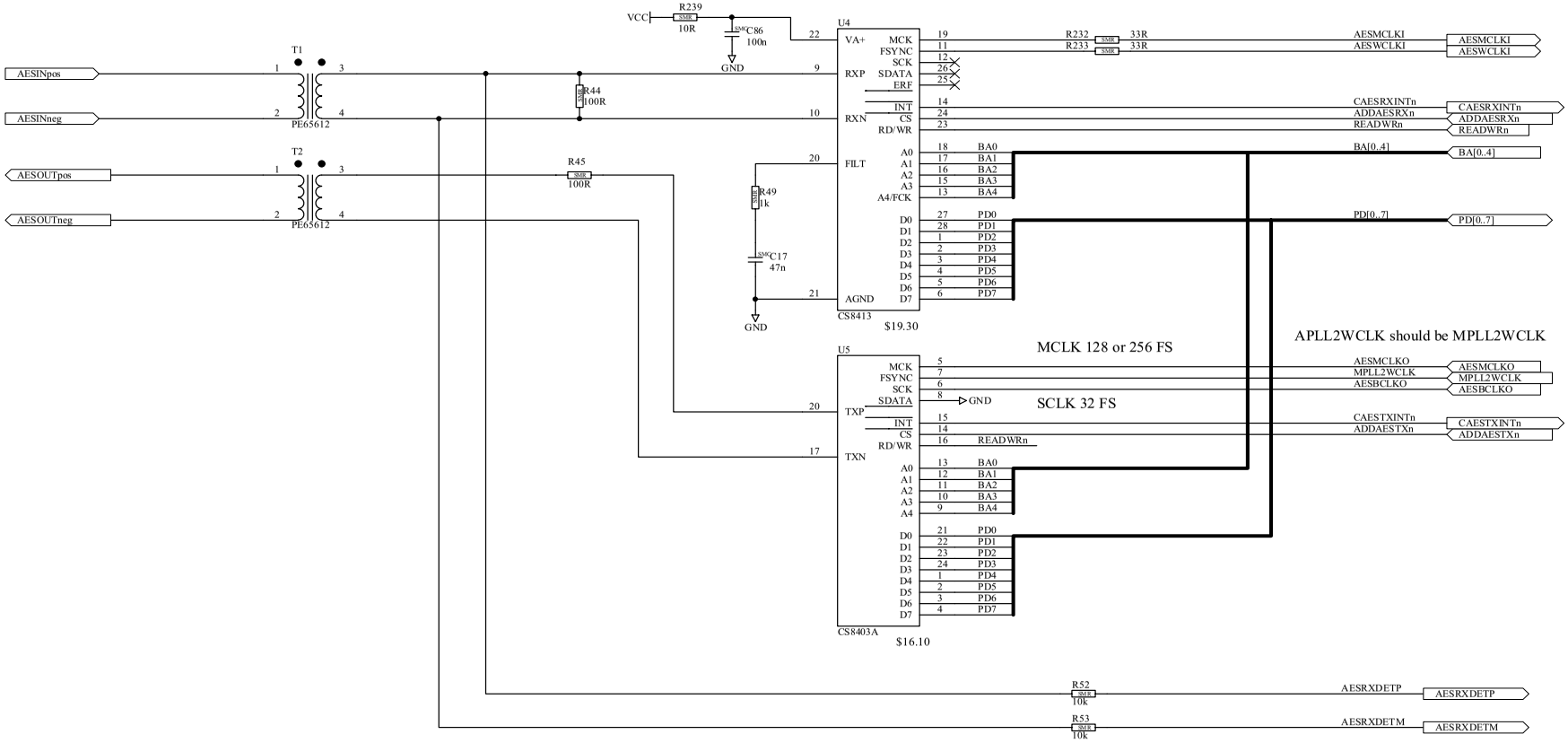
XILINX LOADER AND BUS BUFFER CONTROL



Title ***SIO1 - xilinx loader***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number:xload.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:17	Sheet 19 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\XLOAD.SCH			



Title: ***SIO1 - LTC Reader/Generator Xilinx***			*Fairlight ESP Pty Ltd*
Size: A3	Number: ltc.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000	Time: 12:23:18	Sheet 15 of 19	*Frenchs Forest*
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\XLTC.SCH			*NSW*
			Australia 2086



Title: ***SIO1 - AES Synch I/O***			*Fairlight ESP Pty Ltd*
Size: A3	Number: mes.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000 Time: 12:23:19	Sheet 5 of 19		*Frenchs Forest*
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\AES.SCH			*NSW*
			Australia 2086

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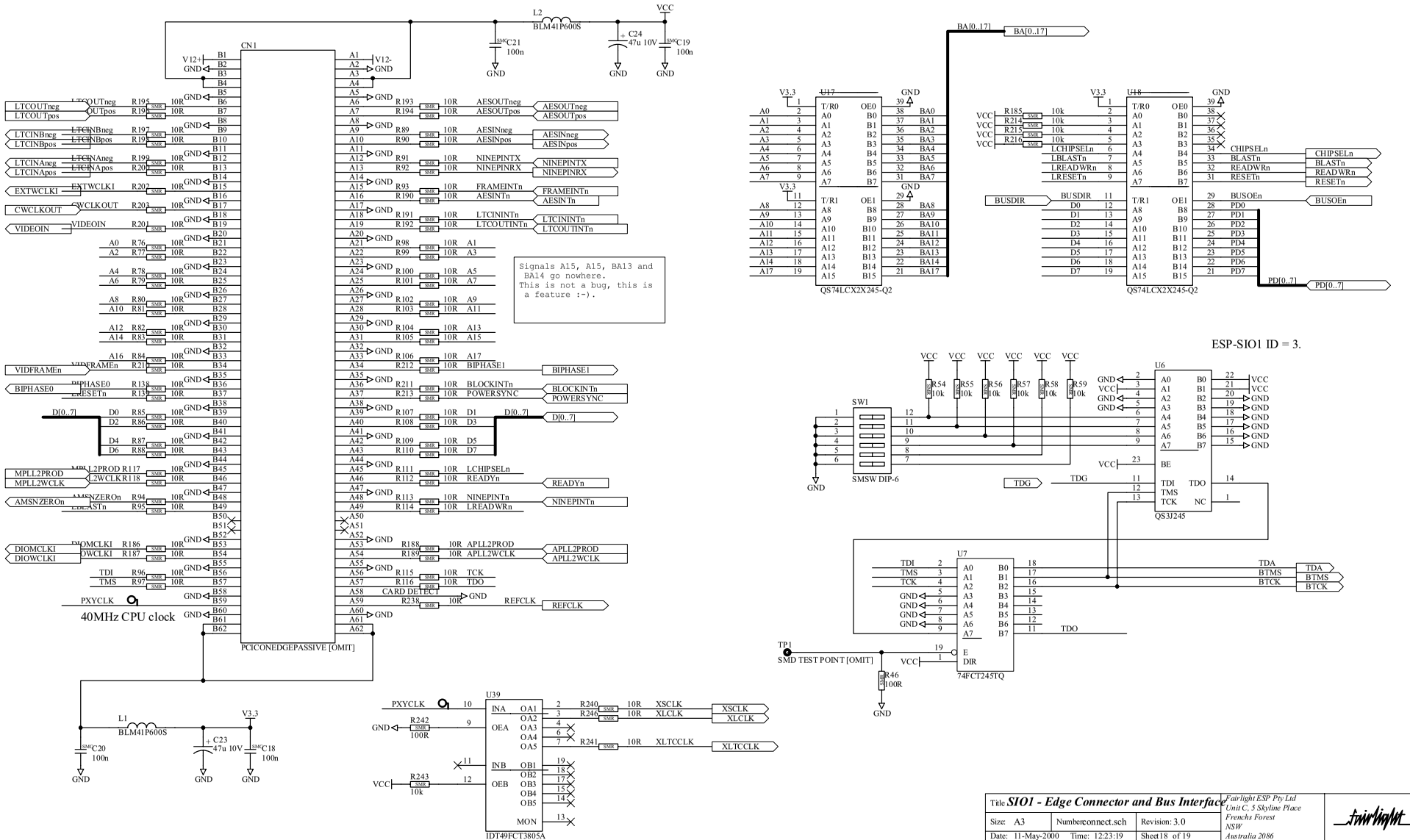

Title	***SIO1 - Edge Connector and Bus Interface***		*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Numberconnect.sch	Revision: 3.0	
Date: 11-May-2000	Time: 12:23:19	Sheet 18 of 19	
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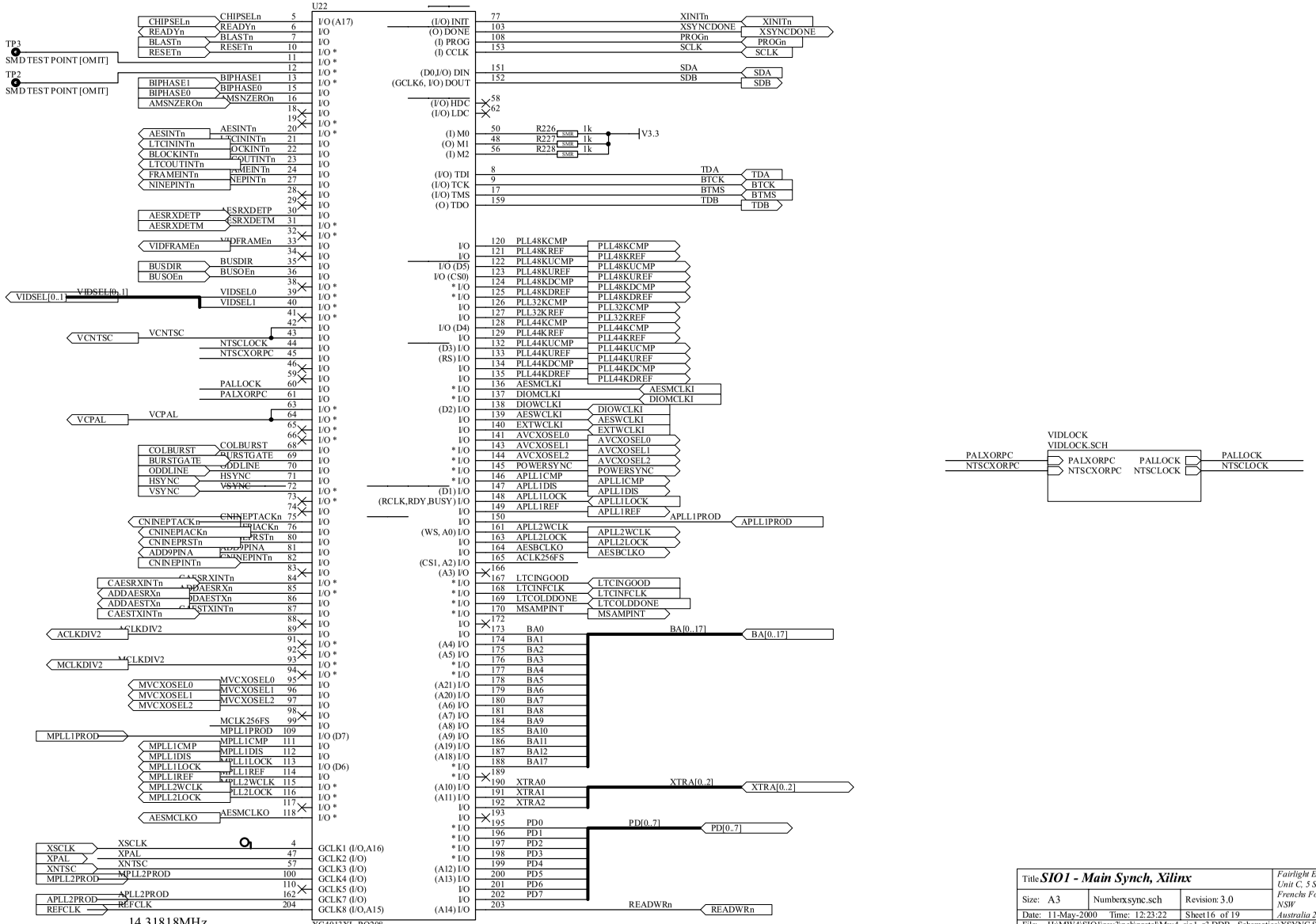

Title: ***SIO1 - Main Synch, Xilinx***			*Fairlight ESP Pty Ltd*
Size: A3	Number: xsync.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000	Time: 12:23:22	Sheet 16 of 19	*Frenchs Forest*
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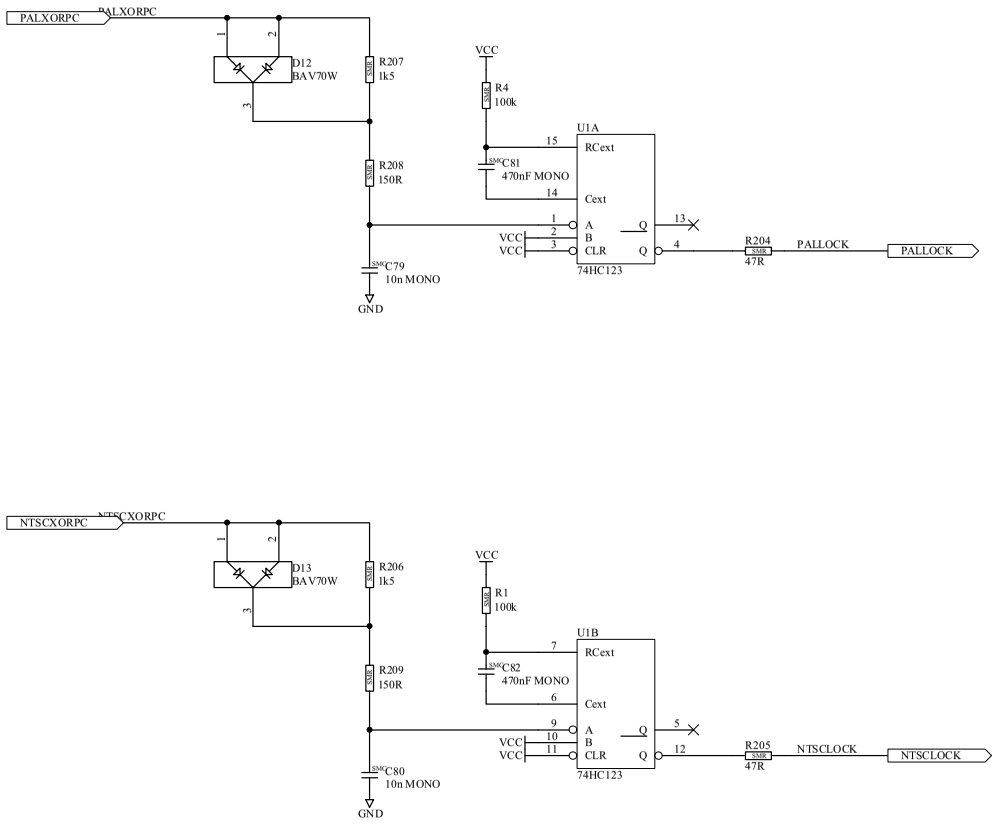
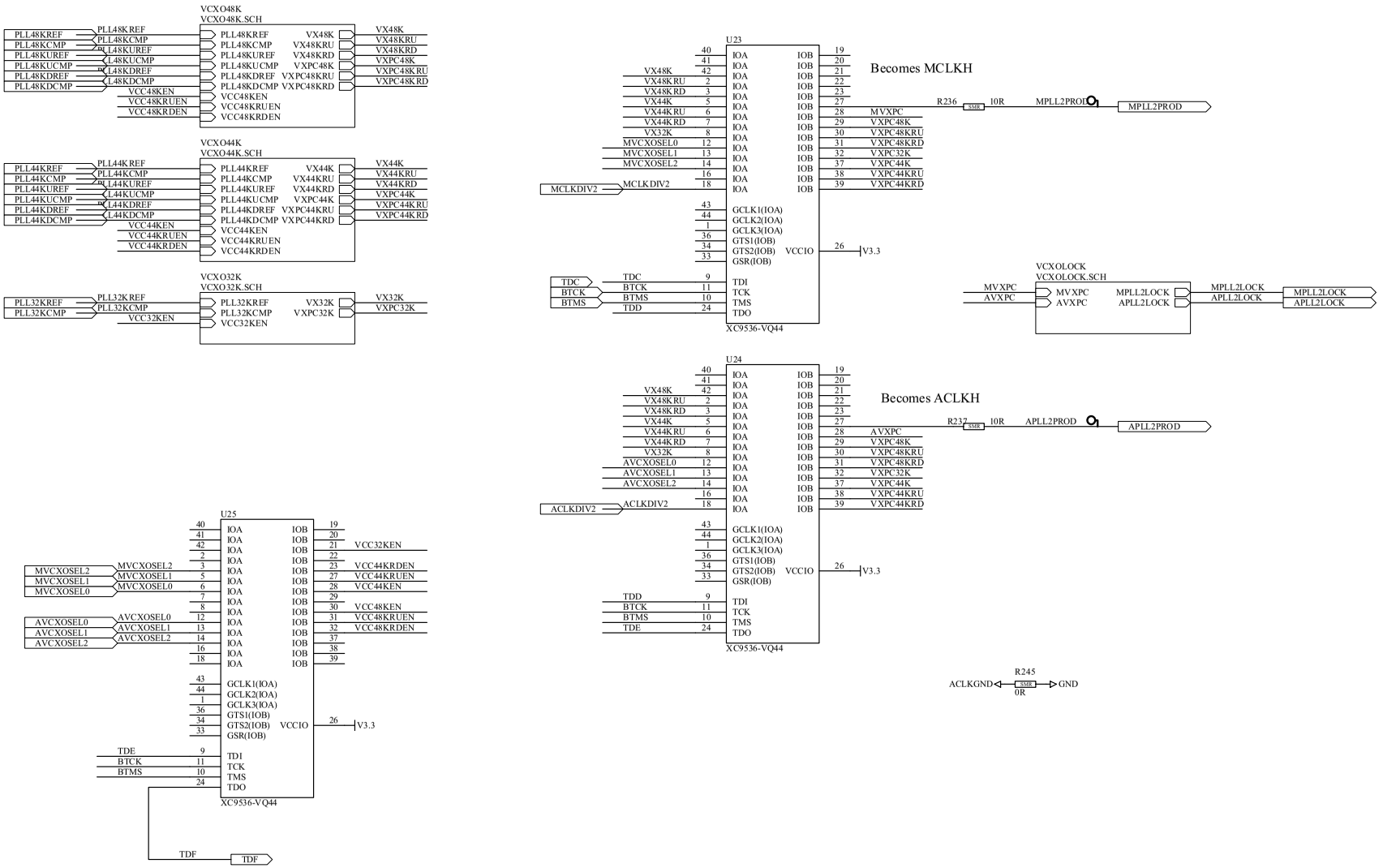
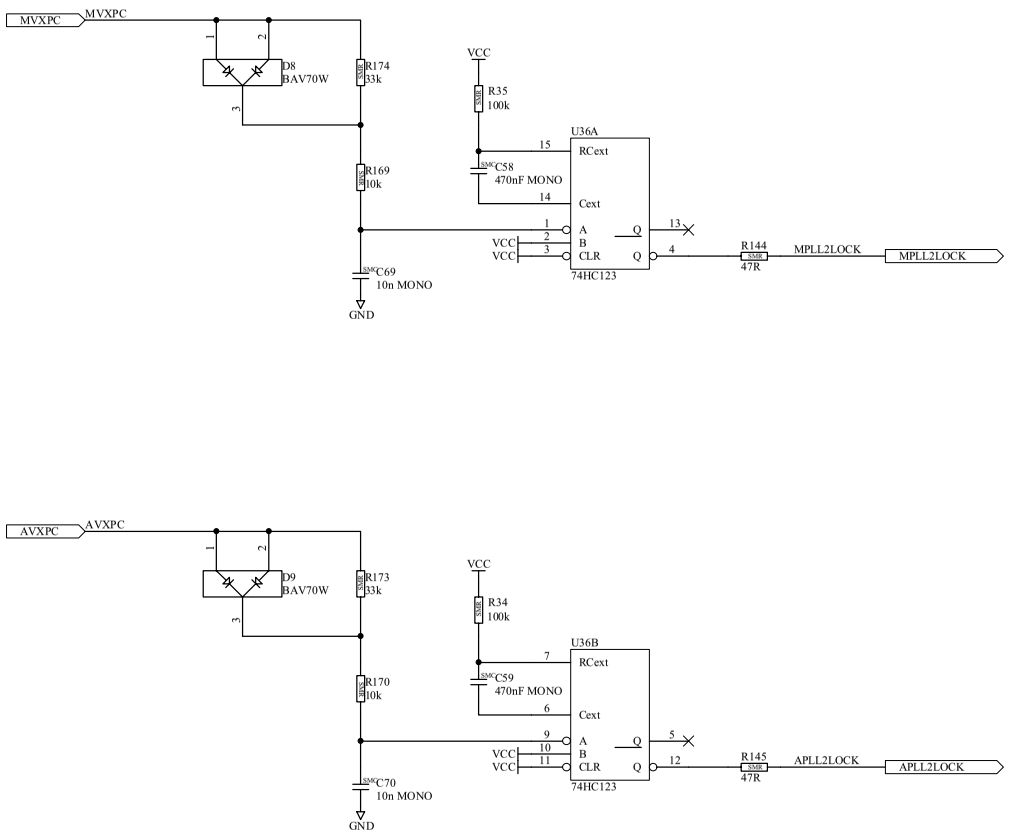
			Australia 2086



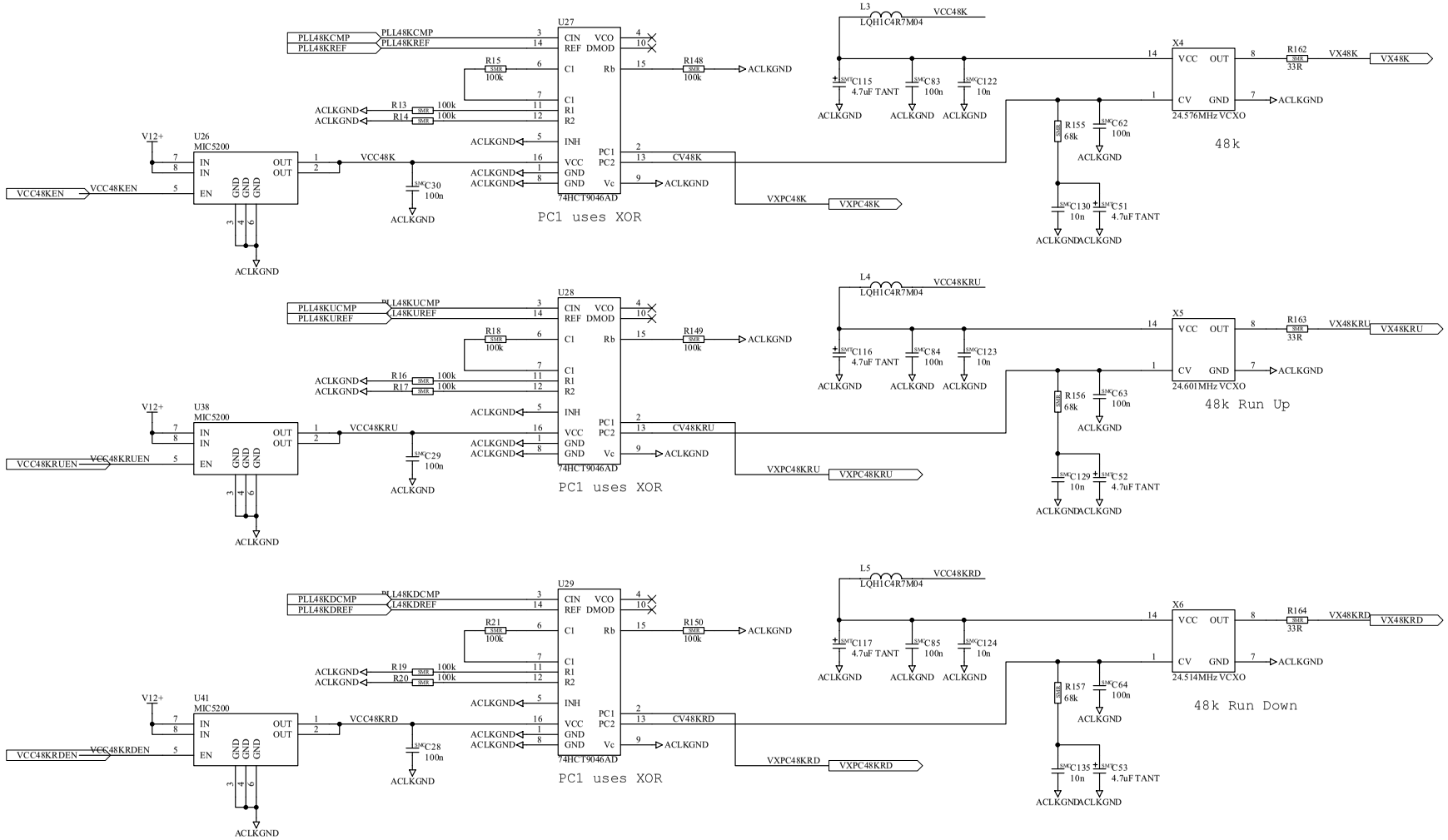
Title *SIO1 - Video PLL Lock Detect*			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number vidlock.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:23		Sheet 17 of 19	
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VIDLOCK.SCH			



Title *SIO1 - Audio Clock VCXOs*			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number vcxo.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:24	Sheet 6 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VCXO.SCH			



Title ***SIO1 - Audio clock PLL Lock Detect***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number vcxolock.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:26	Sheet 10 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VCXOLOCK.SCH			



Title: ***SIO1 - 48k Sample Rate VCXOs***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number: vcxo-48k.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:27	Sheet 7 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VCXO48K.SCH			

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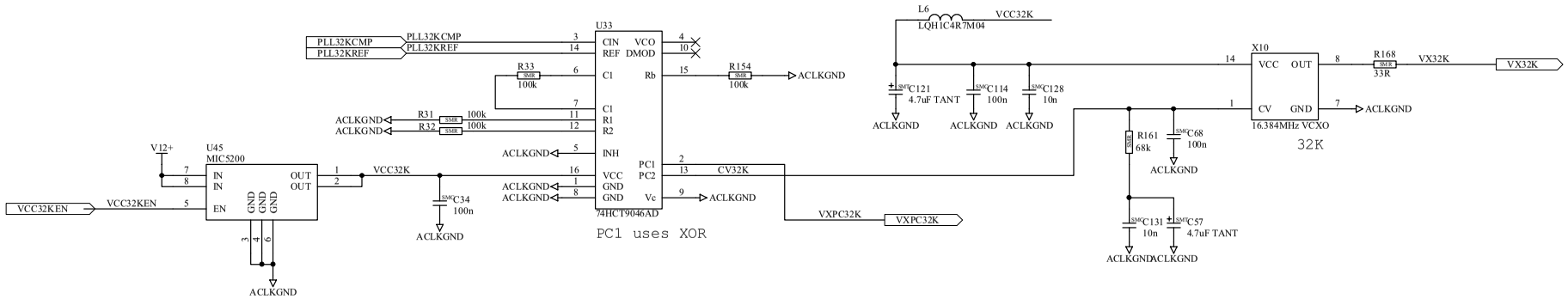
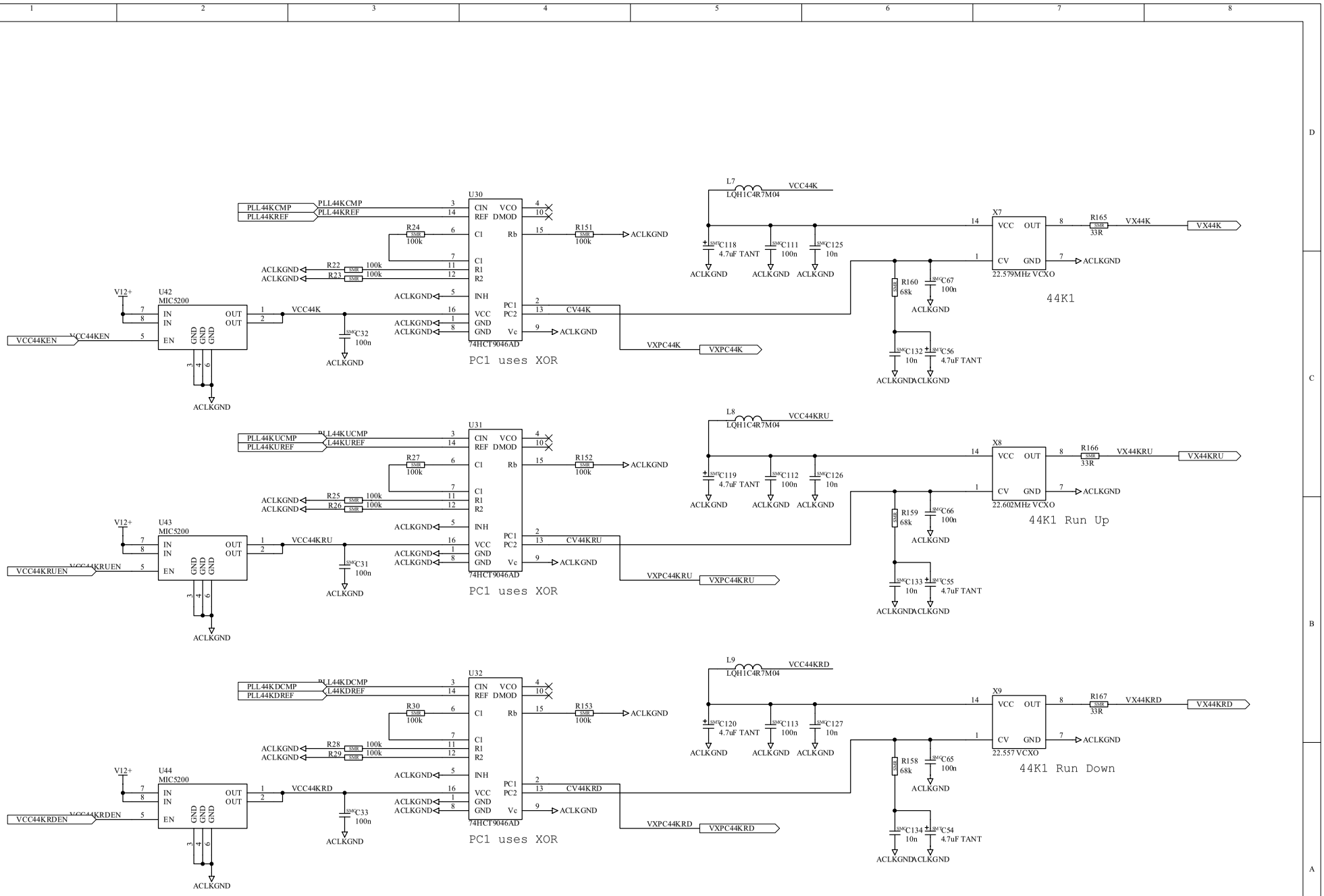


Title *SIO1 - 32k Sample Rate VCXOs*			*Fairlight ESP Pty Ltd*
Size: A3	Numbervcxo32k.sch	Revision: 3.0	*Unit C, 5 Skyline Place*
Date: 11-May-2000 Time: 12:23:28		Sheet9 of 19	*Frenchs Forest*
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VCXO32K.SCH			*NSW*
			Australia 2086



Title: ***SIO1 - 44k1 Sample Rate VCXOs***			*Fairlight ESP Pty Ltd* *Unit C, 5 Skyline Place* *Frenchs Forest* *NSW* *Australia 2086*
Size: A3	Number: vcxo44k.sch	Revision: 3.0	
Date: 11-May-2000 Time: 12:23:29	Sheet 8 of 19		
File: H:\MW4\SIO1\rev3\pcb\protel\Mw4_sio1_r3.DDB - Schematics\VCXO44K.SCH			

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9MW4SIO2 - Auxiliary Sync I/O Card

Terminology

SIO2	MW4-SIO2 sync IO 2 card
PXY	MW4-PXY dual processor card
ECN	Engineering Change Note
IOC1	MW4-IOC1 connector boardcontains all IO connectors and plugs into PXY.

Signal names are in *italics*.

Signal names postfixed with *n* are active low.

1. Introduction

The SIO2 card provides the optional synchronisation features for MW4. SIO2 provides a MIDI interface, a second Sony 9 pin master interface and a Sony 9 pin slave (remote) interface.

2. Functional Description

2.1 Edge Connector (sheet 2)

The edge connector CN1 slots into the PXY card to connect to the IO bus. The power supply is filtered by C2 (10n), L1 (BLM41P600S), C3 (47u) and C1. The inductor L1 straddles the connector to the power plane to suppress any power noise entering or exiting the card. To further reduce EMI and match loading on the PXY IO bus, all signals to the card have 10 Ohm series resistors.

All cards in MW4 have PCB revision and modification level detection via JTAG. U1 has pins 2,3,4,5 hard wired on the PCB to indicate the PCB design revision. SW1 is set to the modification revision number. As modifications are done to the SIO2 card as per ECNs, SW1 should be changed to reflect the modification level. With all switches ON, the modification level is 0. Pins 19,20,21,22 define the card ID (4 for SIO) to allow auto card detection when the system starts.

As the JTAG chain in the system can be quite long, U2 buffers all JTAG signals. U3 and U4 buffer signals to the card to reduce loading on the PXY IO bus. All buffers have internal 25 Ohm resistors which reduce the EMI effects of signal transitions.

2.2 Control (sheet 5)

The Xilinx CPLD at U19 provides the decoding for the SIO2 card.

When *SIO2CSn* is asserted by PXY, U19 uses *A[8..15]* to decode whether the access is to the MIDI serial port (*MIDICSn* asserted) or the Sony 9 pin ports (*NPCSn* asserted). For any access to SIO2, the *SIO2ENn* signal is asserted to enable the data buffer at U4 on sheet 2.

The devices indicate transfer competion by asserting *MIDIDTACKn* (for MIDI acccesses) or *NPDTACKn* (for Sony 9 pin accesses). This in turn asserts *SIO2RDYn* back to PXY.

U19 also has an internal register which reports the cable connected status bits: *MIDIINPRn* (MIDI IN cable present), *BPR* (Sony 9 pin B master cable connected), *RPR* (Sony 9 pin remote cable connected).

The register offsets (based at SIO2):

0000-000F MIDI duart

0100-010F Nine pin duart

0400 read-back control register

bit	value	
0..7		spare

0500 read presence bits

bit	value	
0	*MIDIINPR*	MIDI IN cable present
1	*BPR*	9pin B cable present
2	*RPR*	9pin remote cable present
3..7	0	

0700 revision of CONTROL CPLD

2.3 MIDI Interface (sheet 3)

X1,C4,C5 provide 4MHz to drive the internals of the U5 (68681) serial interface for MIDI transmission. MIDI operates as 8 bits 1 stop bit no parity at 31250 baud. To setup the baud rate the following register settings should be used:

CTUR $= 00_{16}$

CTLR $= 04_{16}$

ACR[6:4] $= 110_{2}$

CSRA $= DD_{16}$

CSRB $= DD_{16}$

MIDI OUT is generated by buffering through U11 inverter and converted to a 5mA current source using U8,R67,R68.

MIDI IN is optically isolated by U7 and protected by D1 and R66. The MIDI IN cable presence detection is provided by U10,R17,R18 by detecting *MIDINp* at +5V (as *MIDINp* would be contect via a 220R resistor to +5V like *MIDOUTp*).

The MIDI IN is rebuffered by U12, R16, U9, R69, R70 like MIDI OUT.

2.4 Sony 9 pin B and Remote (sheet 4)

X2,C6,C7 provide 3.6864MHz to drive the internals of the U5 (68681) serial interface for MIDI transmission. MIDI operates as 8 bits 1 stop bit no parity at 38400 baud.

Serial data to RS422 level for Sony 9 pin by U15,U16,U18 (ADM483E). Note that the Sony 9 pin Remote ports shares the transmit line from the B master port. Only one of Sony B or Remote can be used.

To detect the presence of the Sony 9 pin cables, the *BRXn* (for Sony 9 pin B) and/or *RRXn* (for Sony 9 pin Remote) are checked for being low.

SIO2 Debugging

Introduction

The aim of this document is to accumulate information to help people debug SIO2s. Please edit and add information to this file - it will make your job easier. If you don't know how to edit the file, ask Chris Alfred. Also remember to update the 'Document Revision' above when you do any changes.

Equipment

Digital Multimeter
Digital CRO
ATX power supply
Xilinx JTAG cable (Parallel Cable III, Model:DLC5)
Xilinx JTAG software

PC with serial port program, 2 serial ports and 1 x serial cables (connects to J11 on PXY).

PXY (working) connected to harddisk and with IOC1.

Loopback connectors for IOC1.

Serial cable

DB9 female	10 way IDC
2	5
3	3
5	9

IOC1 Loopback connectors

SONY B,R 9 pin D female

Connect pin 8 to 2.
Connect pin 7 to 3.

MIDI 9 pin D male

Connect pin 2 to 3.
Connect pin 6 to 8.

Programming Files

Contained in zip file 'prog.zip'.

JTAG Connections (on PXY)

Using JP7 for whole chain (uses JP16 for power, JP17 1-2shorted, JP8 shorted)

JP7	3	TDI	JP16	1	Vcc
	5	TDO		2	GND
	7	TMS			
	9	TCK			

1. Initial Debugging Sequence

1. Do all modifications and check.

2. DONT apply power, check none of the power is shorted (+12v, - 12V, Vcc, GND). There should be about 190R between Vcc and GND (without power supply connected); and 1k between 3.3V and GND.

3. Check all power supply voltages at PXY PW1 (voltages are marked on PCB).

4. Check for 40.21MHz at edge connector pin B59.

5. Program CPLDs
   Jumper PXY JP8
   Jumper JP17 1-2
   Connect JTAG cable to JP7 and JP16 (see JTAG Connections)

   Remove any PCI cards from the PXY.

   Start the PXY. When the LEDs light, place a jumper on J5 to hold it in reset.

   Run jtagpgmr.exe
      File:Initialise should show 12 devices
      Load pxy_sio2.cdf and program all devices

6. Remove PXY jumper JP8
   Remove PXY jumper J5.

   Connect test loopback connectors onto IOC1 card (P4 SONYA, P5 SONYB,

7. Boot the PXY from disk.

8. Run SIO2 diagnostics.
   Type:sio2 -d

   On success you should see:

```
control cpld registers
  revision ..... 1
  control ..... PASS
  status ..... 07
midi duart
  ivr ..... PASS
```

```
9pin B/R duart
  ivr ..... PASS
duarts loopback
  TX: B/R  MIDI  RX: B    R    MIDI     (press any key to exit)
     ---- ----      ---- ---- ----
    nn pass pass      pass pass pass
```

nn will be a counting hex number.

3. Common Faults and solutions

The most common faults are:

1. Modification errors
2. Hand soldering errors
3. Missing or wrong components
4. Faulty crystals

Power supply

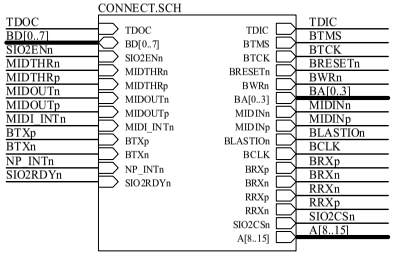
If the impedence between Vcc and GND is low (say 10R), then there is probably an output pin shorted to Vcc (i.e. you are measuring the FET output on impedence).

JTAG chain

If devices are not initialised/programmed
check TCK clocking
check TMS pulses
check chain link
JTAG chain)
check that end of chain is pulled-up

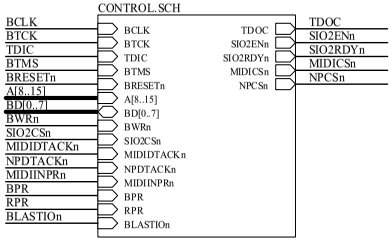
SHEET 2

CONNECT
CONNECT.SCH



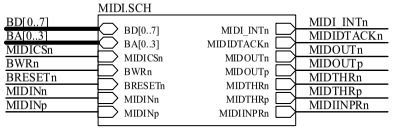
SHEET 5

CONTROL
CONTROL.SCH



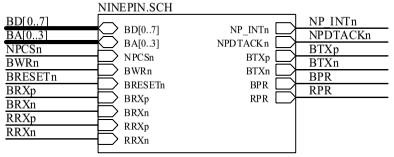
SHEET 3

MIDI
MIDI.SCH

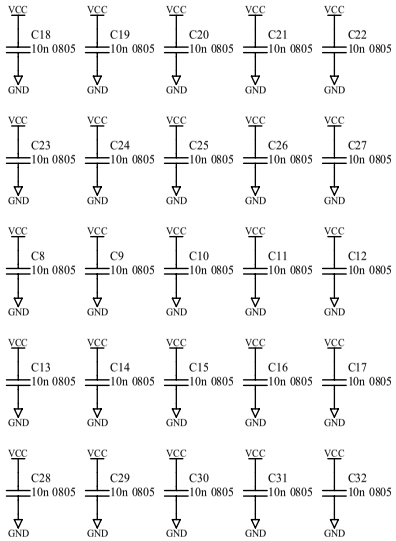


SHEET 4

NINEPIN
NINEPIN.SCH

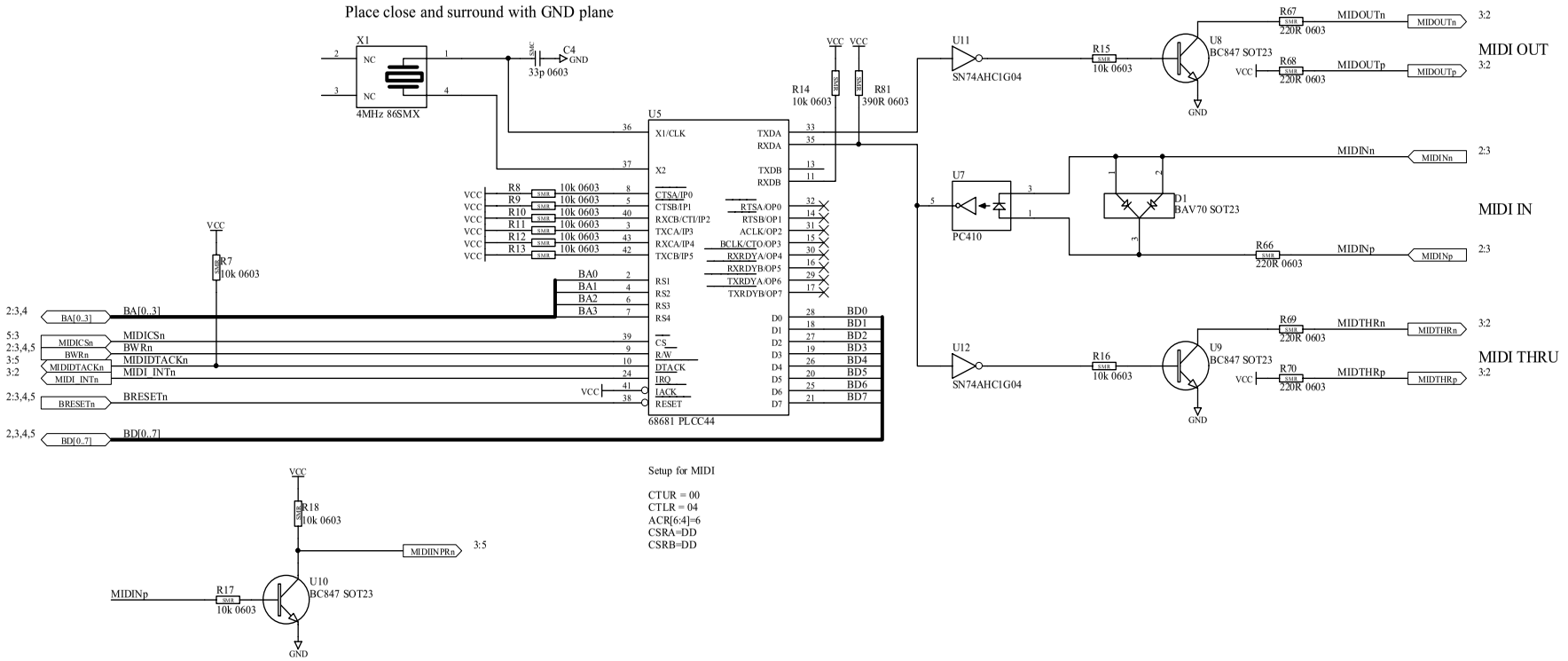


PLACE DECOUPLING CAPACITORS NO FURTHER THAN 1" APART



PCB1

Title	MW4-SIO2 - optional sync section
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Error : FLprotel.BMP file not found.	
Number: mw4-sio2.prj	Revision: 2
Design: Erik de Castro Lopo / Chris Alfred	Date: 25-Aug-2000 Sheet 1 of 5



Rev 2 - removed C5

Title: MW4-SIO2 - midi in and out ports	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: midi.sch	Revision: 2
Design: Chris Alfred	Date: 25-Aug-2000 Sheet 3 of 5

Error : FLprotel.BMP file not found.

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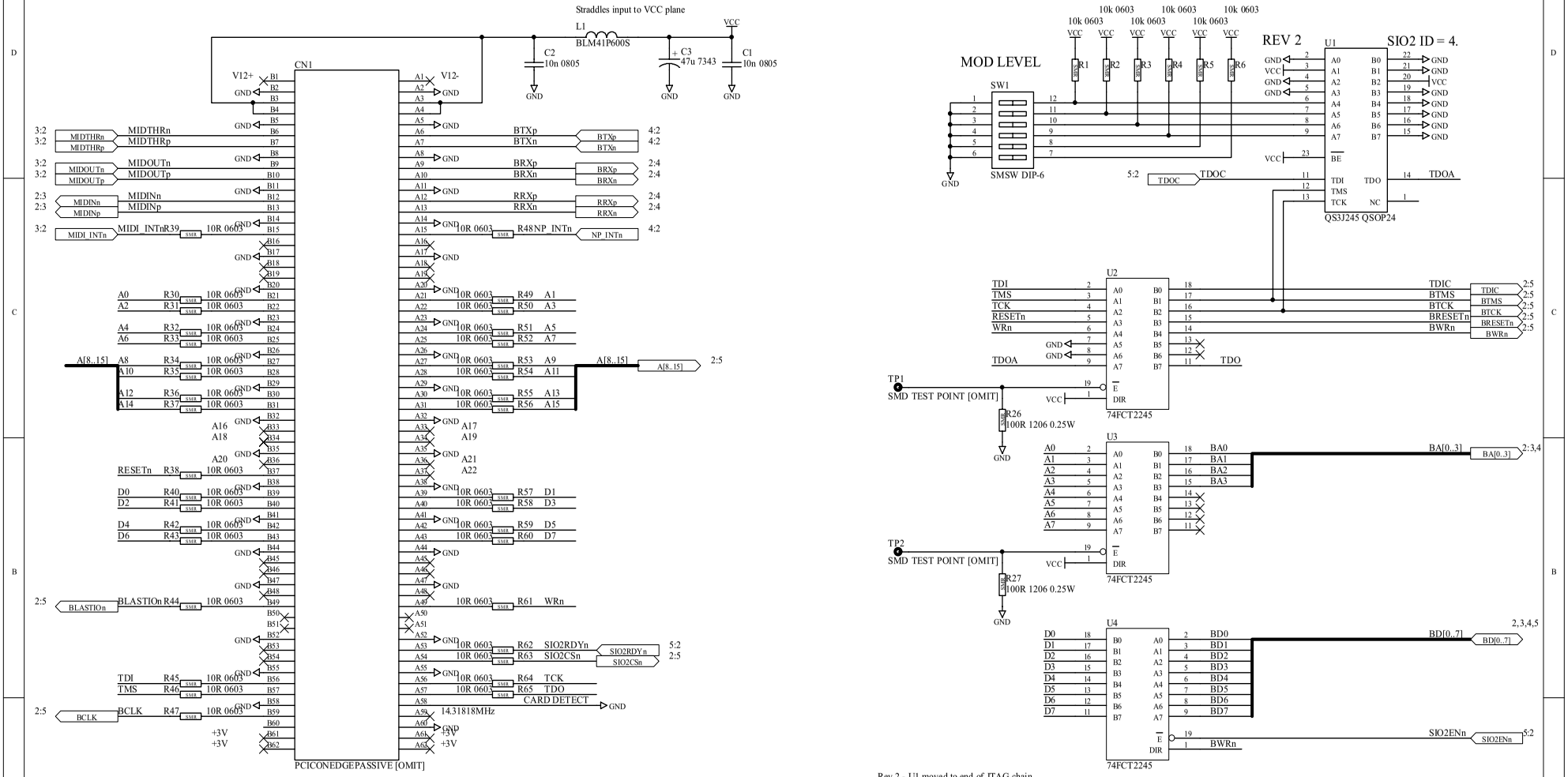

Title	MW4-SIO2 : Edge Connector	Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number:	connect.sch	Revision:	2
Design:	Erik de Castro Lopo	Date:	25-Aug-2000
		Sheet	2 of 5

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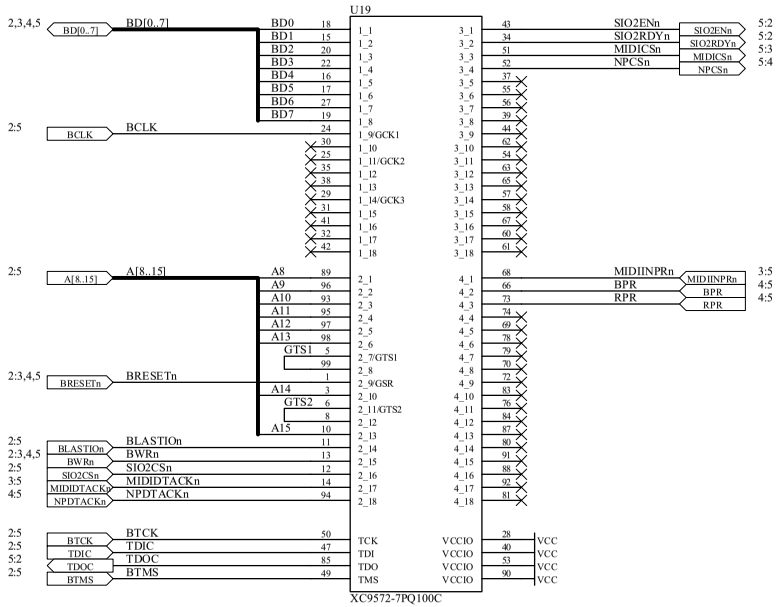

Title	MW4-SIO2 - control
Number:	control.sch
Revision:	2
Design:	Chris Alfred
Date:	25-Aug-2000
Sheet	5 of 5

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Error : FLprotel.BMP file not found.

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Place close and surround with GND plane

X2
3.6864MHz 86SMX
C6 33p 0603
U6
68681 PLCC44
R19 R20 R21 R22 R23 R24 10k 0603
R25 10k 0603
BA[0..3]
NPCSn
BWRn
NPDTACKn
NP_INTn
BRESETn
BD[0..7]

Cable presence detect

U13 SN74AHC1G04
U14 SN74AHC1G04
R79 R80 100k 0603
BPR
RPR
BRXn
RRXn

U16 U15 U18 ADM483EAR
R71 R72 R73 R74 47k 0603
R28 R29 100R 1206 0.25W
BRXp BRXn
BTXp BTXn
RRXp RRXn

USED FOR 9 PIN B AND REMOTE TRANSMIT

Rev 2 - removed C7

Title	MW4-SIO2 - nine pin B and remote
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: ninepin.sch	Revision: 2
Design: Chris Alfred	Date: 25-Aug-2000 Sheet 4 of 5

Error : FLprotel.BMP file not found.

9MW4CG5 - High Speed Graphics Card

Terminology

SRAM	Static RAM
VRAM	Static RAM used for video data
PRAM	Static RAM used for palette data
PXY	PXY Dual Processor Board
CG5	MW4-CG5 Graphics Card
HSSL	High Speed Serial Link for FAME console
OS	Operating System (OS9 for 68xxx)
FPGA	Field Programmable Gate Array (volatile)
CPLD	Complex Programmable Logic Device (non-volatile)
FIFO	First In First Out

1. Introduction

The CG5 graphics card was designed specifically to operate with the PXY dual processor board but also to initially be software compatible with the ESP-CG4 graphics card. Later, new Xilinx programs will be designed to increase the screen resolution from the 512 by 512 pixels of CG3 and CG4 to a new resolution of 1024 by 768 pixels and to increase the number of colour planes from 8 to 11. The document below will refer to 11 colour planes and an 88 bit video data bus even if only 8 planes (64 bit bus) will be used initially.

Included on the CG5 PCB is a HSSL for interfacing with the FAME mixing console. The use of programmable devices in the design allows the CG5 to be 99% software compatible with CG4 initially but also allows later modifications to the existing hardware by changing the configuration data loaded into the two Xilinx devices.

2. Installation

The PXY board has two slots which will accommodate the CG5. These two connectors are marked on the PXY as S3 and S4. Slot S3 should be used in preference to slot S4 which is reserved for later use.

3. General overview

The CG5 receives two clock signals from the PXY. The first is the 40MHz CPU clock, which is used for bus interface and SRAM timing as well as for the HSSL. A second 14.318MHz clock is used to generate the video clocks by use of a phase locked loop (PLL) based clock generator chip.

The rest of the CG5 can be considered as six main functional blocks. The first block (main controller) performs address decoding and handshaking with the processors on PXY. The address control logic block multiplexes addresses from the PXY CPUs with internally generated video address lines to enable addressing of both the VRAM and PRAM as well as generating all video timing signals. The data multiplexer multiplexes the 8 bit CG5 private data bus onto the 88 bit VRAM address bus and combines the 11 video plane data streams to generate an 11 bits per pixel video data bus which feeds the video output block via a high speed synchronous FIFO. The FIFO feeds the 11 bit per pixel video bus through the palette SRAMs to generate a 15 bit TTL colour signal. The last two blocks contain the video SRAM and the HSSL interface.

4. Theory of Operation (Graphics)

The CG5 is a highly specialised video graphics engine with a number of features to allow certain types of images to be displayed more efficiently than would be possible on a generic PC type graphics card. In particular CG5 has dedicated hardware to efficiently generate horizontal, vertical and 45 degree angle lines from software as well as allowing horizontal scrolling areas within static areas. These features are used extensively within the Fairlight disk recorder application.

Most of the complicated logic required to implement the CG5 is contained within two high density FPGA devices; the address control Xilinx (ADDX) and the data multiplexer Xilinx (DATAX). These devices store their configuration data internal to the device using SRAM which must be reloaded after each power up via the CONTROL Xilinx (U21). This operation is performed automatically by the CPU during the OS booting sequence, with the configuration file stored on the Flash ROMs of the PXY or on the machine's hard drive. It is therefore possible to change the operation of the CG5 by changing these configuration files.

During operation, the image on the screen is stored in VRAM. The two FPGAs then read the data out of the VRAM and display it line by line on the screen. In order to change the screen image, the CPUs on the PXY must be allowed to change the data held in the VRAM without interrupting the generation of the screen image. On CG4, video generation (ie the video dot clock) was locked to the speed of the CPU clock (33MHz) which made interleaving of video and CPU access to the VRAM relatively simple.

CG5 however was specified to generate a picture of 1024 by 768 pixels with a refresh rate of 75Hz and thus required special circuitry not present on CG4. This circuitry consists of a programmable clock generator (U20) and a high speed FIFO (U11). The clock generator generates 2 clock signals from the 14.318MHz reference clock. The first clock is the video dot clock which will be set at about 32MHz for 512 by 512 pixel mode or 75-80MHz for 1024 by 768 pixel mode. The second clock frequency is in the 95-98MHz range and is used by the video generation circuitry. During video generation, data is read out of the VRAM using the 40MHz CPU clock but is serialised and loaded into the high speed FIFO on the 95-98MHz FIFO clock. The serialised data is read out of the FIFO using the video dot clock. This scheme allows interleaving of CPU and video access to the video RAM.

The VRAMs are arranged as eleven separate planes (only eight are used in CG4 compatibility mode), five of which have horizontal scrolling capabilities (two in CG4 mode). Ignoring the horizontal scrolling capabilities for the moment, the first pixel on the top line is generated by taking the least significant bit of the byte at address zero of each of the eleven VRAMs and forming an eleven bit wide signal. This signal is fed into the FIFO which feeds the low eleven address lines of the PRAMs; the higher address lines act as palette attribute bits (ie odd line, odd dot, flashing etc), generating at the data output of the PRAMs a value which when fed

through a digital to analog converter produces an analog RGB value for that particular pixel.

The second pixel on the top line is generated using a similar procedure on the second least significant bit of the zeroth byte and so on. The first line of 1025 pixels is therefore generated using the first 128 bytes of the VRAMs, while the second line of pixels is generated using the second 128 bytes etc.

Five of the eleven planes (only two are used in CG4 compatibility mode) are used when horizontal scrolling is required. Scrolling areas within static areas are produced by writing separate data to the scrolling and non-scrolling planes and manipulating the value of the scroll register. For a 1024 by 768 pixel screen, the scroll register can hold a value between zero and 1023, specifying the pixel offset between the static and scrolling data. Video data which one might think would be scrolled off the right hand side of the screen is in fact wrapped around to the left hand side of the screen on the same line. Video data on any line of a scrolling plane should therefore be considered more as a loop of pixels than a line.

Hardware assisted line drawing is performed by use of a screen pixel position register/counter on the CG5. Whenever the CPU directly accesses VRAM, the VRAM address is loaded into the screen position register/counter. By then accessing a special memory area outside the VRAM address map, the pixel at the currently stored location can be accessed, with the current location being modified after the access to move the current location up/down or left/right ready for the next access. The X, Y pixel location is also stored a specific location in the CG5 memory map allowing it to be read from or written to.

The PRAMs perform a mapping from the video data to a particular colour on the screen (specified by the data values stored in the VRAMs). Software which wishes to display particular images on the screen therefore writes data to specific planes of the VRAMs depending upon which colour is to be displayed and the address specifies the location on the screen which is affected. The PRAMs are arranged as two banks of two 128k by 8 bit SRAMs with each bank producing a 15 bit wide signal which is fed into the digital to analog converters. Two banks of SRAM are required to allow adjacent pixels to be created using different banks and hence slowing down access to the PRAM to an acceptable rate.

5. Detailed Description

5.1 PXY Edge Connector

(see connect.sch)

This schematic contains the PCI style connector (the pinout is NOT the standard PCI pinout), the address and data bus buffers (U29, U30), the JTAG download port buffer and the JTAG card identifier chip (U26). The JTAG identifier chip allows the CPU on PXY to identify the card and revision number of the CG5. The DIP switch SW1 allows setting of modification level. Most signals entering or leaving the CG5 have a 10 ohm series termination resistor.

5.2 Clock Generators

(see clock.sch)

The 40MHz PXY clock is buffered by U3 with a separate buffer output to drive each of the FPGAs and CPLDs. The video and FIFO clocks are generated from the 14.318MHz clock supplied by the PXY by use of the programmable clock generator at U20. This clock generator

chip is programmed from the CONTROL CPLD (U21) using a two pin serial protocol.

5.3 Control Xilinx (CPLD)

(see control.sch)

The control Xilinx (CONTROL, U21) is a non-volatile CPLD which performs address decoding as well as generating handshaking signals for communicating with the PXY, control logic to drive the address/data buffers and programming interfaces for the programmable clock generator (U20) and the SRAM based FPGAs.

When doing address decoding, the CONTROL Xilinx splits the CG5 address space into the following address areas ; CONTROL Xilinx register area, the ADDX register area (AXREG signal is asserted low), DATAX register area (DXREG asserted low), VRAM access (VRAMACC asserted low) and VRAM auto-increment access (AIACC asserted low).

5.4 Address Control Xilinx

(see addx.sch)

The address Xilinx (ADDX, U22) multiplexes the CPU address bus with its own internally generated addresses (used for video generation) onto video RAMs. In the process it carries out the following four main functions:

1) Perform address decoding; to allow the CPU access to VRAM and control registers internal to ADDX and to generate appropriate read/write signals for the VRAMs and PRAMs.

2) To synchronise with the data multiplexer Xilinx U12 (DATAX) (datax.sch), generate the video synchronisation signals (VSYNC, HSYNC, BLANK) and generate addresses for stepping through VRAM while generating the video output data.

3) To allow CPU access to the VRAM when it is not being used for video generation.

4) To disable video generation (PALENn driven LOW) and allow CPU access to the PRAMs.

Input addresses are supplied to ADDX via a 19 bit address bus BA[0..18]. These address signals are multiplexed inside ADDX with internally generated video access addresses to provide the VRAM address signals XA[0..16], so that during CPU accesses BA[0..16] are fed directly to XA[0..16] whilst during video generation accesses, internally generated addresses drive XA[0..16]. In addition scrolling address lines XSA[0..6] are generated by adding (ignoring any carry which may be generated) the value of a horizontal scroll register (internal to ADDX) to XA[0..6] to produce the scrolling address lines XSA[0..6].

During CPU access to VRAM, ADDX generates the handshaking signal required by the DATAX Xilinx (PALEN, BYTEMODE, BITMASK, VDATATS, BS[0..2] and HS[0..2]) and the appropriate output enable and write signals for the VRAMs (RAMOEn and RAMWRn). In addition to controls for the bus switches (PALOEn and PALEN), individual output enables (PENn[0..3]) and write (PWRn[0..3]) signals are generated for accessing the PRAMs.

Control registers internal to ADDX may be accessed from software via the 8 bit data bus PD[0..7]. The address of these internal registers may change when the configuration file for ADDX is changed to modify existing features or add new features.

ADDX also generates a number of clock signals from its DOTCLK input. VDOTCLK and FDOTCLK are the same frequency as DOTCLK and are used to drive the video generator CPLD (VIDEO, U13) and the high speed synchronous FIFO read operation (see next section). Using separate output clock signals allows more control over clock phase (inverted or not inverted) as well as improving signal integrity by restricting each clock signal to one source and one destination. Other clock signals of this type are PALCLKA and PALCLKB which are anti-phase versions of a clock running at half the frequency of VDOTCLK.

Other signals of interest are the bit select lines BS[0..2] and BYTEMODE which are generated by ADDX for CPU access to the VRAMs. When BYTEMODE is HIGH VRAM is accessed in bytes of eight contiguous pixels while when it is LOW a single pixel within the byte (ie eight consecutive pixels) is accessed depending on the value of the three bit select lines.

5.5 Data Multiplexer and High Speed FIFO

(see datax.sch)

The data multiplexer Xilinx (DATAX, U12) sits between the 8 bit CG5 data bus PD[0..7] and the 88 bit graphics data bus which is arranged as eleven groups of 8 bits: DA[0..7], DB[0..7], DC[0..7], DD[0..7], DE[0..7], DF[0..7], DV[0..7], DW[0..7], DX[0..7], DY[0..7] and DZ[0..7]. DATAX contains an internal set of registers which drive the VRAM enable signals PDA[0..10], specifying which VRAM planes are accessed during a CPU read or write.

For a CPU byte write operation, the data arrives at the 8 bit data port PD[0..7], is manipulated internally depending on the value of internal registers and is then placed on the eleven 8 bit data buses Dx[0..7]. For byte read operations data arrives via the eleven 8 bit data buses is combined internally to DATAX to generate an 8 bit output which is driven onto PD[0..8]. When writing to a particular bit within a byte (BYTEMODE is LOW), DATAX must first read the full byte from the eleven 8 bit buses, modify the correct bit internally and then write the modified data back onto the eleven 8 bit buses.

During video generation data is read from the VRAMs via the eleven 8 bit data buses (all of the planes are enabled) and loaded into a set of internal shift registers. The 88 bits read in this operation contains the data from all eleven planes for the display of eight consecutive pixels. The data values for the eight consecutive pixels are then clocked out of DATAX to the high speed synchronous FIFO U11 via the FD[0..11] over the following eight cycles of the 95-98MHz FIFO write clock FIFOWCLK. During this time, DATAX asserts the FIFO write signal FIFOWRn. Data is clocked out of the high speed FIFO on the slower 32-80MHz FDOTCLK whenever ADDX asserts the FIFO read enable signal FIFOREn. The FIFO status signals (FIFOHFn, FIFOEMn FIFOFLn, FIFOAEn and FIFOAFn) are fed back to ADDX which controls the whole process.

5.6 Video RAM

(see vram.sch)

The eleven SRAMs which make up the VRAM bank are 128kbyte by 8 bit devices. This size allows screen image of up to 1024 by 1024 pixels but to make CG5 comply with SVGA video monitor standards a screen image of 1024 by 768 pixels will be used.

The VRAM chips share common output enable and write signals, RAMOEn and RAMWRn. Address lines generated by ADDX (XA[0..16] and XSA[0..6]) specify VRAM addresses, with only the VRAMs associated with the scrolling planes being connected to the scrolling address lines XSA[0..6].

Each VRAM chip has its own enable signal, one of the PDA[0..10] lines, which allow individual VRAMs to be accessed even though they share common output enable and write signals. In addition, each VRAM has its own data bus which connects only to DATAX; one of the buses DA[0..7], DB[0..7], DC[0..7], DD[0..7], DE[0..7], DF[0..7], DV[0..7], DW[0..7], DX[0..7], DY[0..7] and DZ[0..7].

5.7 Palette

(see palette.sch)

The video palette consists for two palette RAMs U1 and U2, and the associated chips on this schematic. During video generation (PALENn is high and PALMOD is low) the serialised video data is fed into the D inputs of U10 where it is latched. The outputs of the latch at U10 is fed into the address lines of the two palette RAMs U1 and U2 and the data coming out of the PRAM data lines VDA[0..15] is the colour data which is eventually fed into the three D-A converters to produce analogue signals for red, green and blue.

To change the colour values, video generation must be turned off (indicated by PALENn being low and PALMOD being high) which allows the address and data bus to be accessed from the PXY CPU via U8 and U9 respectively. The sixteen bit wide palette data bus is read from and written to with separate 8 bit accesses controlled by the enable signals PENn[0..1] and the palette write signals PWRn[0..1].

5.8 Video Generation

(see video.sch)

During video generation, the data from the PRAMs is fed into the VIDEO CPLD at U13 and then into the D-A which is built around the diodes, resistors and transistors on the right hand side of this schematic. The horizontal and vertical synch signal are buffered by the drivers constructed out of Q4, Q5, Q6 and Q7.

5.9 High Speed Serial Link (HSSL) Interface

(see hssl.sch)

The HSSL interface is a 1Mbit bi-directional full-duplex serial link with hardware handshaking designed specifically to interface with the Amek console used in FAME systems. All signals are transmitted over the HSSL cable in differential mode using a driver on the IOC board. The HSSL cable carries data, clock and write signals as well as a receiver FIFO full signal, which is used in the transmitter control logic to hold off or halt transmission until there is room in the receiver's FIFO for another byte of data.

All of the HSSL control and CPU interfacing hardware is located in a HSSL CPLD (U24). Any CPU write to or read from the HSSL begins a HSSL specific transfer start signal, HSSLCSn, being generated on the PXY. When the read or write operation is finished, the CPLD send the signal HSSLRDYn back to the PXY. The internals of HSSL includes a read only status register and a read/write control register.

To transmit a character on the HSSL, the CPU must first check the status register inside HSSL CPLD, to ensure that the transmitter FIFO's (U23) FIFO full flag is not asserted. If everything is OK, it may write a byte to the transmitter, with the 8 data bits being transferred from the CPU

via the 8 least significant bits of the CPU data bus and the write signal for the FIFO being generating by HSSL CPLD. Whenever the transmit FIFO is not empty and the other end's receiver is not full (ie RCVFFn is HIGH), the CPLD will load a byte from the transmit FIFO into an internal shift register and shift the data out serially (at 1/16th of the 20mhz clock) driving the data and clock signals XMTDAT and XMTCLKn. At the end of the byte transfer the CPLD asserts the serial write signal XMTWRn.

Serial data is received from the differential receivers on the IOC board which drives the signals RCVDAT, RCVCLKn and RCVWRn. RCVCLKn shifts the serial data RCVDAT into a shift register inside the CPLD with a parallel output RD[0..7]. At the end of eight bits of data, the full transferred data byte exists on RD[0..7] and signal RCVWRn from the transmitter writes the byte into the receiver FIFO U28.

If there is data in the receive FIFO, a bit of the status register in HSSL CPLD is set and optionally an interrupt (HRXINTn) can be generated. When the CPU reads data from the receive FIFO, the CPLD generates the FIFO read signal *MRRD and the data is transferred over the least significant 8 bits of the CPU data bus D[0..31].

6. Programming the Xilinx CPLD Devices

*** This section still not complete ***

Both Lattice devices may be programmed by connecting a special download cable from a PC to JP8 of the PXY, while the CG5 is attached to the PXY and power is ON. See [3].

7. Testing and Diagnostics

*** This section is still not complete ***

Two OS-9 programs have been written to test the operation (CG5TEST) and diagnose faults (CG5DIAG) in the CG5. Both programs must be run with DIP switch #2 of the PXY ON and a PC connected to the serial port JP1 of the PXY so that all I/O can be viewed on the screen of the PC while testing is being carried out. In addition, when running CG5DIAG, DIP switch #3 must also be on to disable the 68040's Memory Management Unit.

Additional References

[1] Chris Alfred, Motorola MC68040 operation, Fairlight ESP.

[2] Motorola, MC68040 32 bit Microprocessor User's Manual.

[3] Chris Alfred, ESP-PXY Waveform Executive Functional Description, Fairlight ESP.

[4] Lattice Semiconductor, Lattice Data Book 1994.

[5] Xilinx, The Programmable Logic Data Book 1994.

[6] Fairlight ESP, CDIAG v3.0.

9MW4QDC - QDC Digital Channel Card

1. General Description

The PCB assembly MW4-QDC is the DSP engine of the QDC Technology architecture. As such it is the successor to ESP-DCC and performs a similar function in the MFX 48, Prodigy 2 and FAME 2 systems. It is designed to be largely compatible to ESP-DCC from a functional and software point of view, at the same time providing significantly increased capabilities for future expansion.

The name QDC "Quad Digital Channel" refers to the fact that MW4-QDC consists of four identical sections, each of which corresponds more or less to a single ESP-DCC. The name could also be interpreted as "Quad DSP Card", but this is not strictly correct since there may be up to 8 DSPs per card.

It is anticipated that depopulated QDC assemblies may be built with fewer than four sections and/or fewer than eight DSPs installed if this proves to be useful.

1.1 I/O Capabilities

MW4-QDC has connectors for six I/O mezzanine cards, which plug onto and lay parallel to the main QDC PCB. These cards provide for analog and digital I/O. There are two positions available for each of three different I/O card types:

- AI-1, which provides 8 analog inputs
- AO-1, which provides 8 analog outputs
- AES-1, which provides 4 stereo digital (AES) inputs and 4 stereo digital (AES) outputs

Thus, in the normal fully loaded configuration each QDC plus I/O cards provides 16 analog ins, 16 analog outs, 8 stereo digital ins and 8 stereo digital outs.

The I/O connectors for the AES-1 and AO-1 cards are identical, which allows these cards to be interchanged as required. However use of a mezzanine card in the position normally reserved for the other will require special external I/O cabling to deal with the resulting changed pinout on the 50pin sub-D connectors.

Typically, one or both of the analog output cards (AO-1) will be replaced by digital I/O cards (AES-1), increasing the digital I/O capability up to 16 stereo in + 16 stereo out.

The maximum possible I/O capability is achieved with four AES-1 cards (configuration C in table 1).
If the analog input card (AI-1) is also fitted in this configuration then there are total of 48 (mono) input channels, of which any 32 (with certain restrictions) can be used simultaneously.

	Number of I/O Cards			Analog		Digital (mono/		Total I/O (mono)	
config	AI-1	AO-1	AES-1	Inputs	Outputs	Inputs	Outputs	Inputs	Outputs
A	2	2	2	16	16	16/8	16/8	32	32
B	2	1	3	16	8	24/12	24/12	40/32	32
C	2	0	4	16	0	32/16	32/16	48/32	32
D	2	3	1	16	24	8/4	8/4	24	32
E	2	4	0	16	32	0	0	16	32

A: standard configuration
B,C: additional digital I/O
D,E: additional analog outputs

Table 1. QDC I/O Configurations

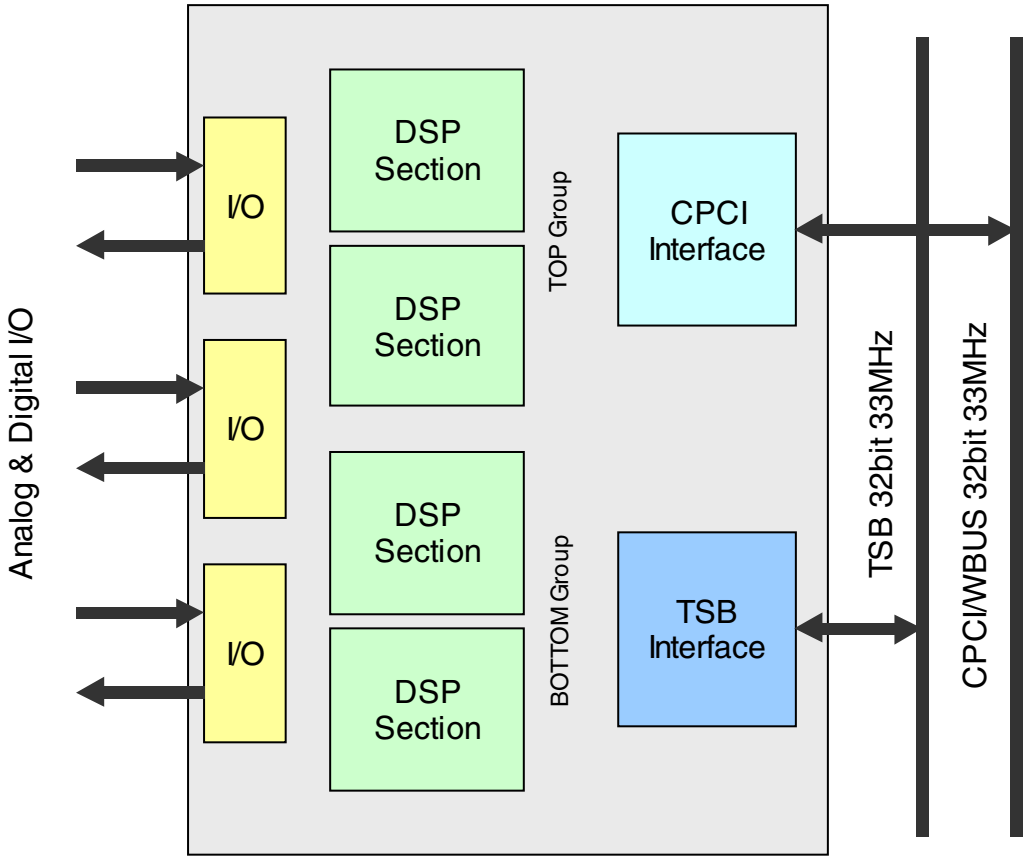


Fig. 1. QDC Basic Blocks

2. Functional Description

2.1 DSP Groups

The four identical DSP Sections can be viewed as two groups each consisting of two sections. The groups are referred to as the "top" and "bottom" groups for obvious reasons (see fig 2). Within each group the sections are referred to as the "left" and "right" sections. In a depopulated board the Top group must always be present and within a depopulated group the Left section must always be present.

Associated with each group is one I/O slot for each of the three I/O assemblies AI-1, AO-1 and AES-1. An input routing matrix is provided which maps the physical inputs to any of the DSP inputs within that group. Outputs have a fixed correspondence between physical outputs and DSP outputs (see figs. 3,4).

2.2 PCI Interface

The Waveform Buss of the MFX3 system has been replaced by a PCI Buss using the industry standard Compact-PCI (CPCI) mechanical format. This is a 32bit synchronous buss running at a clock speed of [up to] 33MHz, providing a maximum throughput in burst mode of nearly 133MB/s.

The PCI interface on the QDC operates in slave only mode and supports zero wait state write bursts to DRAM and one wait state read bursts from DRAM. Accesses to the internal I/O buss (XBUS) incur more wait states and do not support burst mode.

2.3 TSB Interface

For transmission of audio samples between QDCs and between the individual sections of a single QDC a separate buss referred to as the TSB (Time-Sliced-Buss) is provided. This is a 32 bit buss dedicated to a broadcast mode of operation whereby one device transmits data which is received simultaneously by all other devices on the buss. The external interface to the TSB uses a protocol which is electrically identical to the PCI buss and which has a transfer cycle time of 30ns (33MHz).

The TSB uses a TDM (time-division multiplexing) technique to provide multiple data channels within a sample period. At a sample rate of 48k approximately 680 channels are available.

2.4 DSP Section:

Each DSP section is an independent computational unit containing two Analog Devices 21061L SHARC DSPs running at 40MHz. The SHARC executes one instruction per clock cycle and can achieve a computational throughput of up to 120MFLOPs. Each DSP component has 1Mbit of high speed SRAM on-chip which is used for program and data storage.

The two DSPs share a common buss which is used to access a number of external subsystems within the DSP section:

- 3Mbit Static RAM for additional program and data storage
- 2Mbit Flash ROM which holds the initial program executed by the DSP on startup
- up to 64MB DRAM (Waveform RAM), dual-ported to CPCI buss
- TSB Interface supporting up to 1024 channels.

Each DSP has two serial inputs and two serial outputs, which provide for the transmission of audio data to and from the I/O cards. Each serial line carries a stereo pair of audio data.

2.5 XBUS

XBUS is an internal control buss which provides access to various functions such as:

a) configuration of TSB controller
b) configuration of audio I/O
c) interrupt handling to/from DSP sections
d) access to LED display for each DSP section
e) buss access to I/O mezzanine cards

The XBUS has a data buss width of up to 10 bits; most peripherals will use the lower 8 bits as a byte-wide data path.

2.6 Audio I/O

External I/O is provided by three 50 pin sub-D connectors at the left side of the PCB. The top and bottom connectors are wired identically and each provide 8 analog inputs and 8 analog outputs. The middle connector provides 8 digital inputs and 8 digital outputs.

Each I/O mezzanine card is supported by two connectors at the left and right sides of the board. The left hand connectors are wired directly to the external I/O connectors, the right hand connectors carry sample clocks, serial data to the DSPs and the XBUS. Transmission of audio data between the I/O cards and DSPs uses the industry standard I2S format.

2.7 Audio Clocks

Sample synchronisation is derived from master sample clocks generated by PXY and transmitted over the backplane to QDC. There are two master sample clocks, referred to as MCLK (master) and ACLK (auxiliary), each of which consists of two signals, one running at the sample rate (Fs) and one at 256*Fs:

master clock:	MCLKL	Fs
	MCLKH	256*Fs
aux. master clock:	ACLKL	Fs (alt)
	ACLKH	256*Fs (alt)

The low speed clock (Fs) is also referred to as the word clock. A sample period begins with the rising edge of the master word clock.
The high speed clocks (256*Fs) are buffered and distributed to the I/O cards for use by converters and transceivers. For the serial transmission of audio data QDC generates a bit

clock at 64*Fs and a framing signal corresponding to the I2S serial format for use by the I/O cards and DSPs.

The master clock (MCLK) is used for all system timing and DSP sample synchronisation. ACLK is provided for special functions such as output sample rate conversion.

Provision is also made for a sample clock derived from an AES input to be transmitted back to PXY for use as a master clock reference.

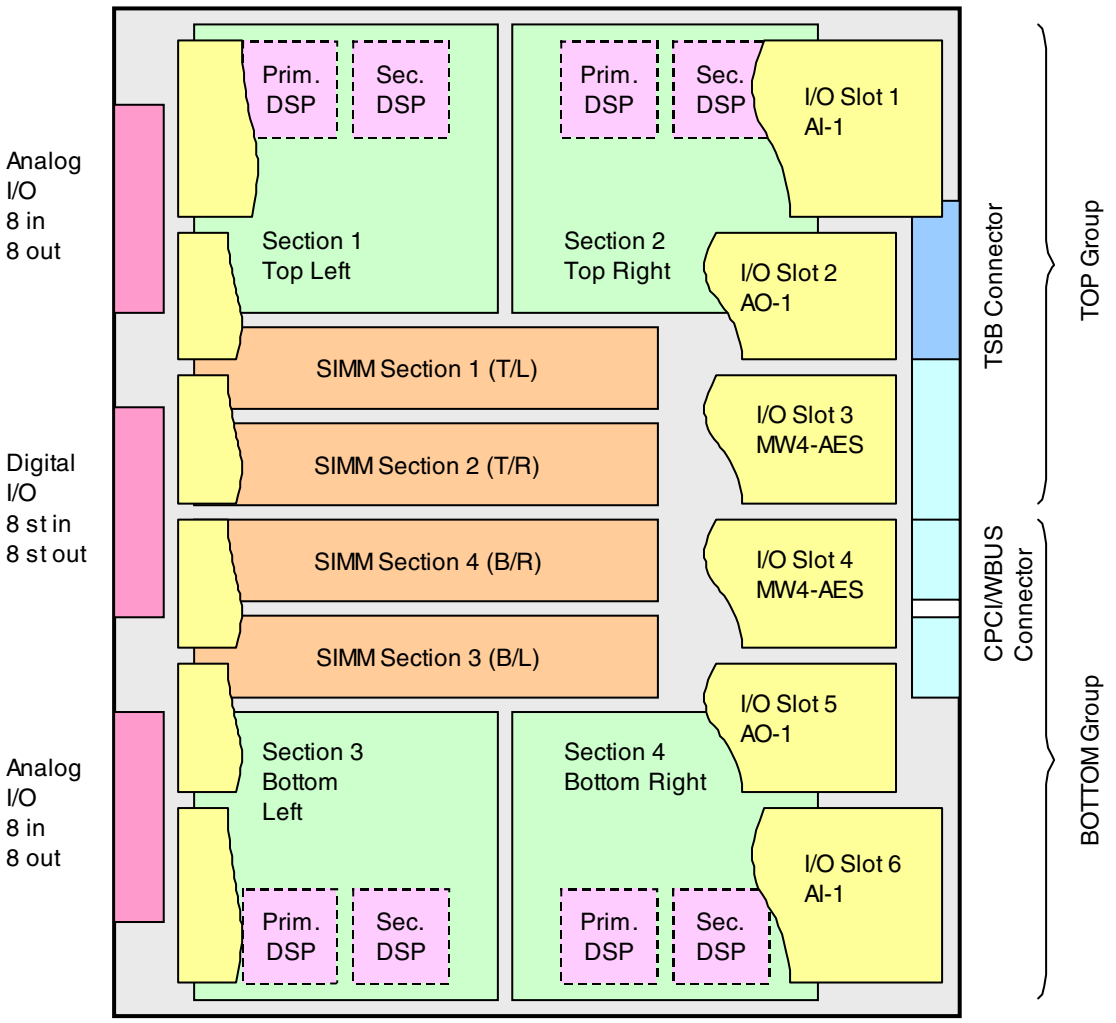


Fig. 2. QDC PCB Mechanical Layout / Functional Blocks (Top view)

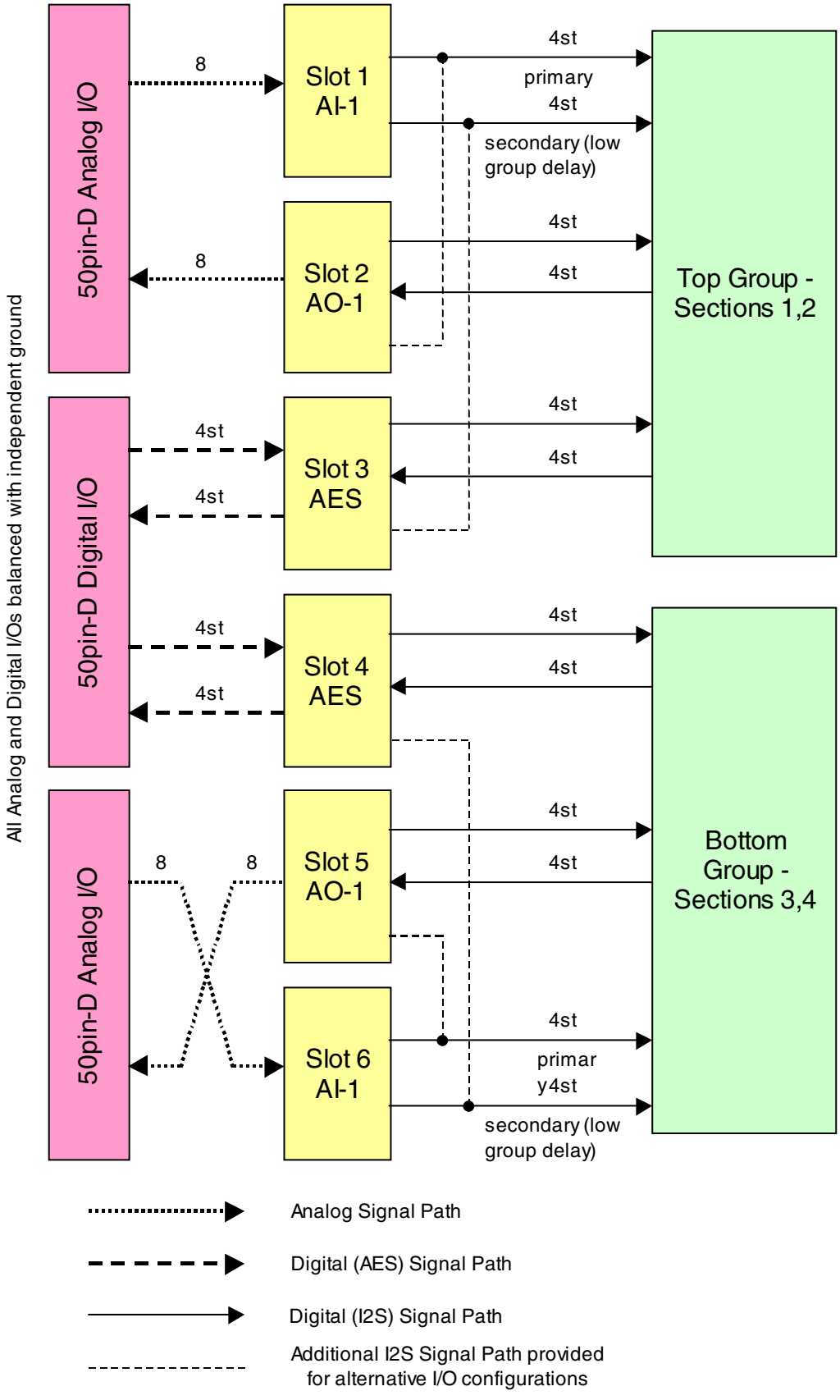


Fig. 3. QDC Audio I/O Architecture

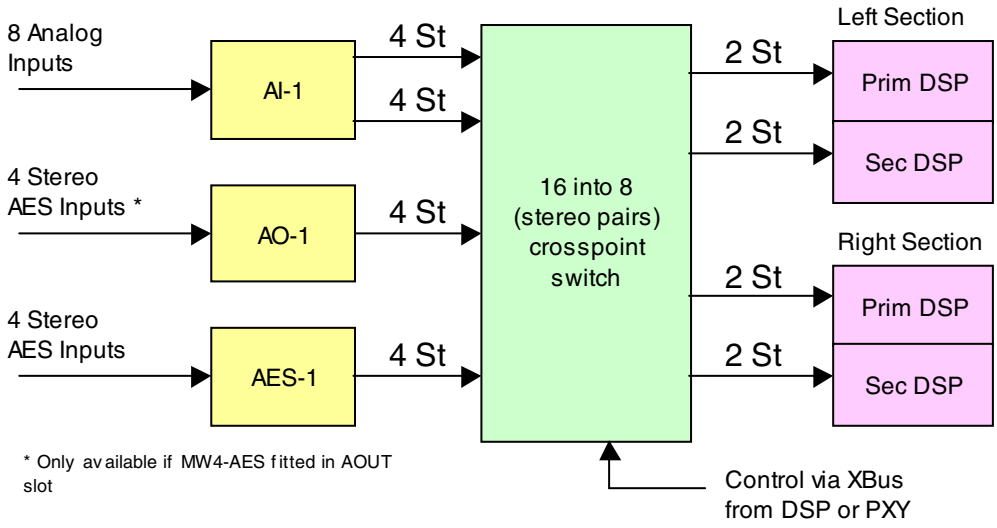


Fig. 4a. QDC Input Flow for one of two (Top/Bottom) Groups

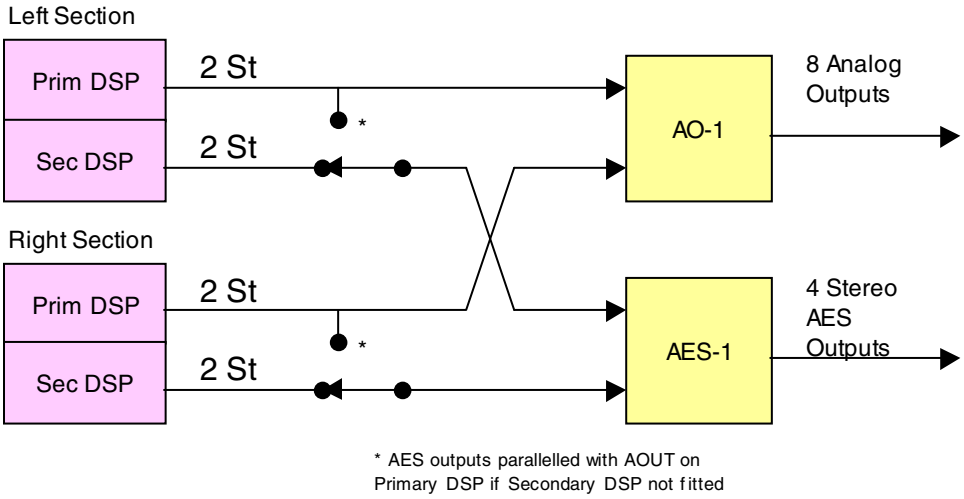


Fig. 4b. QDC Output Flow for one of two (Top/Bottom) Groups

3. More Details

3.1 Technology

The QDC consists almost entirely of 3.3v surface mount technology. The only 5v components are the DRAM SIMMs and the Bus switch (Quickswitch) parts. No special interface components are required because most of the 3.3v logic devices are also 5v tolerant. However it should be noted that the 3v SHARC DSPs do not have 5v tolerant inputs.
No assumptions are made about the I/O mezzanine boards, which may use either 3v or 5v logic.

3.2 PCI Interface & XBUS Controller

The PCI and XBUS controllers operate in conjunction with the DRAM controllers in each DSP section to provide a multipath buss supporting four distinct modes of operation:

a) PCI access to DRAM
b) PCI access to XBUS
c) PCI access to DSP host port
d) DSP access to XBUS

In addition each DSP section may access its own DRAM independently of the above, subject to arbitration for PCI accesses to the DRAM.
In general, it is expected that access types (c) and (d) will be very infrequent, as these will obviously cause buss contention problems if used very often.

Arbitration functions are distributed between the PCI, XBUS and DRAM controllers.

The PCI Interface is implemented using a Xilinx XC95288XL CPLD, the XBUS interface uses an XCS-10XL FPGA part.

3.3 TSB Interface

Access to the TSB is provided to each DSP section via a dual-port static RAM (DPRAM). The DPRAM effectively contains an image of the TSB data channels, with each data channel occupying one address in the DPRAM. At the beginning of a sample period the TSB address (channel) counter is reset to zero and is then incremented on each rising edge of the TSB clock.

The TSB clock and reset signal are generated by a central TSB master controller which is located on PXY. Each device on the TSB is assigned a range of channels during which it will transmit its data. During this time data is read from the DPRAM and driven onto the TSB data buss. Whenever a device is not transmitting data it is receiving data from the TSB and writing it to DPRAM. It is up to the software configuring each TSB device to ensure than only one device is transmitting at a given time.

The overall effect of this architecture is that at the end of a sample period the TSB images of all devices on the TSB contain the same data, thus providing a very high bandwidth data sharing mechanism.

To ensure data integrity the TSB interface on QDC implements three data "pages" for the TSB channel data. The TSB hardware cycles through these three pages in consecutive sample periods, so that during any given sample period one page is used for receiving and

transmitting data. The other two pages may be read and written by the DSP without any risk of data contention or race conditions.

3.4 DSP Section:

Each DSP section is an independent computational unit consisting of :-

- 2 SHARC DSPs 21061L at 40MHz
- 64K x 48bit SRAM operating at zero wait states
- 256K x 8bit 120ns Flash
- 4K x 32bit SRAM, Dual Ported to TSB
- 512K - 16M x 32bit EDO DRAM, dual ported to CPCI

3.4.1 Dual DSP

The two SHARC 21061 DSPs share a common buss. Buss arbitration logic is built into the DSP. The primary DSP has an ID of 1, the secondary ID 2. The secondary DSP may be omitted for depopulated boards, in which case the fitting of some other components must also be changed.

The primary DSP is configured to boot from Flash ROM after restart, the secondary DSP is configured for host boot mode and is bootstrapped by the primary DSP.

In addition, the primary DSP of the left section of each group is responsible for programming the DSP Support FPGA (QDC-SUPP), and the top left primary DSP for programming the XBUS Control FPGA (QDC-XBUS) as well.

Programming of the Xilinx FPGA parts is done using the DSP flag outputs; after configuration the flag lines take on their normal functions.

3.4.2 Static RAM

Normally the DSPs execute programs and load data from their internal RAM, which avoids accesses to the shared external buss and possible delays due to buss arbitration. The external static RAM is intended for data storage for algorithms (eg large FFTs) which do not fit in the internal RAM. If this is not required boards can be built without the external SRAM or with smaller parts (16K x 48) or reduced data width (32 bit). Accesses to SRAM incur no wait states.

3.4.3 Flash ROM

The Flash ROM holds the bootstrap program for the primary DSP and the data for programming the Xilinx FPGAs. In addition diagnostic software for use in standalone mode may be stored in the Flash.

3.4.4 DSP interface to TSB

The interface to the TSB includes an address mapping RAM which allows the DSP to access TSB slots in an arbitrary sequence without using indirection (which the SHARC is not very good at). All accesses to the TSB RAM (DPRAM) have a delayed address pipeline, which means that the actual address used by an access (read or write) is the address supplied by the previous access (see fig 7).

This means that only one logical process may access the TSB; however this is not normally a problem since TSB access must be synchronised to the sample clock and are therefore generally performed only in an interrupt routine.

The mapping RAM (MAPRAM) provides 16K logical channels each of which contains the address of one of the 1024 physical TSB channels. The TSB page to be accessed is not mapped, but specified directly in the address from the DSP; however the MAPRAM may specify a page offset ("next page" or "previous page").

Accesses to the TSB or MAPRAM incur no wait states on READ, but one wait state on WRITE.

3.4.5 DSP DRAM Interface

3.4.6 DSP Support FPGA

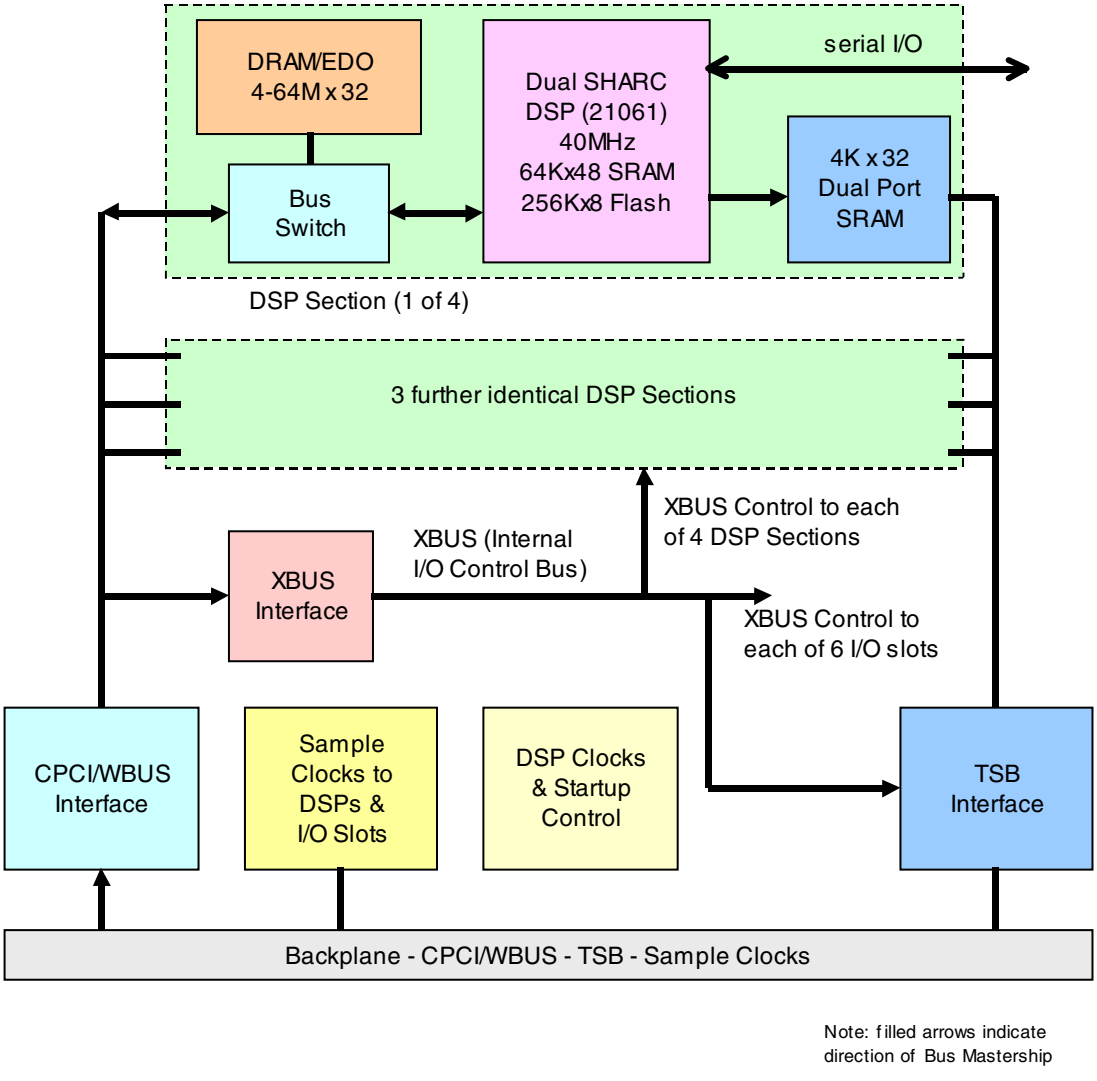
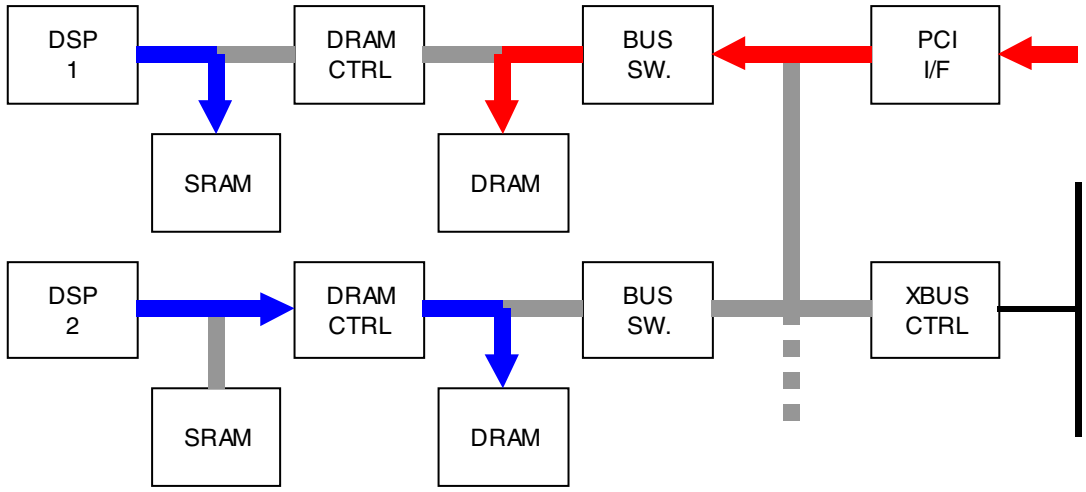
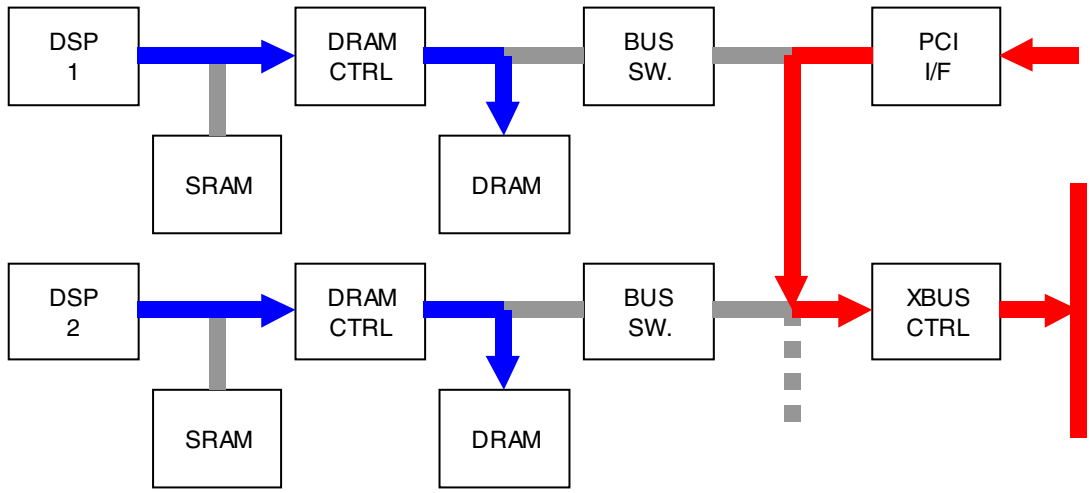


Fig. 5. QDC Functional Architecture



PCI Access to DRAM Section 1
DSP 1 accessing SRAM
DSP 2 accessing DRAM

Fig. 6a. QDC PCI/XBUS/DSP Data Paths



PCI Access to XBUS
DSP 1 accessing DRAM
DSP 2 accessing DRAM

Fig. 6b. QDC PCI/XBUS/DSP Data Paths

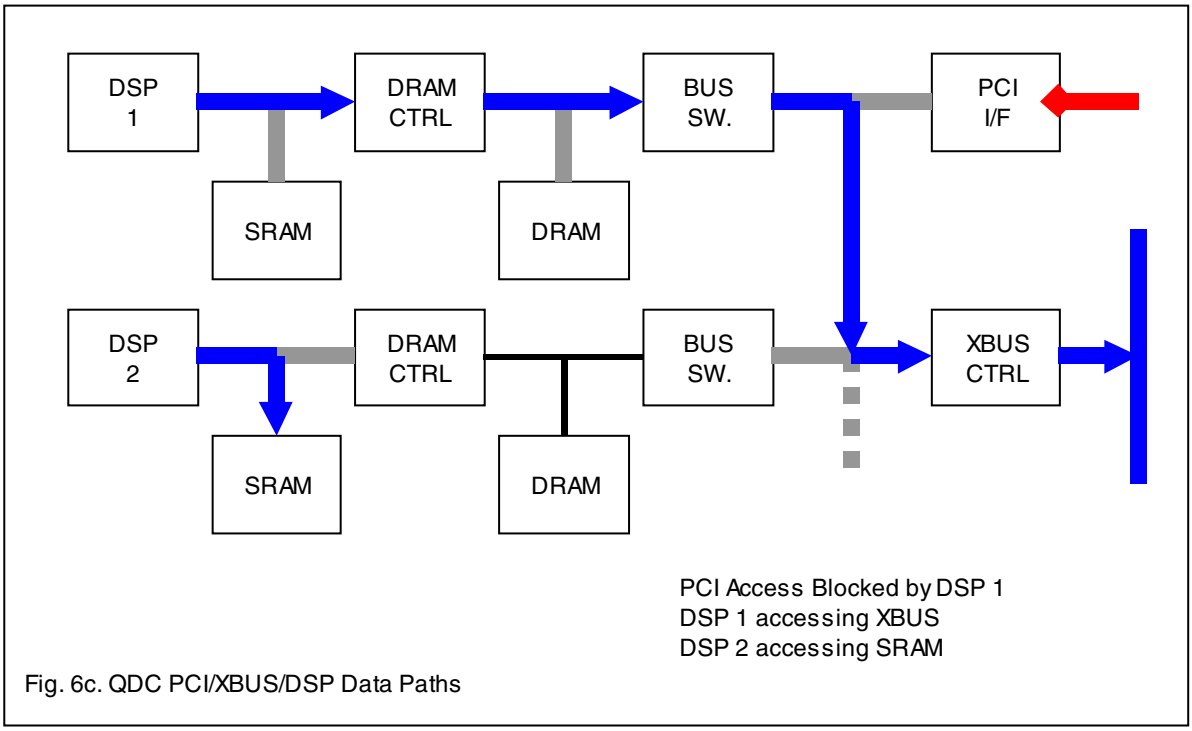


Fig. 6c. QDC PCI/XBUS/DSP Data Paths

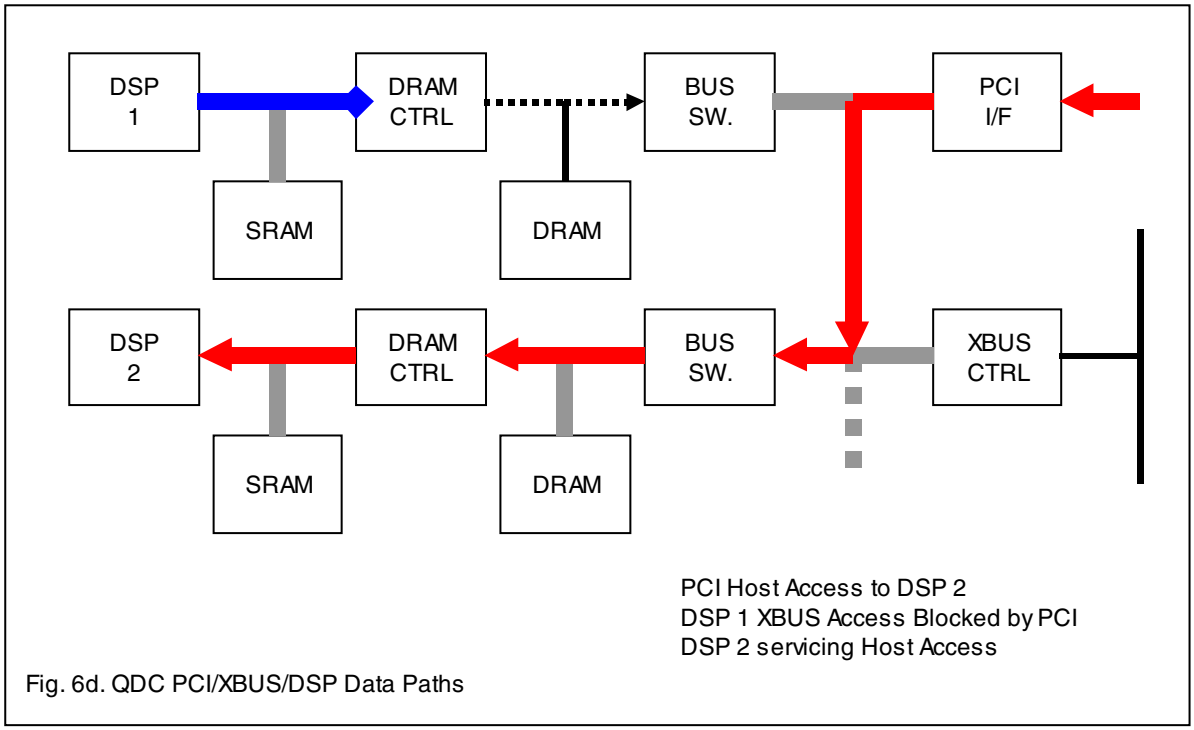


Fig. 6d. QDC PCI/XBUS/DSP Data Paths

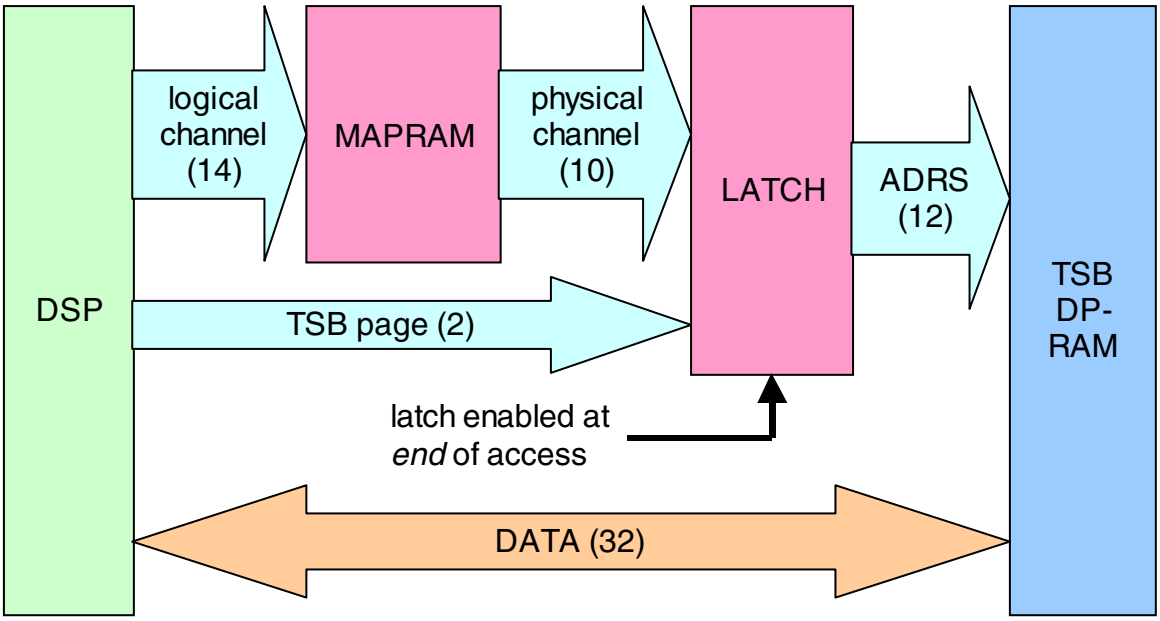
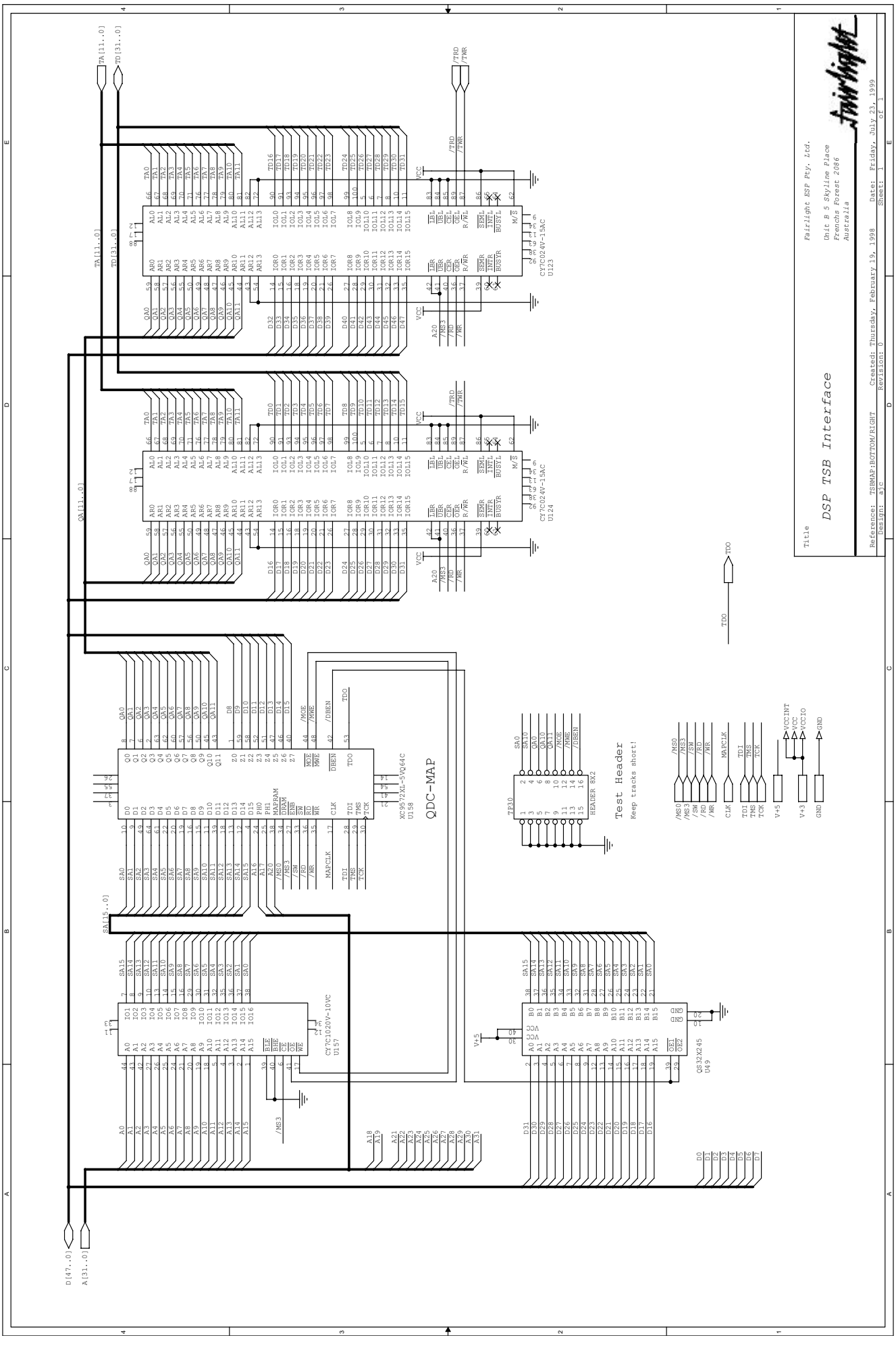
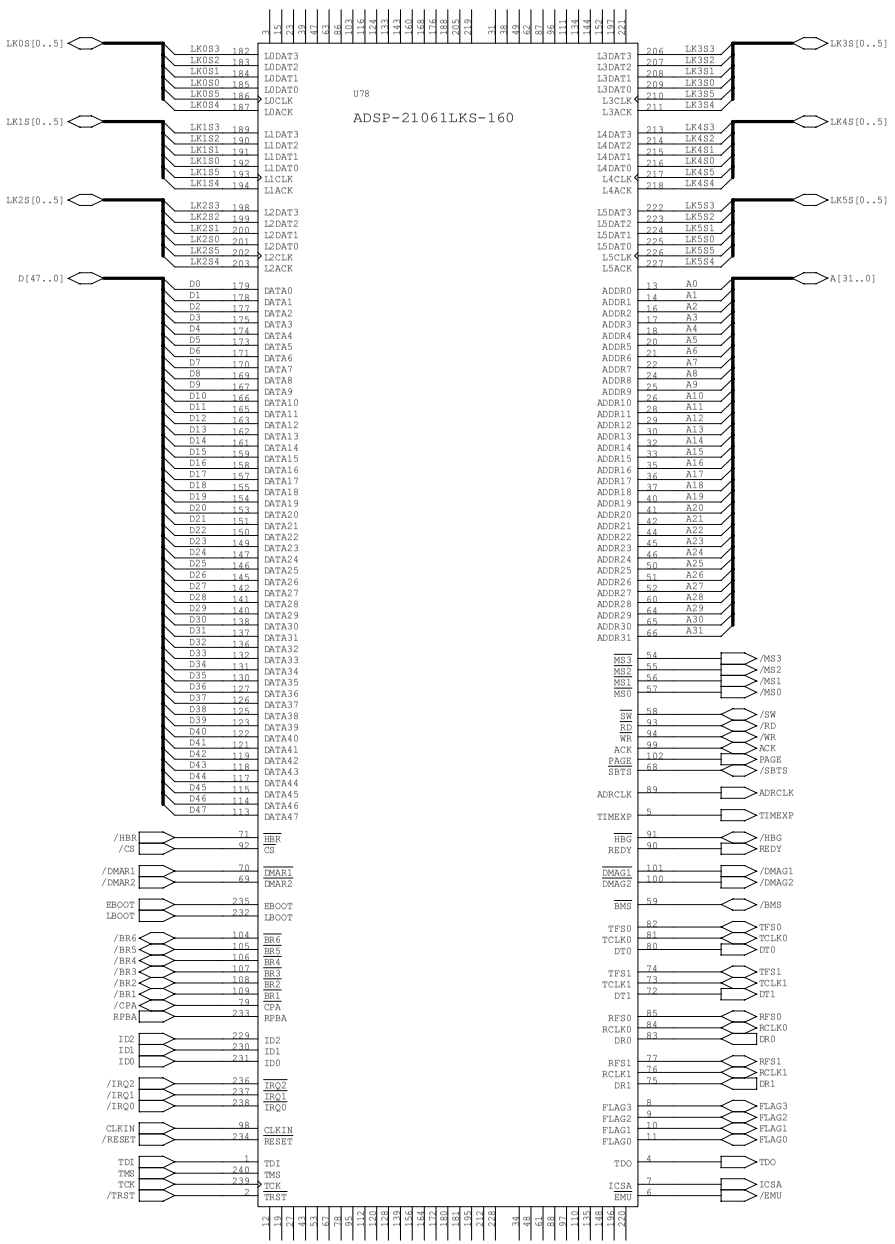
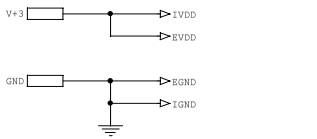


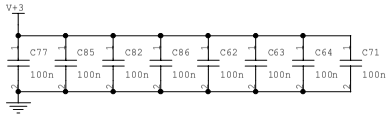
Fig. 7. QDC TSB MAPRAM & Pipeline

Corelis - JTAG Application Notes
For Reference Only


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
DSP TSB Interface
Title
Reference: TSBMAP:BOTTOM/RIGHT
Created: Thursday, February 19, 1998
Date: Friday, July 23, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1
QDC-MAP
Test Header
Keep tracks short!
CY7C1020V-10VC
U157
XC95172XL-5VQ64C
U158
QS32X245
U49
CY7C024V-15AC
U123
U124
HEADER 8X2
TP30
D[47..0]
A[31..0]
SA[15..0]
TA[11..0]
TD[31..0]
QA[11..0]
/TRD
/TWR
/MS3
/RD
/WR
/MCE
/MWE
/DBEN
TDO
TDI
TMS
TCK
MAPCLK
/MS0
/SW
CLK
V+5
V+3
VCCINT
VCC
VCCIO
GND







Title

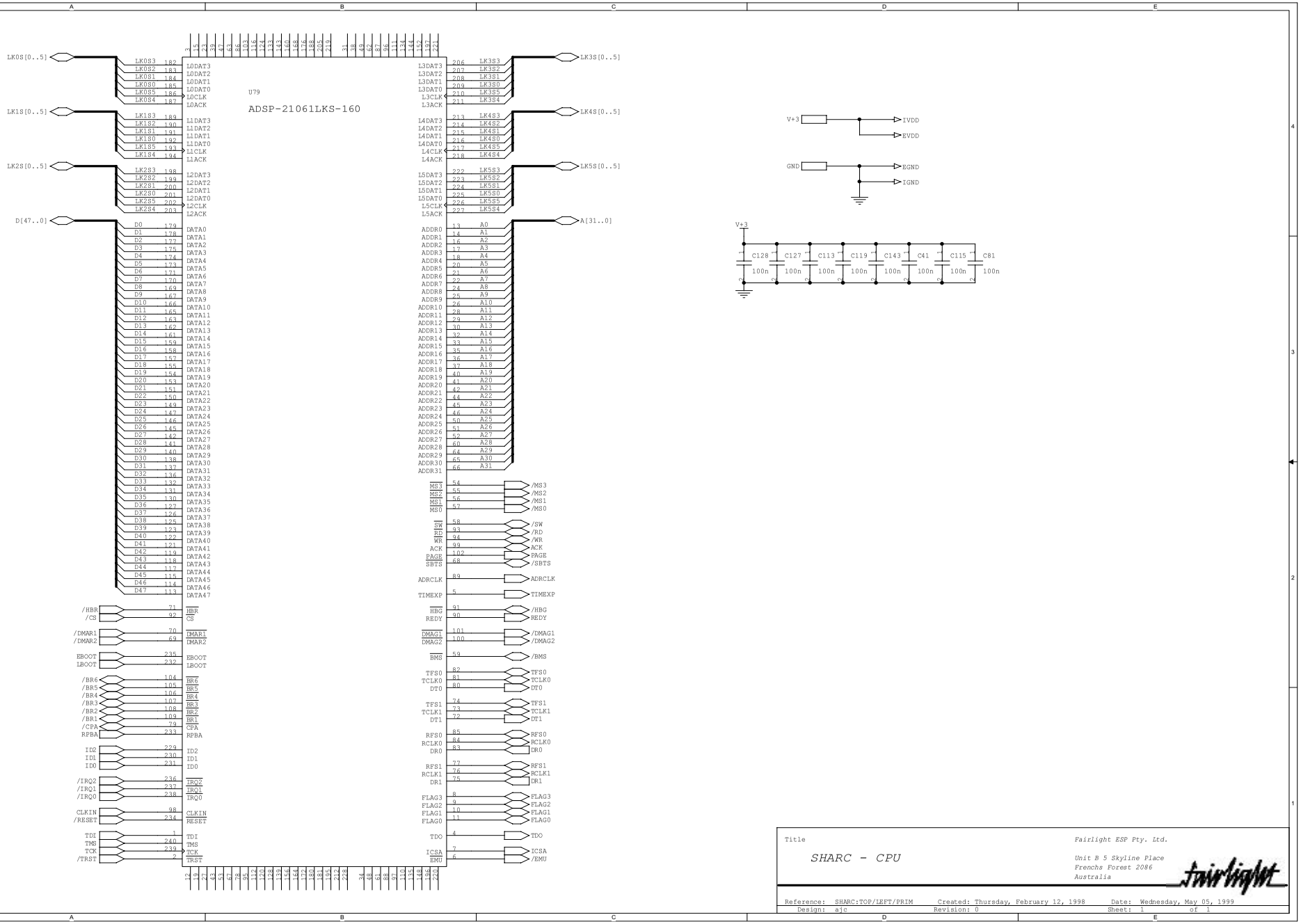
SHARC - CPU

Fairlight ESP Pty. Ltd.

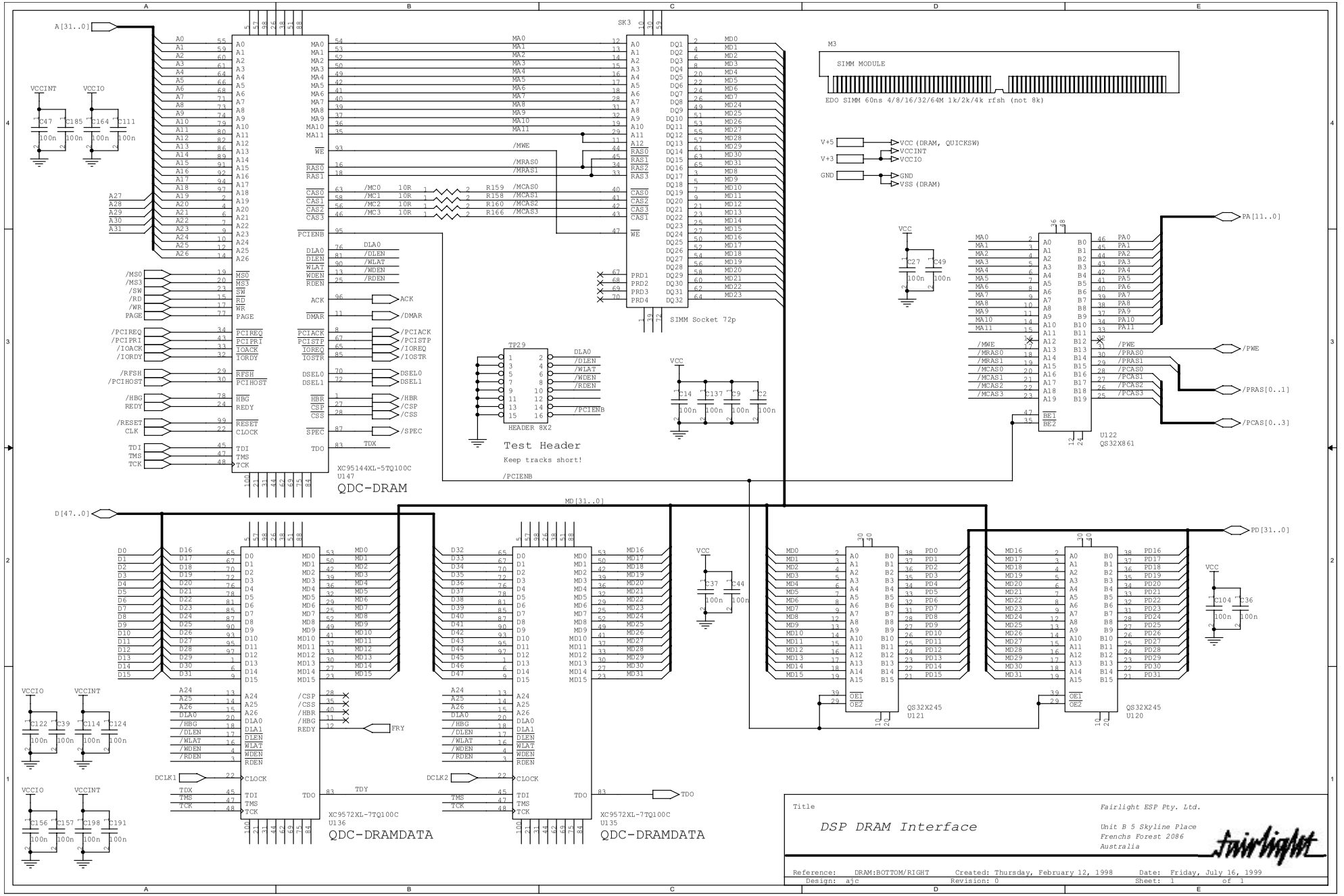
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

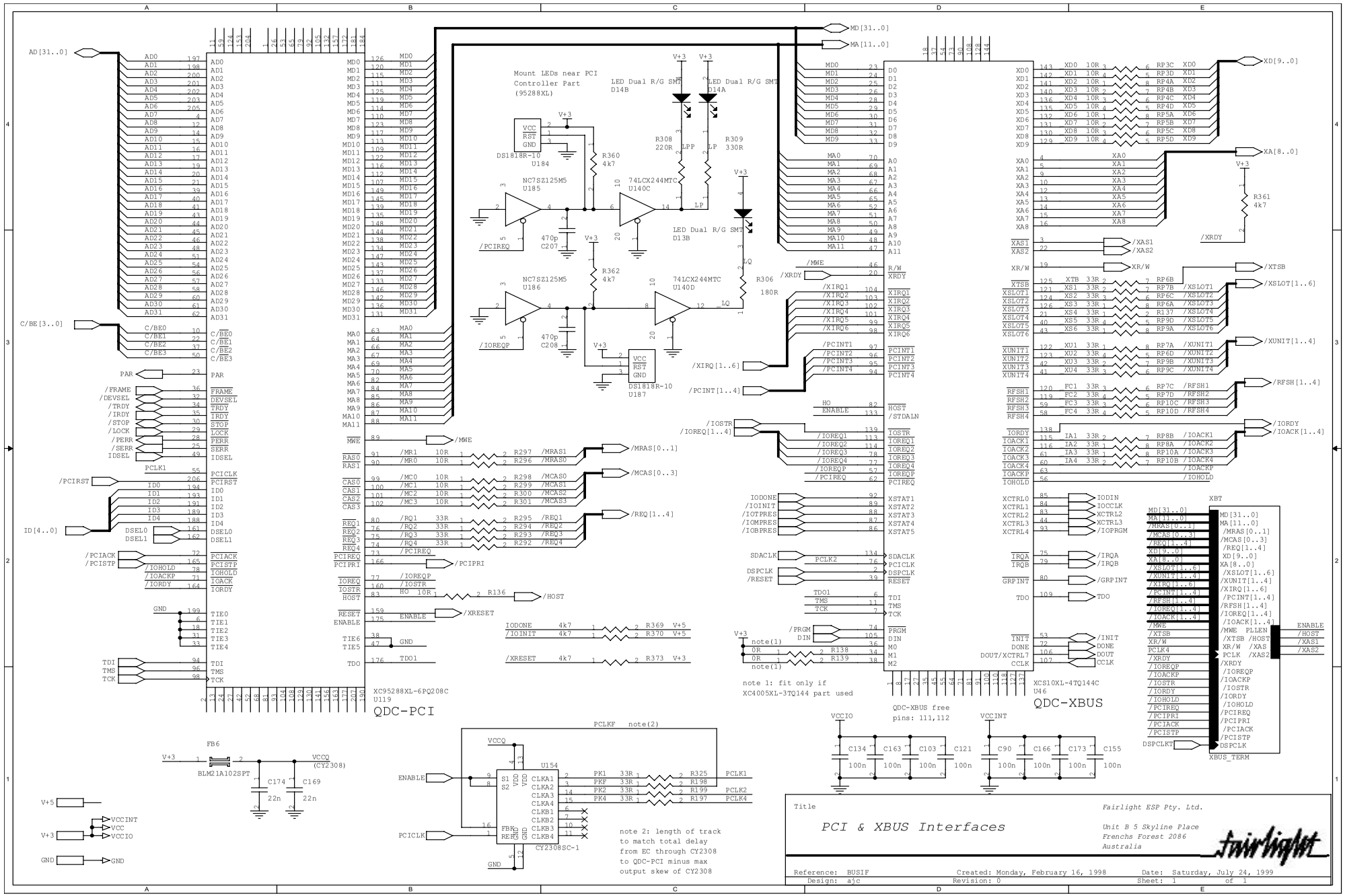
Reference: SHARC:TOP/LEFT/SEC Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999

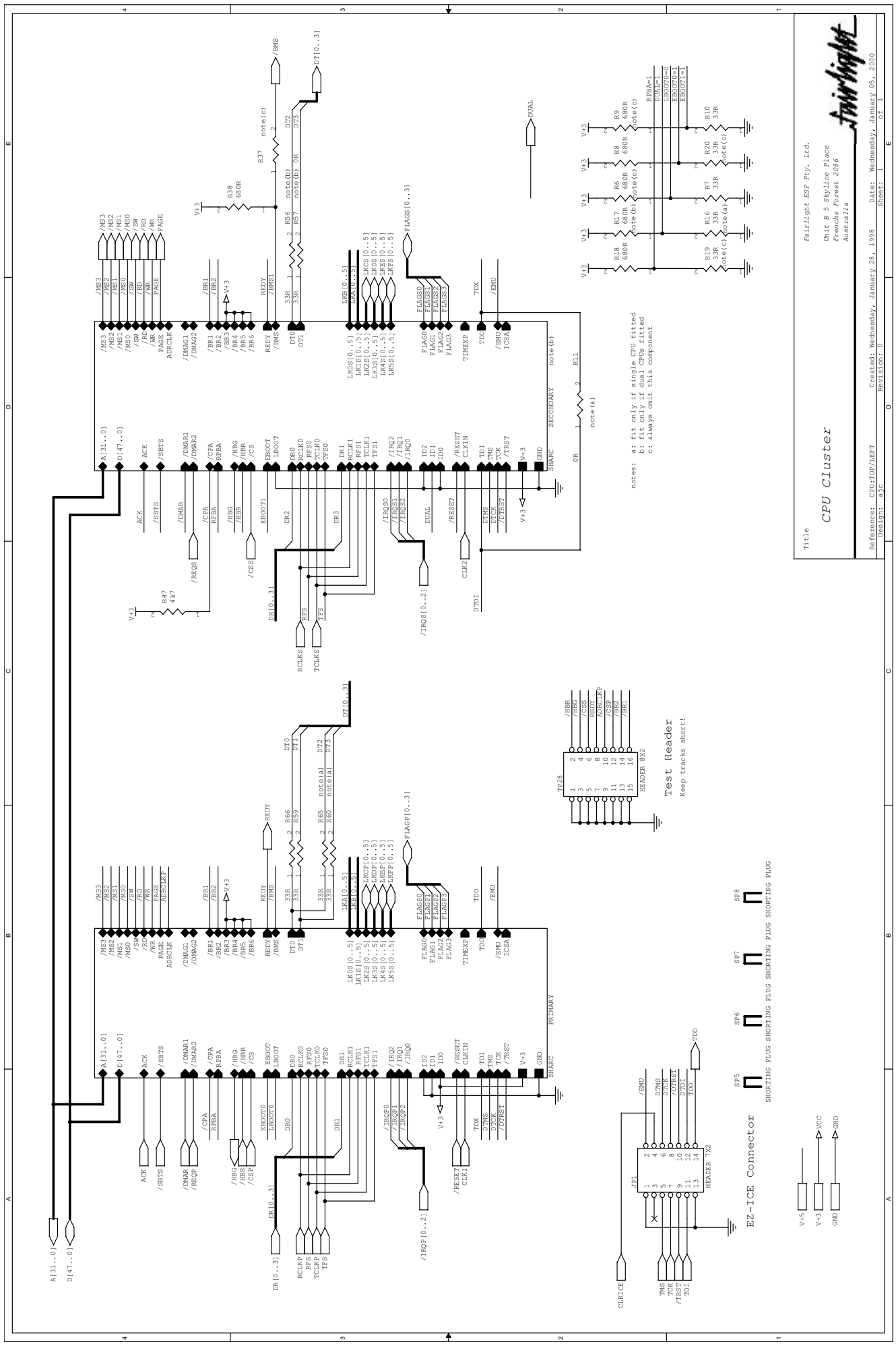
Design: ajc Revision: 0 Sheet: 1 of 1

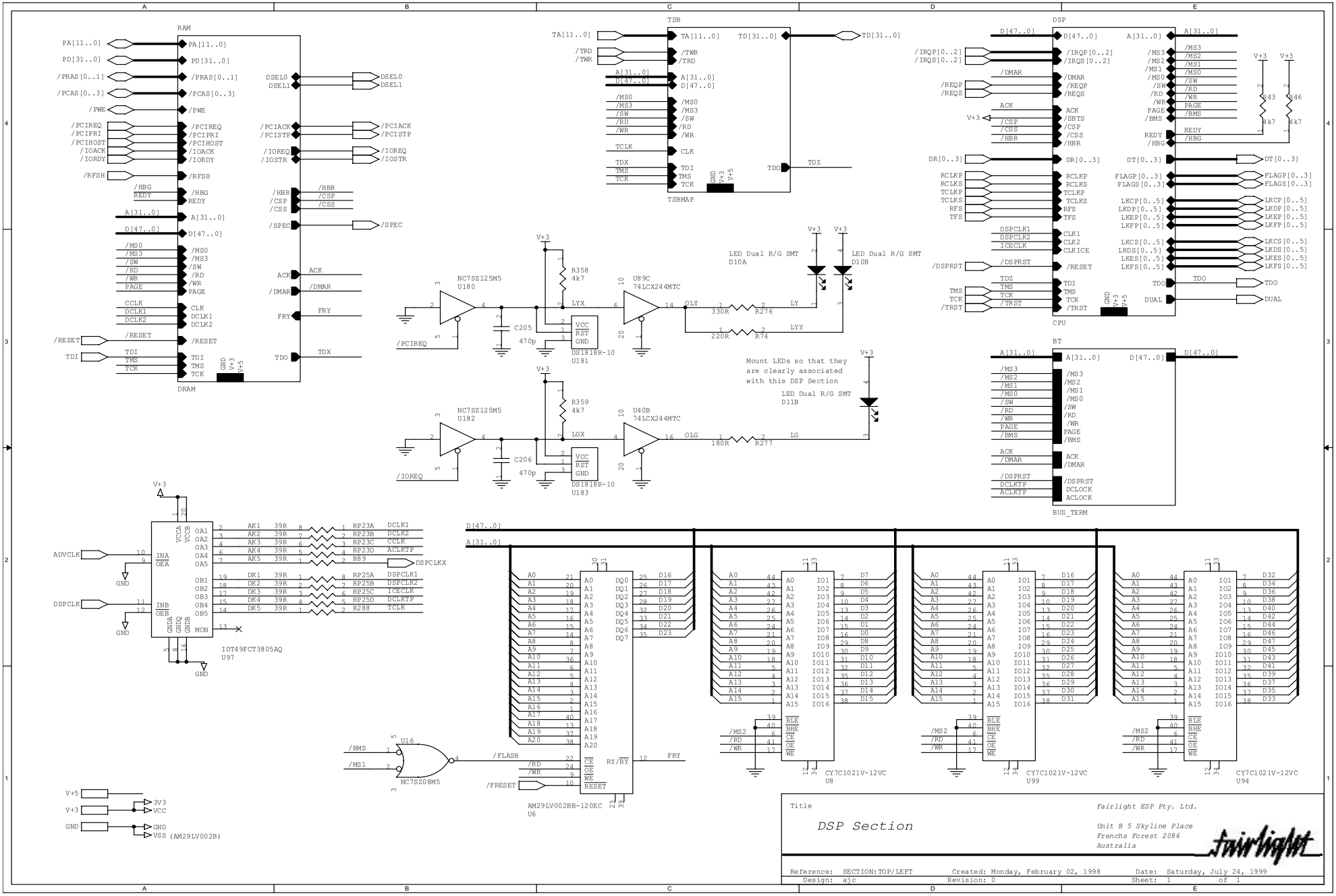


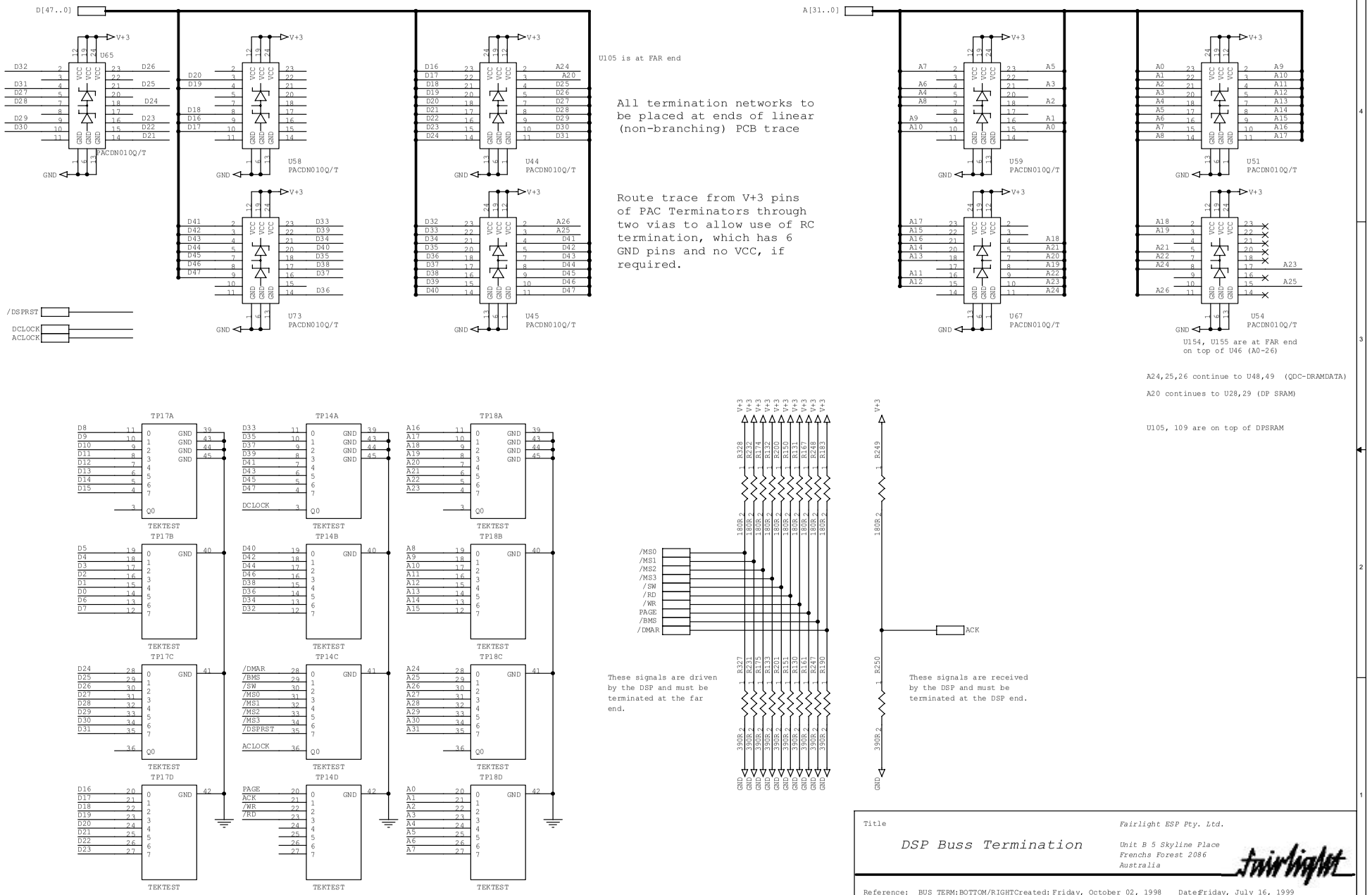
Title	*SHARC - CPU*
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	SHARC:TOP/LEFT/PRIM
Created:	Thursday, February 12, 1998
Date:	Wednesday, May 05, 1999
Design:	ajc
Revision:	0
Sheet:	1 of 1


A[31..0]
VCCINT
VCCIO
C47 100n
C185 100n
C164 100n
C111 100n
A27
A28
A29
A30
A31
/MS0
/MS3
/SW
/RD
/WR
PAGE
/PCIREQ
/PCIPRI
/IOACK
/IORDY
/RFSH
/PCIHOST
/HBG
REDY
/RESET
CLK
TDI
TMS
TCK
MA0
MA1
MA2
MA3
MA4
MA5
MA6
MA7
MA8
MA9
MA10
MA11
/MWE
/MRAS0
/MRAS1
/MCAS0
/MCAS1
/MCAS2
/MCAS3
/MC0 10R R159
/MC1 10R R158
/MC2 10R R160
/MC3 10R R166
PCIENE
DLA0
/DLEN
/WLAT
/WDEN
/RDEN
ACK
/DMAR
/PCIACK
/PCISTP
/IOREQ
/IOSTR
DSEL0
DSEL1
/HBR
/CSP
/CSS
/SPEC
TDX
XC95144XL-5TQ100C
U147
QDC-DRAM
SK3
SIMM Socket 72p
M3
SIMM MODULE
EDO SIMM 60ns 4/8/16/32/64M 1k/2k/4k rfsh (not 8k)
V+5
V+3
GND
VCC (DRAM, QUICKSW)
VCCINT
VCCIO
GND
VSS (DRAM)
TP29
HEADER 8X2
Test Header
Keep tracks short!
/PCIENB
C14 100n
C137 100n
C29 100n
C2 100n
C27 100n
C49 100n
PA[11..0]
/PWE
/PRAS[0..1]
/PCAS[0..3]
U122
QS32X861
D[47..0]
MD[31..0]
PD[31..0]
C122 100n
C39 100n
C114 100n
C124 100n
C156 100n
C157 100n
C198 100n
C191 100n
C237 100n
C44 100n
C104 100n
C36 100n
DCLK1
DCLK2
FRY
TDY
XC9572XL-7TQ100C
U136
QDC-DRAMDATA
XC9572XL-7TQ100C
U135
QDC-DRAMDATA
QS32X245
U121
QS32X245
U120
Title
DSP DRAM Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: DRAM:BOTTOM/RIGHT
Created: Thursday, February 12, 1998
Date: Friday, July 16, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1


Mount LEDs near PCI Controller Part (95288XL)
LED Dual R/G SMT D14B
LED Dual R/G SMT D14A
LED Dual R/G SMT D13B
DS1818R-10 U184
DS1818-10 U187
NC7SZ125M5 U185
NC7SZ125M5 U186
74LCX244MTC U140C
74LCX244MTC U140D
XC95288XL-6PQ208C U119
QDC-PCI
XCS10XL-4TQ144C U46
QDC-XBUS
XBUS_TERM
XBT
note 1: fit only if XC4005XL-3TQ144 part used
QDC-XBUS free pins: 111,112
note 2: length of track to match total delay from EC through CY2308 to QDC-PCI minus max output skew of CY2308
CY2308SC-1
Title
PCI & XBUS Interfaces
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: BUSIF
Created: Monday, February 16, 1998
Date: Saturday, July 24, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1


CPU Cluster
Fairlight DSP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: CPU:TOP/1EFT
Created: Wednesday, January 28, 1998
Date: Wednesday, January 05, 2000
Design: ajc
Revision: 0
Sheet: 1 of 1
notes: a: fit only if single CPU fitted
b: fit only if dual CPUs fitted
c: always omit this component
Test Header
Keep tracks short!
EZ-ICE Connector
SHORTING PLUG
SHORTING PLUG
SHORTING PLUG
SHORTING PLUG


RAM
DRAM
TSB
TSBMAP
DSP
CPU
BT
BUS_TERM
Mount LEDs so that they are clearly associated with this DSP Section
LED Dual R/G SMT D10A
LED Dual R/G SMT D10B
LED Dual R/G SMT D11B
NC7SZ125M5 U180
NC7SZ125M5 U182
DS1818R-10 U181
DS1818R-10 U183
U89C 74LCX244MTC
U40B 74LCX244MTC
IDT49FCT3805AQ U97
AM29LV002BB-120EC U6
NC7SZ08M5 U16
CY7C1021V-12VC U8
CY7C1021V-12VC U99
CY7C1021V-12VC U94
Title
DSP Section
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: SECTION:TOP/LEFT
Created: Monday, February 02, 1998
Date: Saturday, July 24, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1



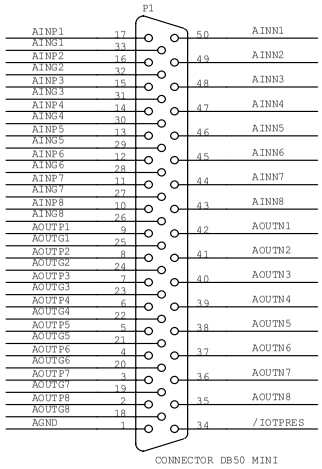
Title

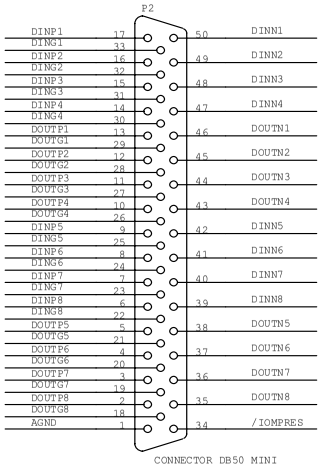
DSP Buss Termination

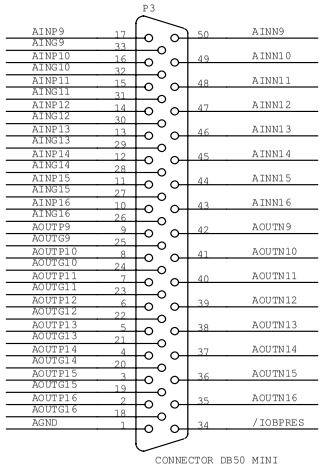
Fairlight ESP Pty. Ltd.

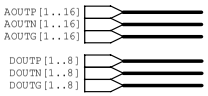
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: BUS_TERM:BOTTOM/RIGHT Created: Friday, October 02, 1998 Date: Friday, July 16, 1999
Design: Design Revision: 0 Sheet: 0 0 of





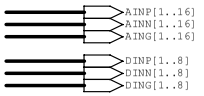


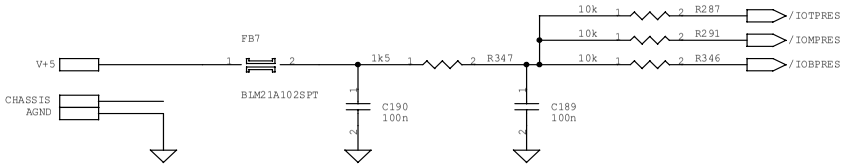


TOP CONNECTOR
(ANALOG I/O)

MIDDLE CONNECTOR
(DIGITAL I/O)

BOTTOM CONNECTOR
(ANALOG I/O)

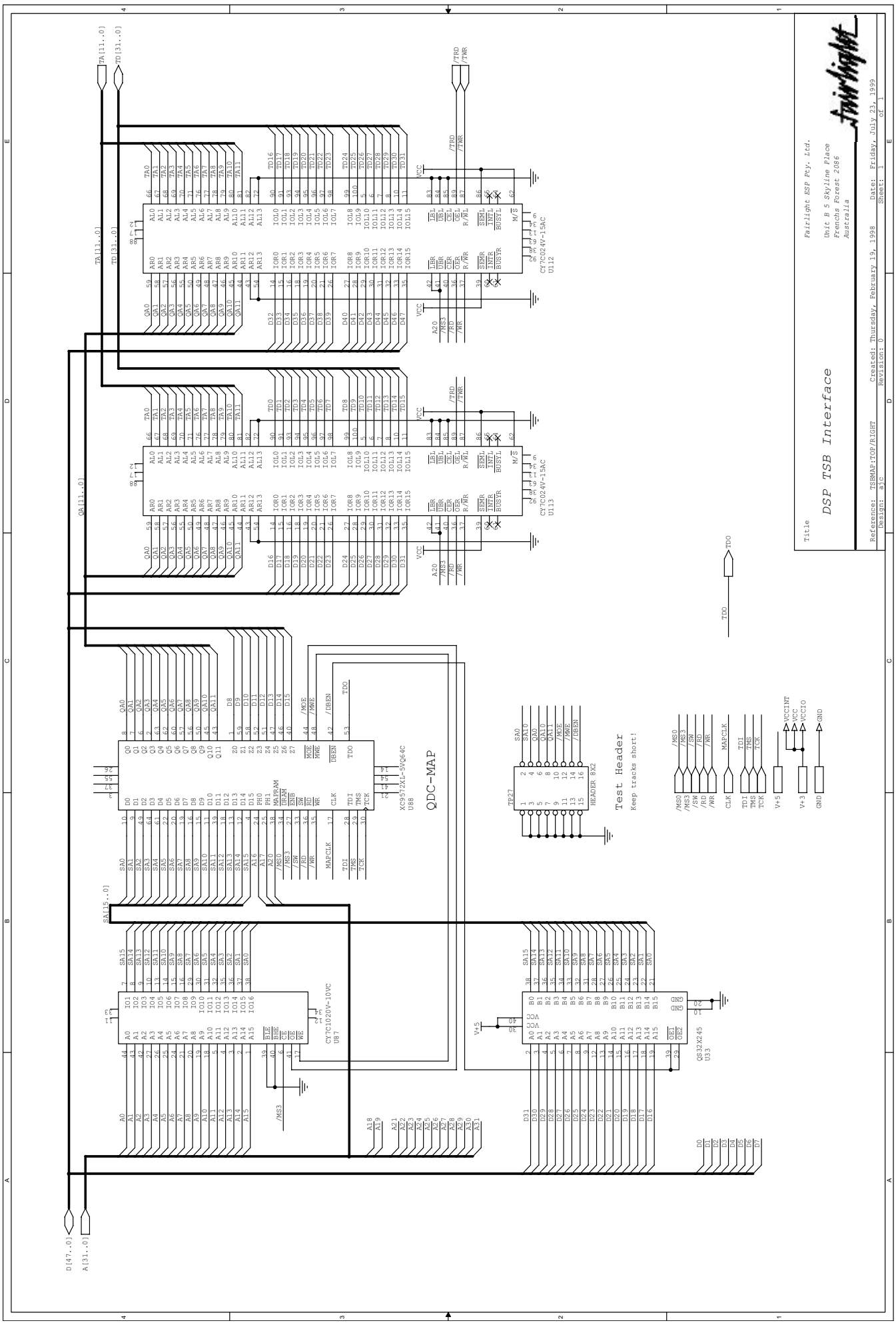


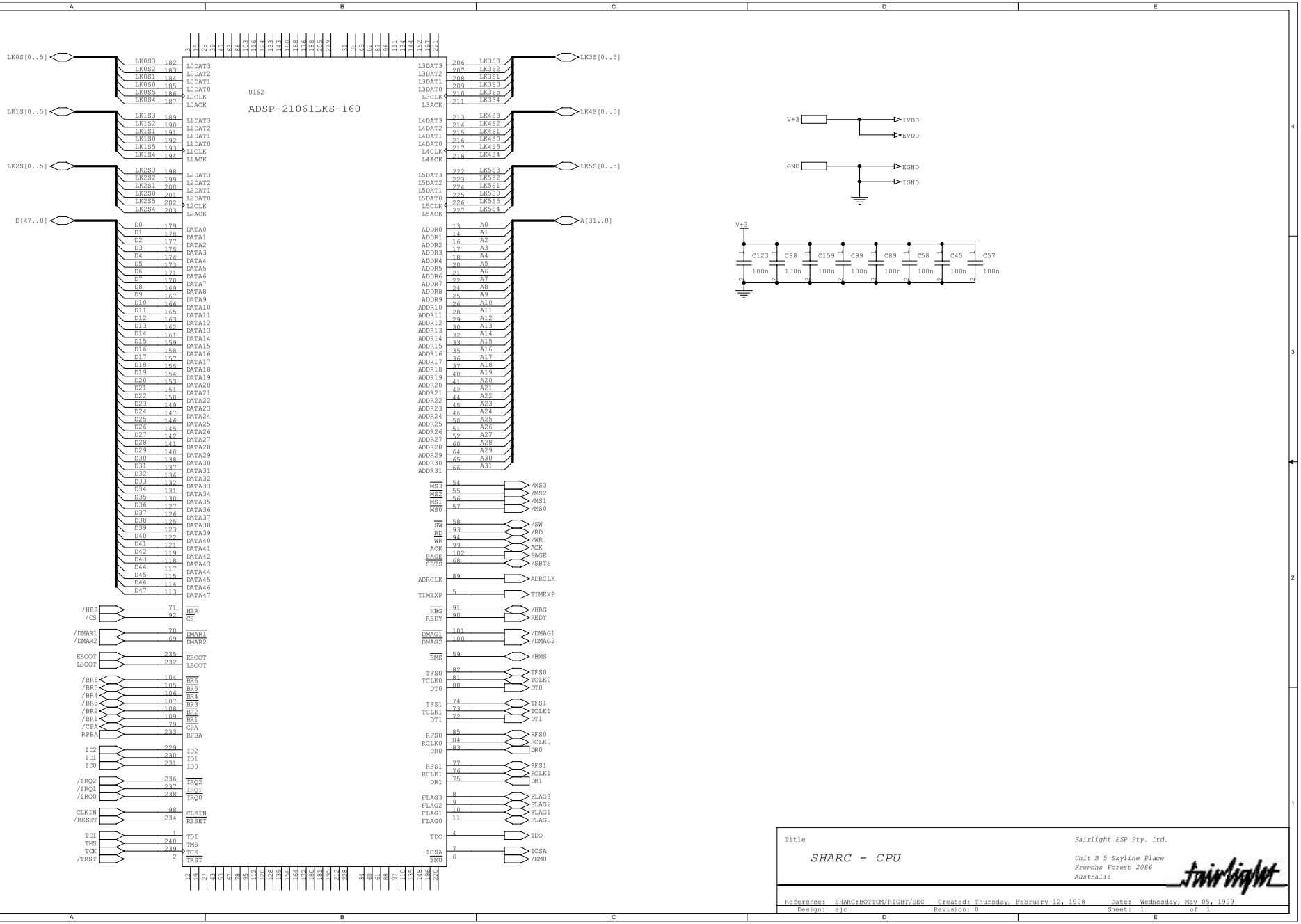


AMP Right Angle Receptacle

745116-2,-1	Standard Mounting Screw
747193-1,-2	Female Screwlocks

Title	ESP-DCC I/O Connectors	Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place, Frenchs Forest 2086, Australia
Reference: IOCONN	Created: Thursday, May 14, 1998	Date: Friday, July 16, 1999	
Design: ajc	Revision: 0	Sheet: 0 of 0	


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
DSP TSB Interface
Reference: TSBMAP7OP/RIGHT
Created: Thursday, February 19, 1998
Date: Friday, July 23, 1999
Revision: 0
Sheet: 1 of 1
Design: gdc
QDC-MAP
Test Header
Keep tracks short!
CY7C1020V-10VC
U87
CY7C024V-15AC
U112
CY7C024V-15AC
U113
XC9572XL-5VQ64C
U88
QS32X245
U33
TP27
HEADER 8X2
V+5
V+3
GND
VCCINT
VCC
VCCIO
TDO
TDI
TMS
TCK
/MS0
/MS3
/SW
/RD
/WR
MAPCLK
CLK
/TRD
/TWR
TA[11..0]
TD[31..0]
QA[11..0]
SA[15..0]
D[47..0]
A[31..0]



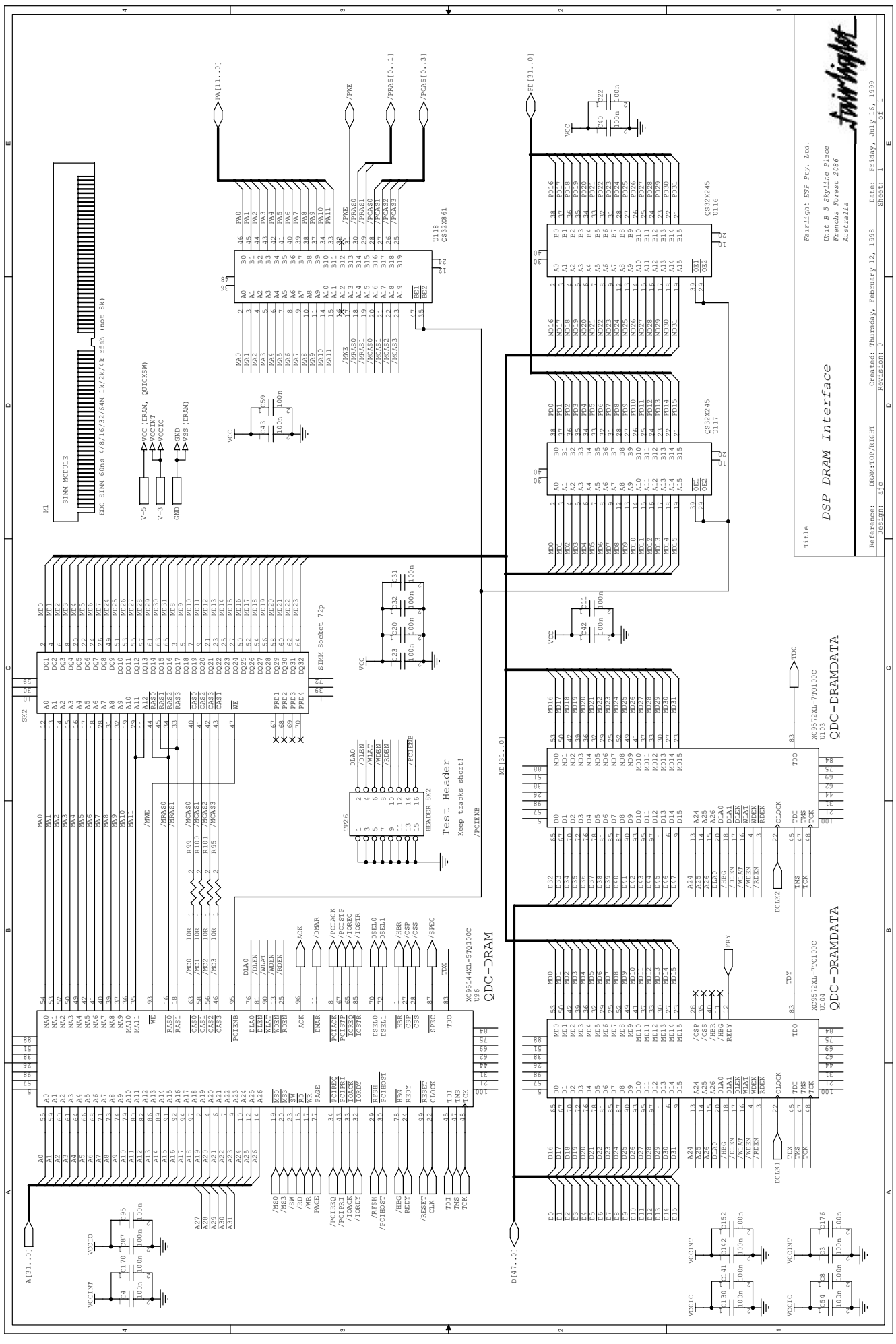
Title

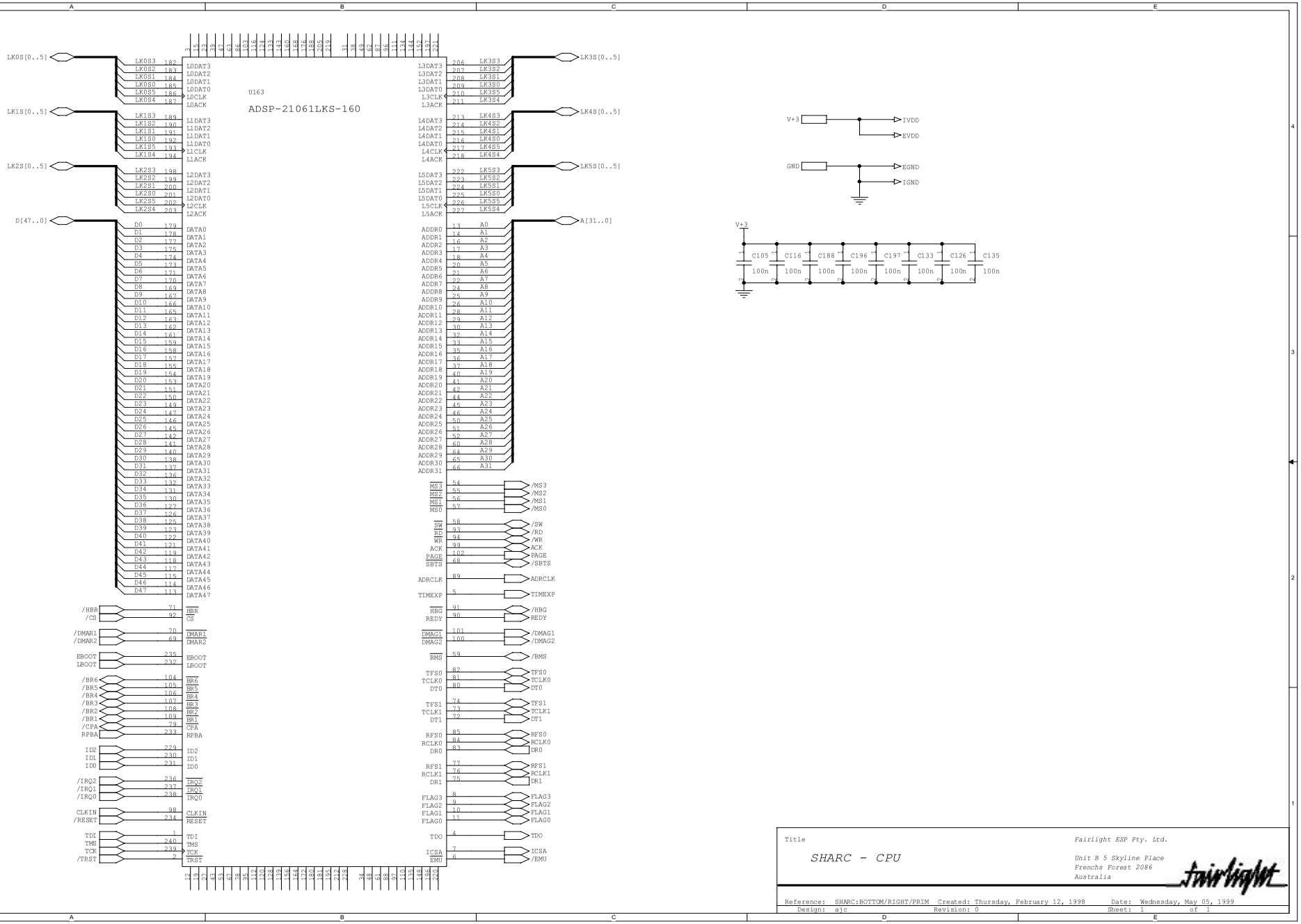
SHARC - CPU

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: SHARC:BOTTOM/RIGHT/SEC Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999
Design: ajc Revision: 0 Sheet: 1 of 1


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
DSP DRAM Interface
References:
Design: ajc
DRAM:TOP/RIGHT
Revision: 0
Created: Thursday, February 12, 1998
Date: Friday, July 16, 1999
Sheet: 1 of 1
SIMM MODULE
EDO SIMM 60ns 4/8/16/32/64M 1k/2k/4k rfsh (not 8k)
Test Header
Keep tracks short!
QDC-DRAM
QDC-DRAMDATA
QDC-DRAMDATA
S3M Socket 72p
HEADER 8X2
QS32X245
QS32X861
XC95144XL-5TQ100C
XC95172XL-7TQ100C
XC95172XL-7TQ100C



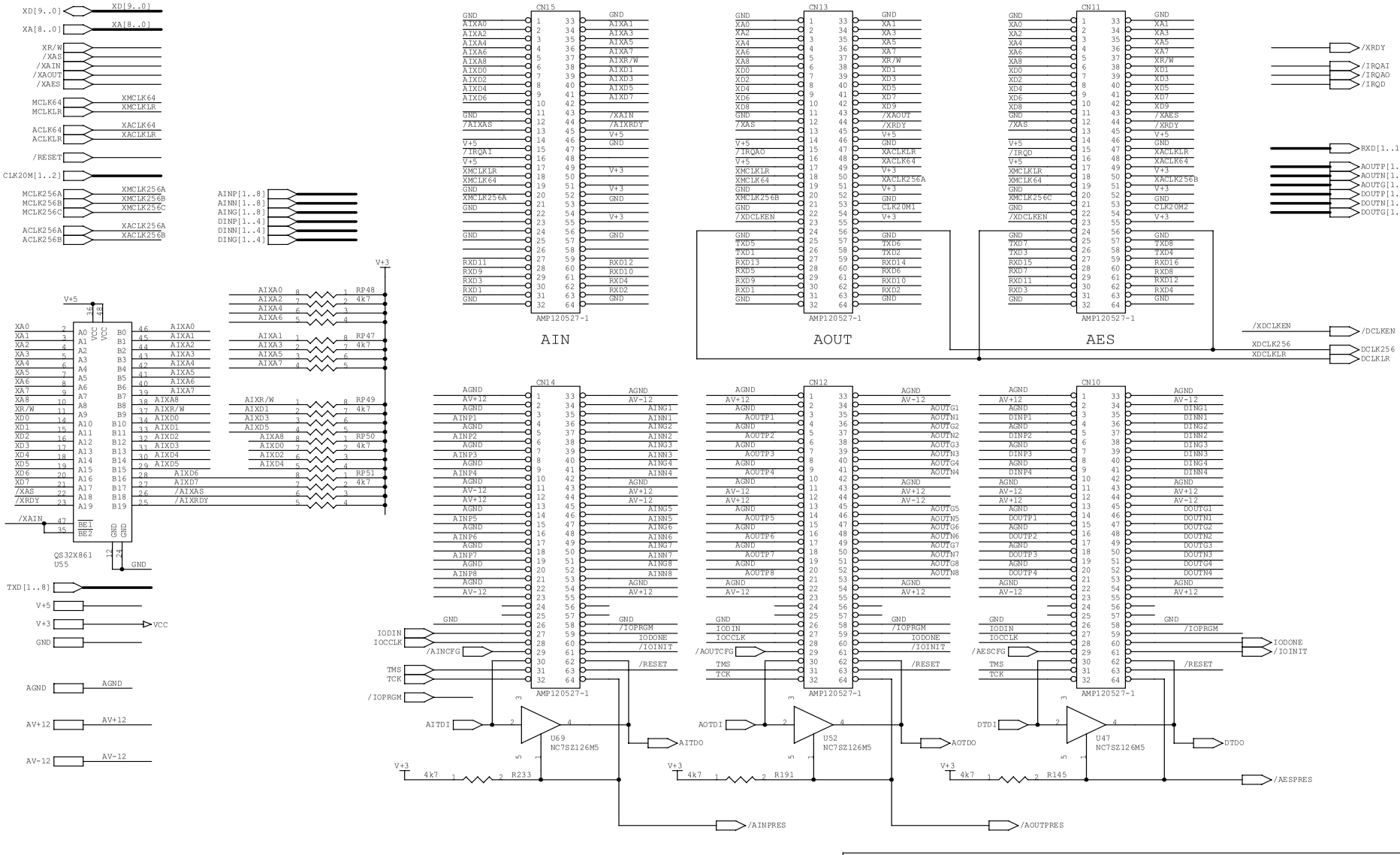
Title

SHARC - CPU

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: SHARC:BOTTOM/RIGHT/PRIM Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999
Design: ajc Revision: 0 Sheet: 1 of 1



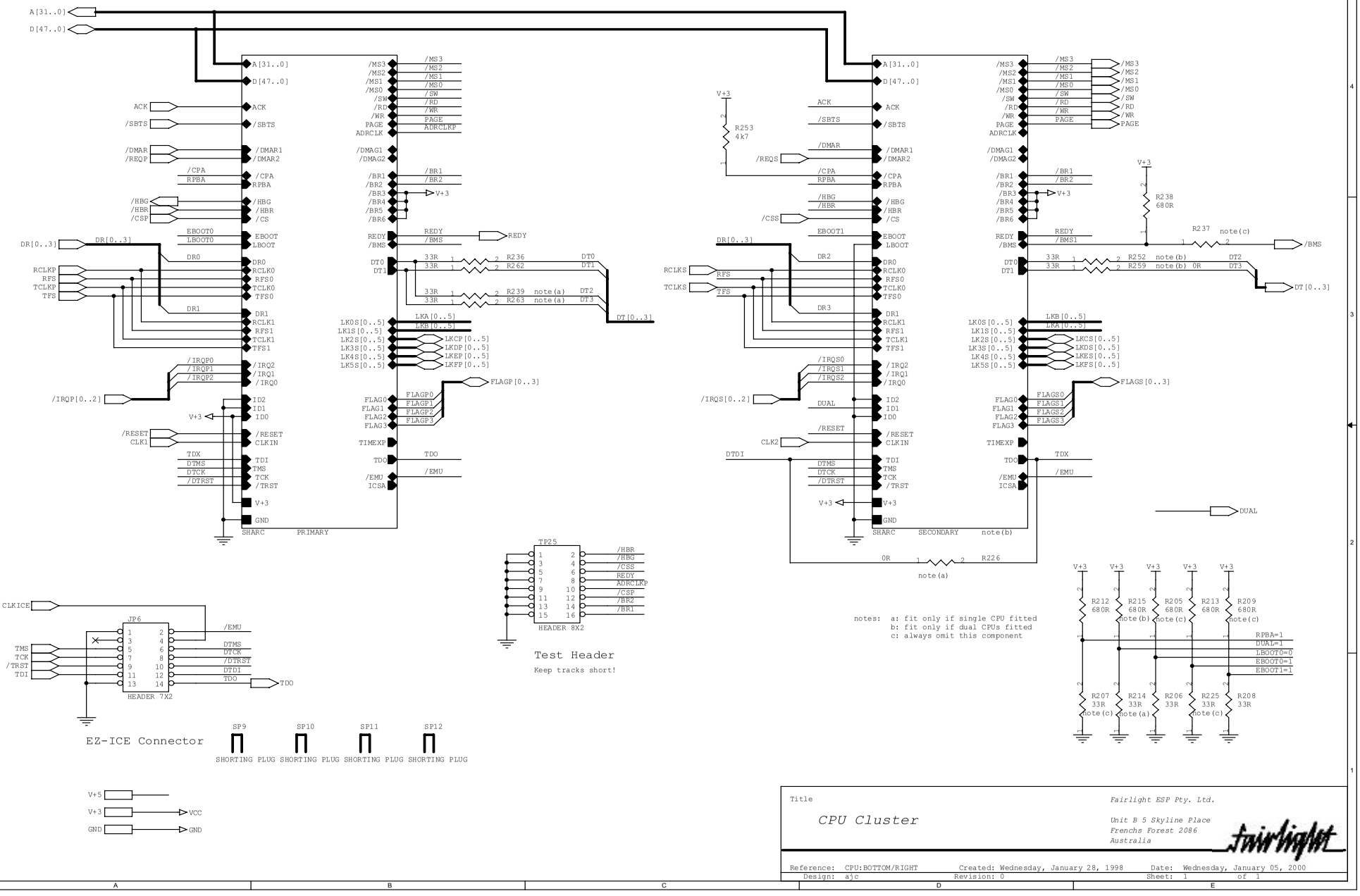
Title

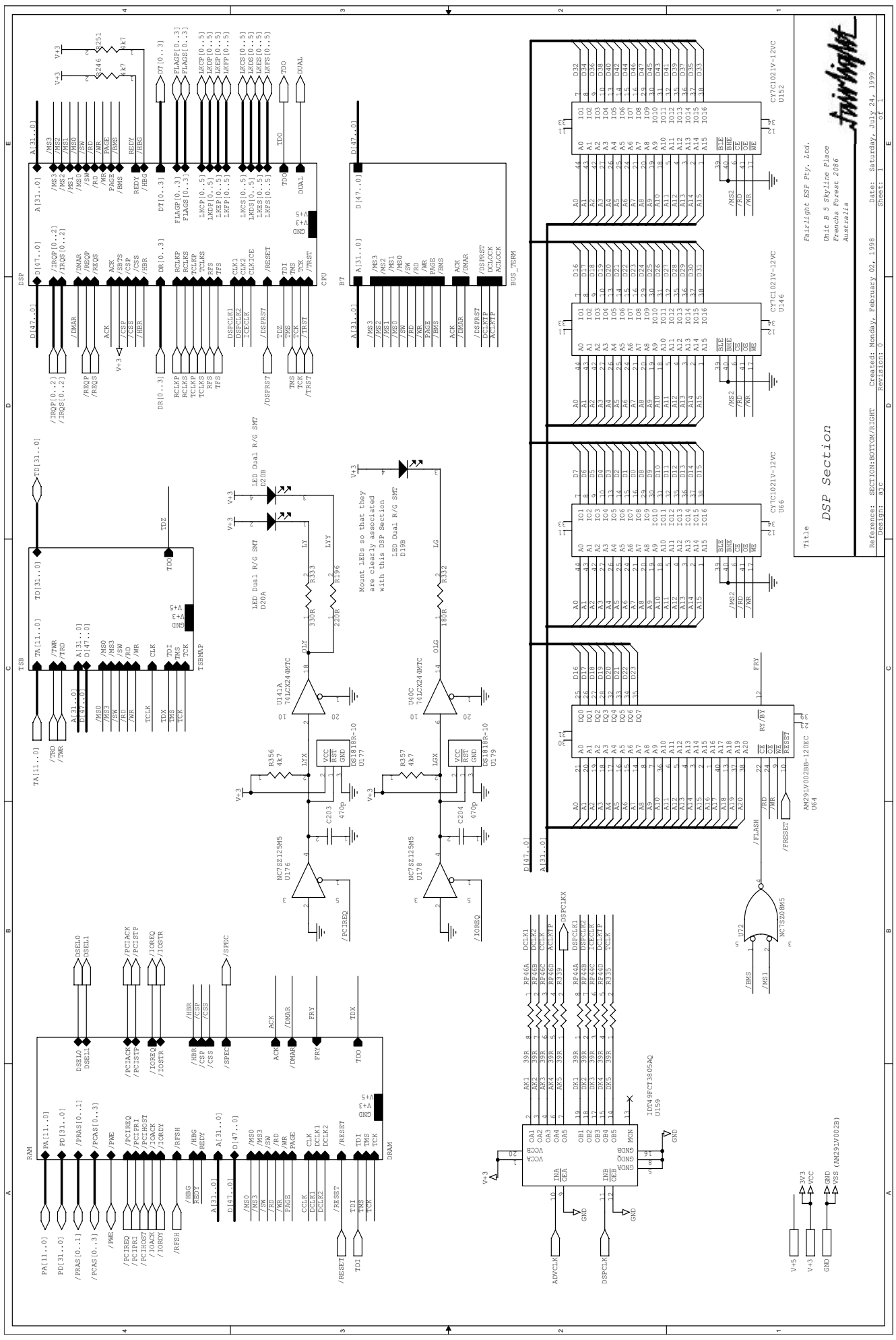
Audio I/O Module Connectors

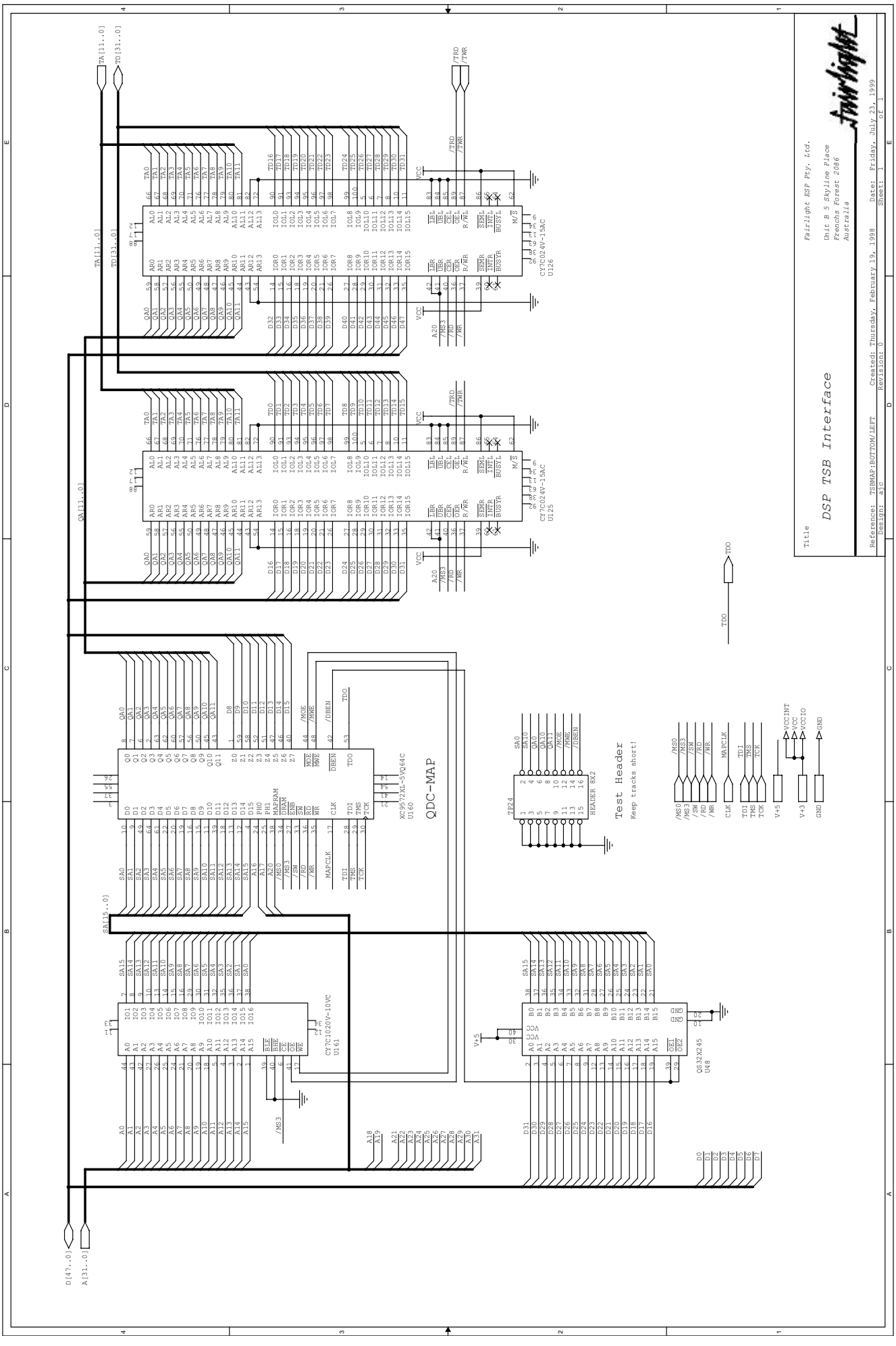
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

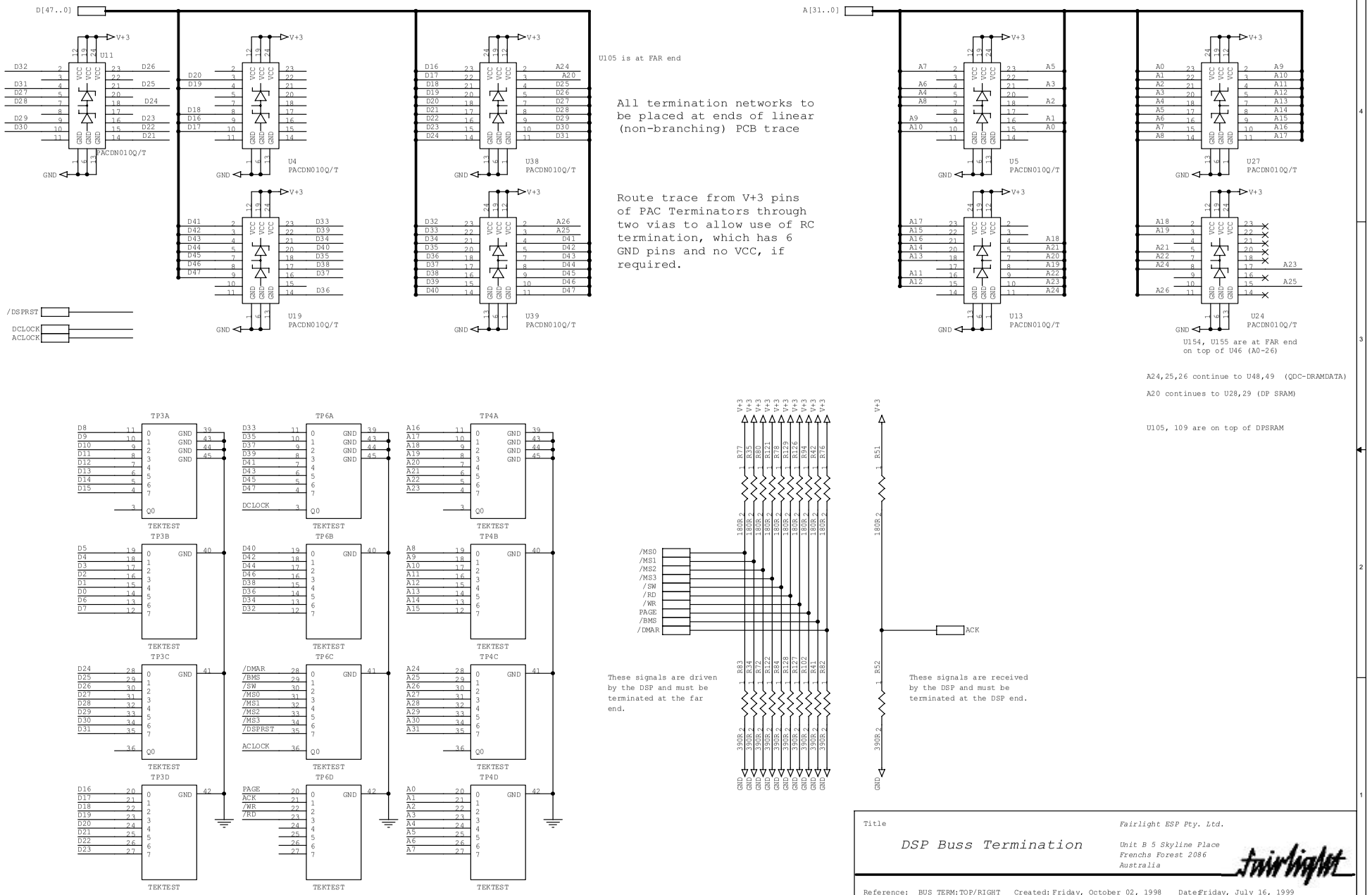
Reference: AUDIO:BOTTOM Created: Wednesday, February 18, 1998 Date: Monday, July 26, 1999

Design: ajc Revision: 0 Sheet: 1 of 1


A[31..0]
D[47..0]
SHARC PRIMARY
SHARC SECONDARY note(b)
R253 4k7
R236 33R
R262 33R
R239 note(a) 33R
R263 note(a) 33R
R238 680R
R237 note(c)
R252 note(b) 33R
R259 note(b) 0R
R226 0R
note(a)
JP6
HEADER 7X2
EZ-ICE Connector
TP25
HEADER 8X2
Test Header
Keep tracks short!
SP9 SP10 SP11 SP12
SHORTING PLUG SHORTING PLUG SHORTING PLUG SHORTING PLUG
R212 680R
R215 680R note(b)
R205 680R note(c)
R213 680R
R209 680R note(c)
R207 33R note(c)
R214 33R note(a)
R206 33R
R225 33R note(c)
R208 33R
RPBA=1
DUAL=1
LBOOT0=0
EBOOT0=1
EBOOT1=1
notes: a: fit only if single CPU fitted
b: fit only if dual CPUs fitted
c: always omit this component
Title
CPU Cluster
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: CPU:BOTTOM/RIGHT
Created: Wednesday, January 28, 1998
Date: Wednesday, January 05, 2000
Design: ajc
Revision: 0
Sheet: 1 of 1


DSP Section
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
References: SECTION:BOTTOM/RIGHT
Created: Monday, February 02, 1998
Date: Saturday, July 24, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1
DSP
BT
CPU
BUS_TERM
TSB
TSBMAP
RAM
DRAM
FLASH
U141A 74LCX244MTC
U40C 74LCX244MTC
LED Dual R/G SMT D20A
LED Dual R/G SMT D20B
LED Dual R/G SMT D19B
Mount LEDs so that they are clearly associated with this DSP Section
CY7C1021V-12VC U66
CY7C1021V-12VC U146
CY7C1021V-12VC U152
AM29LV002BB-120EC U64
IDT49FCT3805AQ U159
NC7SZ125M5 U176
NC7SZ125M5 U178
NC7SZ08M5 U72
DS1818R-10 U177
DS1818R-10 U179


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Title
DSP TSB Interface
Reference: TSBMAP:BOTTOM/LEFT
Created: Thursday, February 19, 1998
Date: Friday, July 23, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1
QDC-MAP
XC95172XL-5VQ64C
U160
CY7C1020V-10VC
U161
QS32X245
U48
CY7C024V-15AC
U125
CY7C024V-15AC
U126
Test Header
Keep tracks short!
HEADER 8X2
TP24
TA[11..0]
TD[31..0]
QA[11..0]
SA[15..0]
D[47..0]
A[31..0]
/TRD
/TWR
/MS3
/RD
/WR
/MCE
/MWE
/DBEN
MAPCLK
TDO
TDI
TMS
TCK
V+5
V+3
VCCINT
VCC
VCCIO
GND



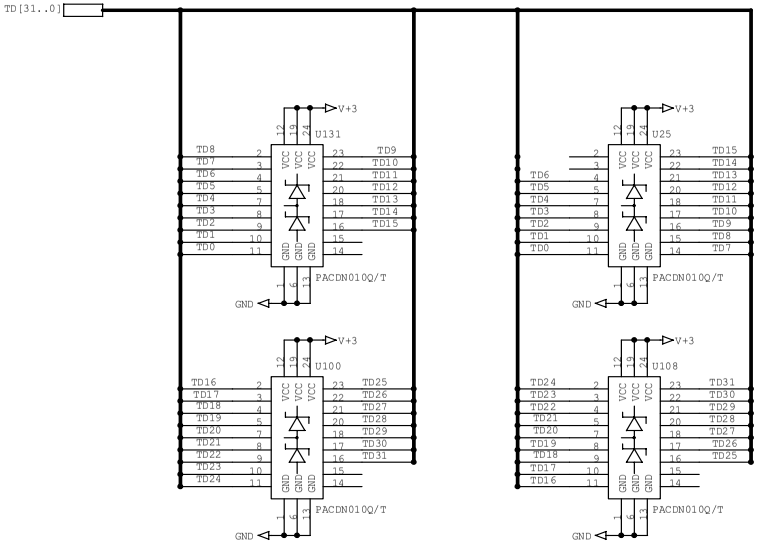
Title

DSP Buss Termination

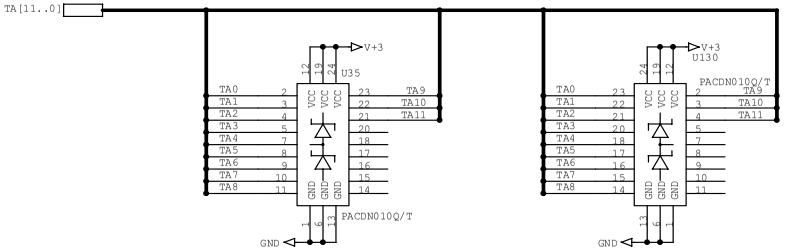
Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: BUS_TERM:TOP/RIGHT Created: Friday, October 02, 1998 Date: Friday, July 16, 1999
Design: Design Revision: 0 Sheet: 0 0 of



U147,149: FAR END



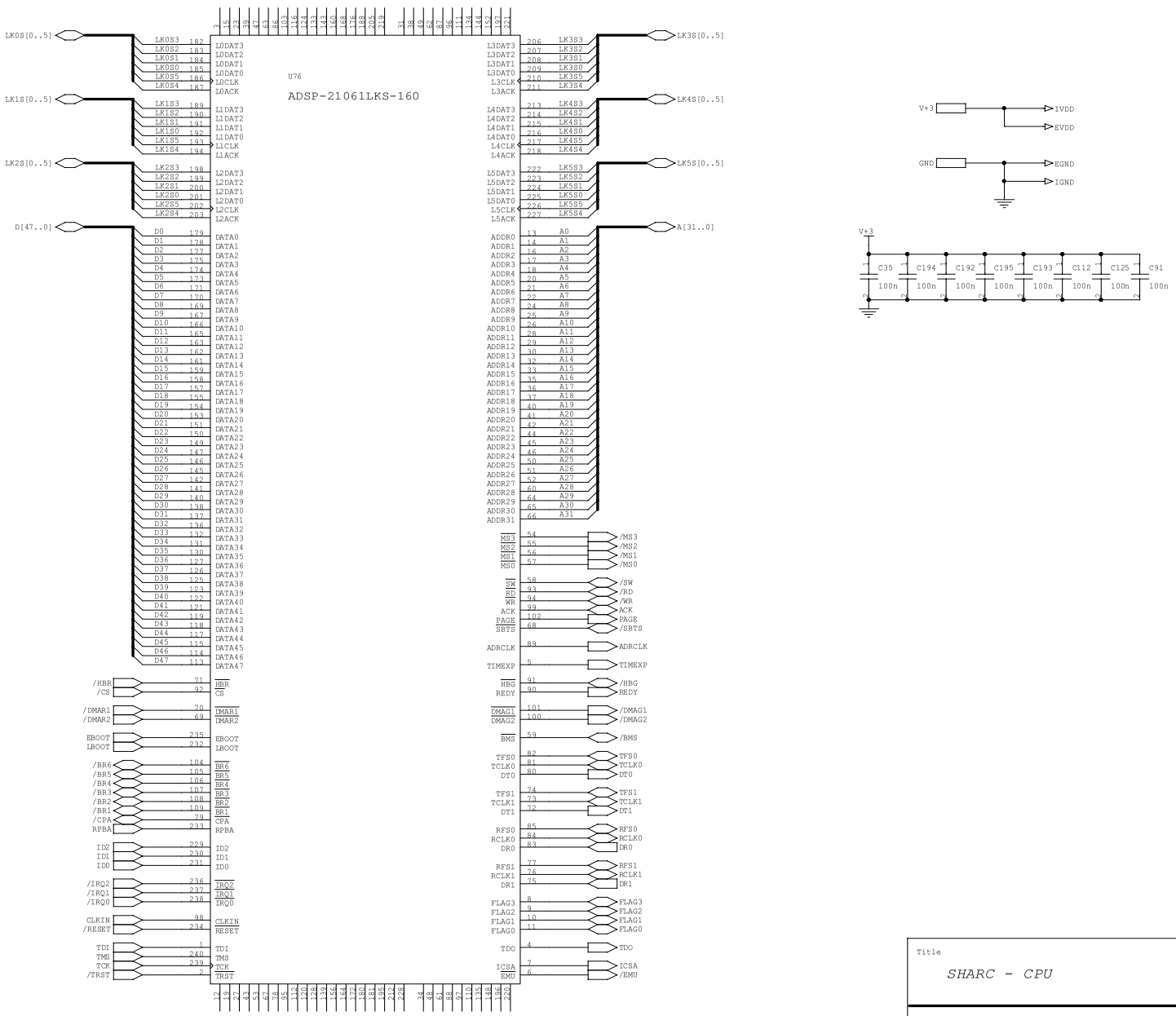
U145: NEAR END

U145: FAR END

All termination networks to be placed at ends of linear (non-branching) PCB trace

Route trace from V+3 pins of PAC Terminators through two vias to allow use of RC termination, which has 6 GND pins and no VCC, if required.

Title		Fairlight ESP Pty. Ltd.
TSB Buss Termination		Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference: TSB_TERM	Created: Tuesday, October 20, 1998	Date: Wednesday, May 05, 1999
Design: ajc	Revision: 0	Sheet: 0 0 of



Title

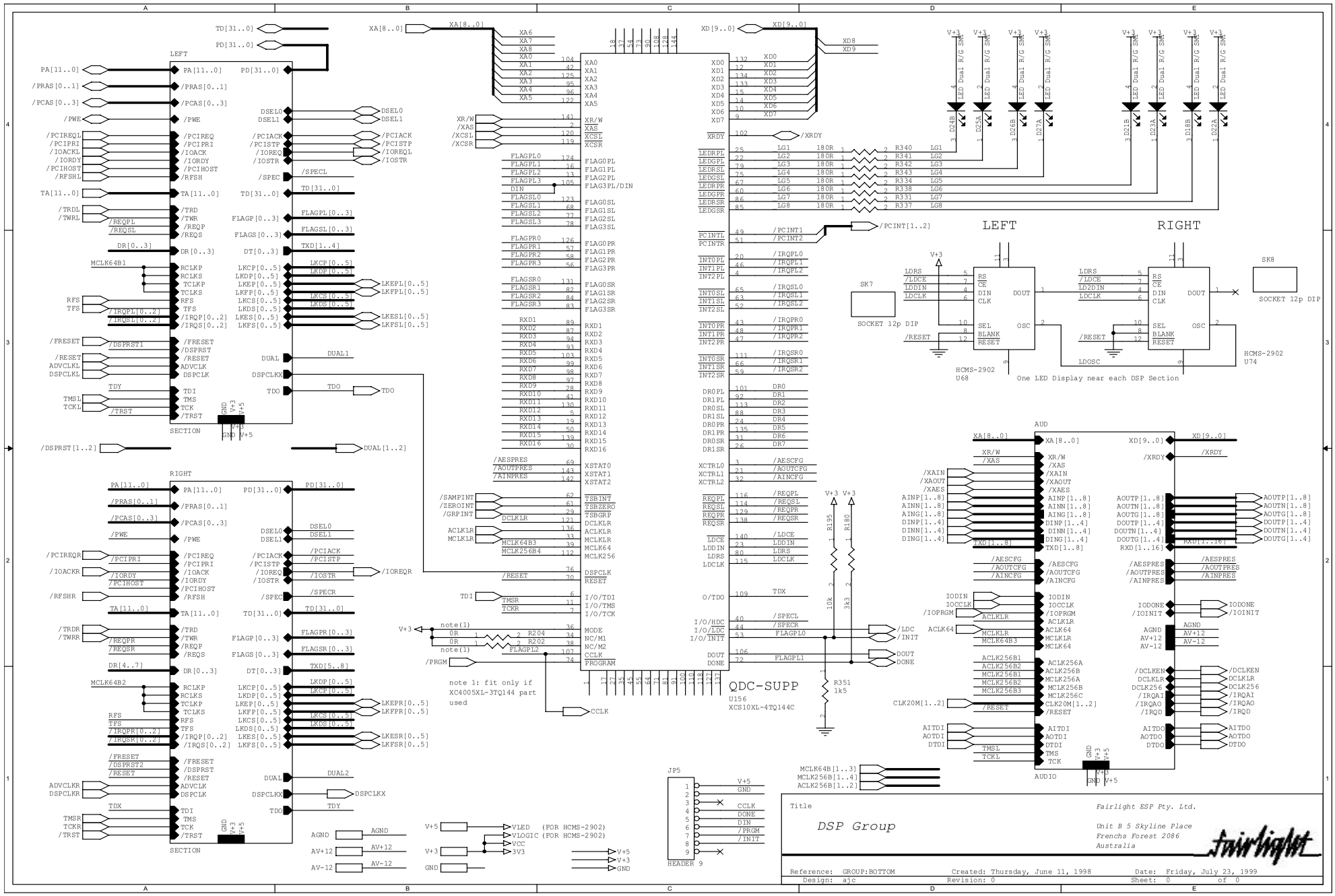
SHARC - CPU

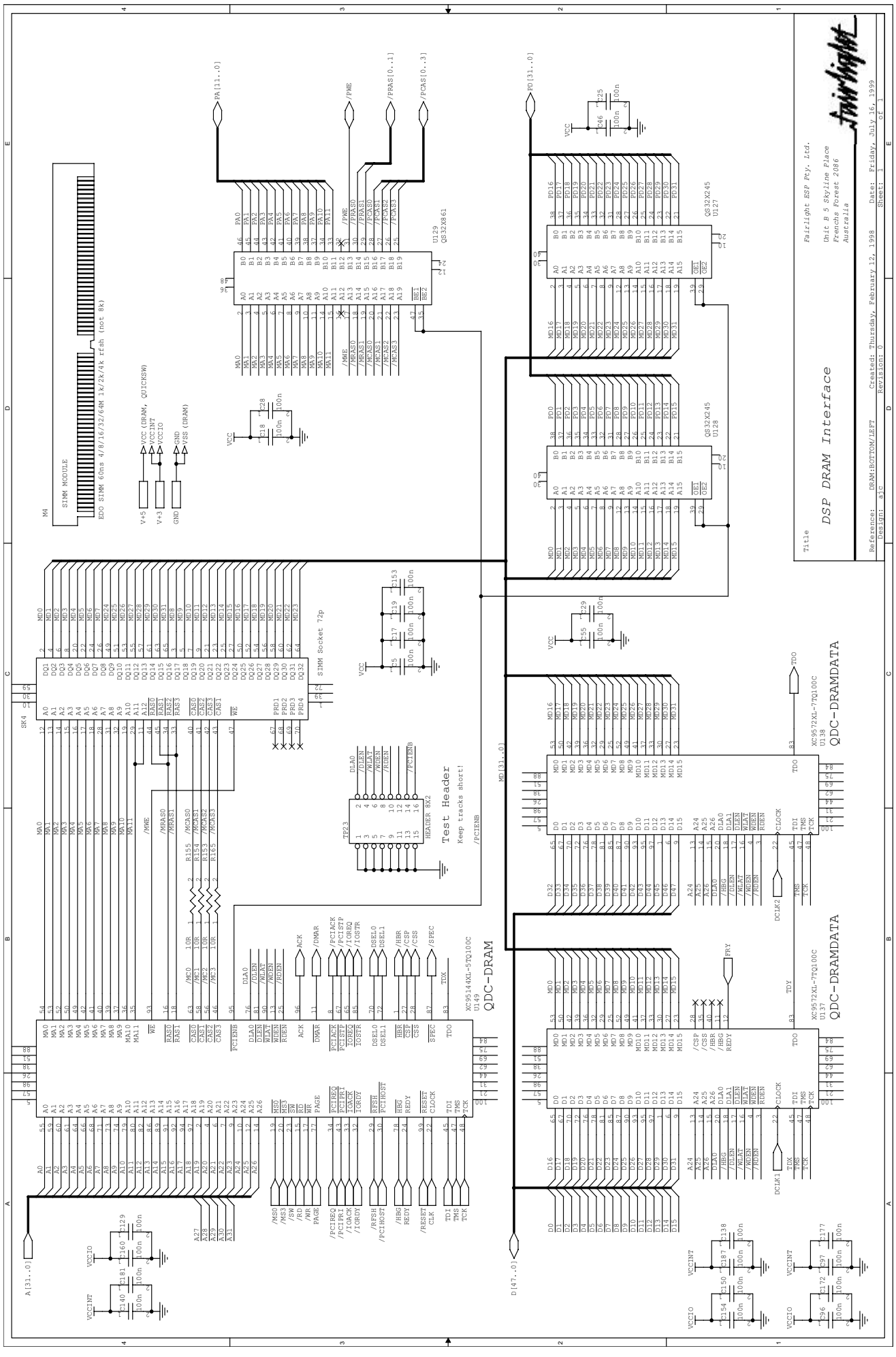
Fairlight ESP Pty. Ltd.

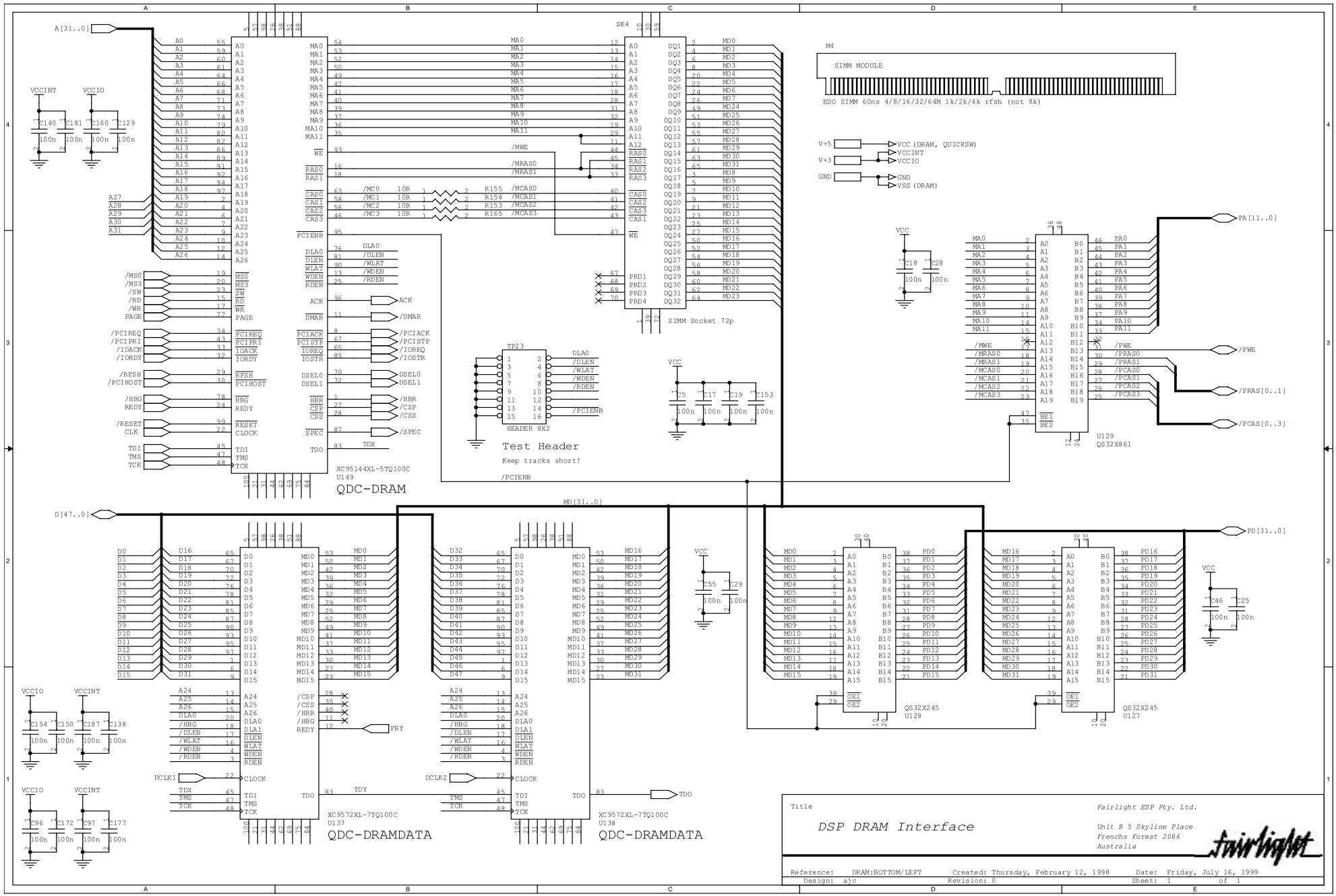
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

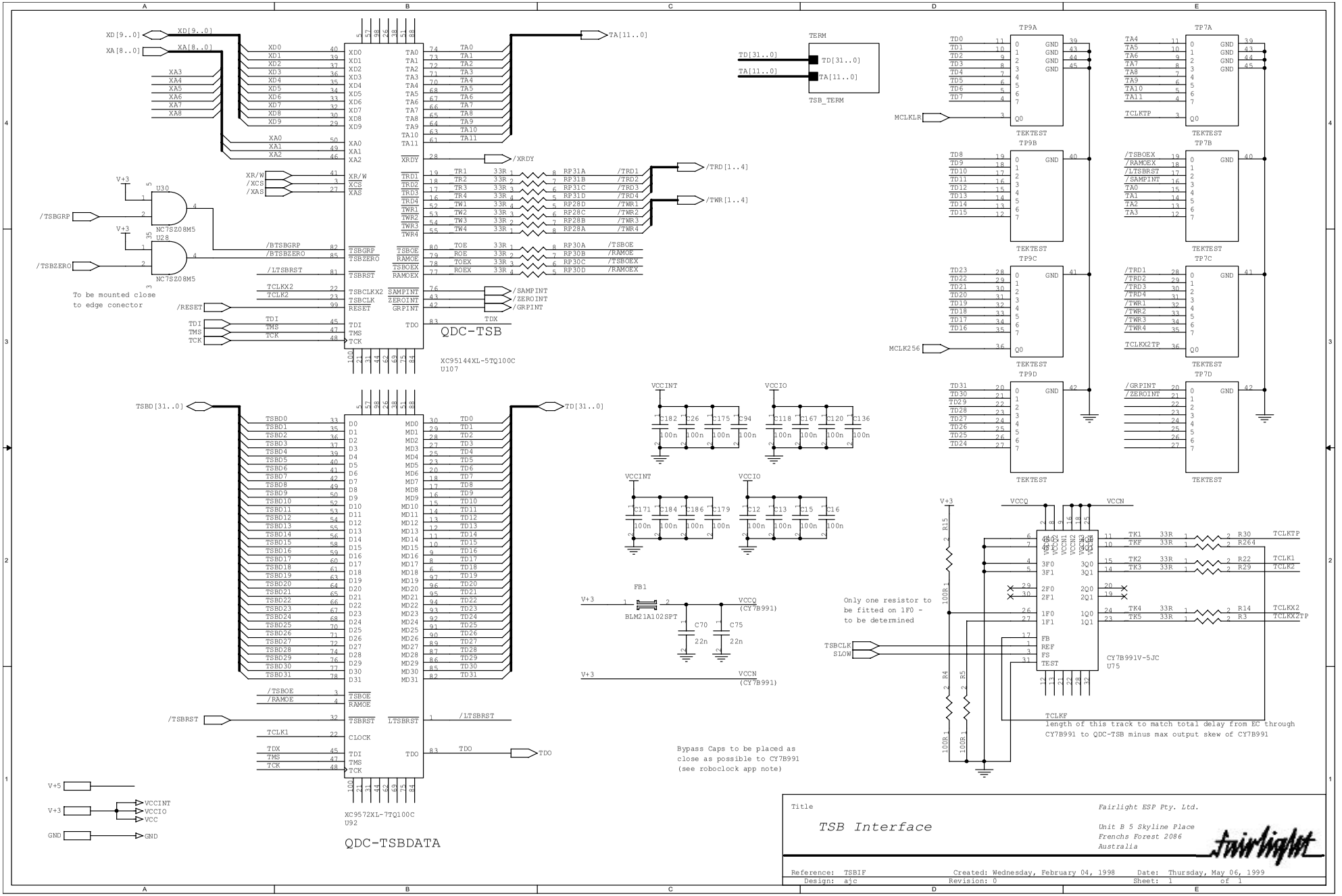
Reference: SHARC:TOP/RIGHT/SEC Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999

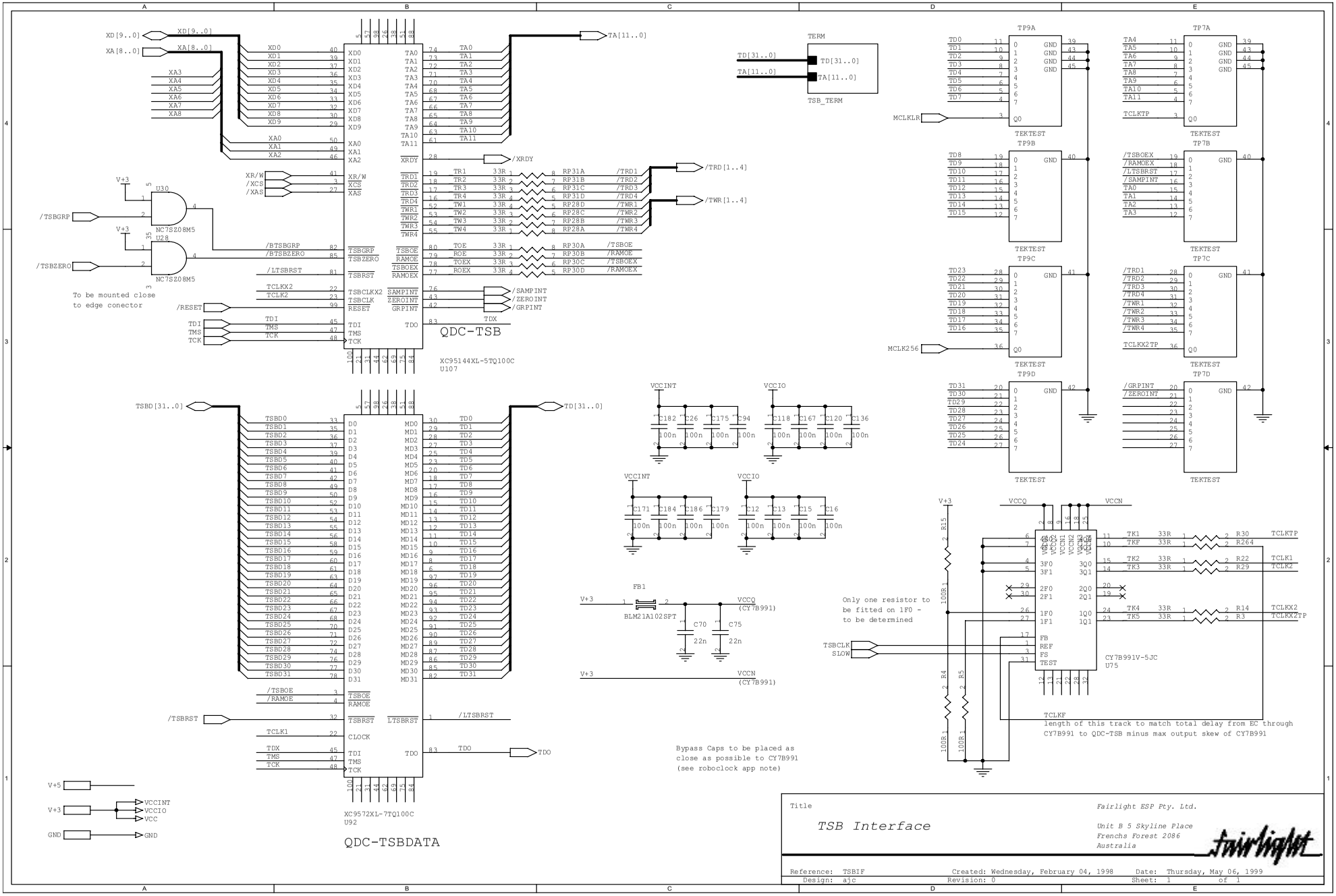
Design: ajc Revision: 0 Sheet: 1 of 1


LEFT
RIGHT
SECTION
QDC-SUPP
U156
XCS10XL-4TQ144C
note 1: fit only if XC4005XL-3TQ144 part used
HCMS-2902
U68
HCMS-2902
U74
One LED Display near each DSP Section
SOCKET 12p DIP
AUD
AUDIO
HEADER 9
DSP Group
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: GROUP:BOTTOM
Created: Thursday, June 11, 1998
Date: Friday, July 23, 1999
Design: ajc
Revision: 0
Sheet: 0 of 0


DSP DRAM Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Created: Thursday, February 12, 1998
Date: Friday, July 16, 1999
Sheet: 1 of 1
DRAM:BOTTOM/LEFT
Revision: 0
SIMM MODULE
EDO SIMM 60ns 4/8/16/32/64M 1k/2k/4k rfsh (not 8k)
S1MM Socket 72p
Test Header
Keep tracks short!
QDC-DRAM
QDC-DRAMDATA
QDC-DRAMDATA
XC95144XL-5TQ100C
XC95172XL-7TQ100C
XC95172XL-7TQ100C
Q832X245
Q832X861
HEADER 8X2

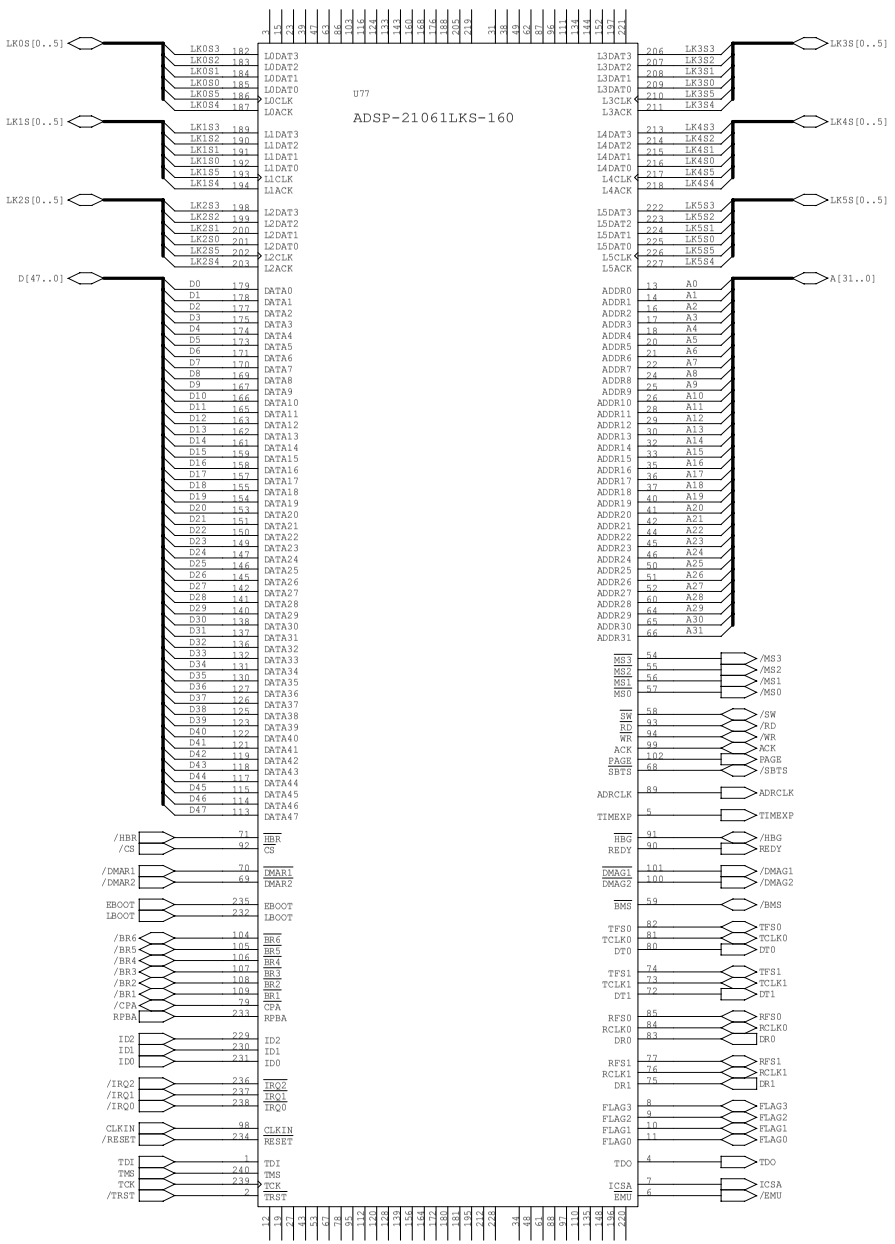

A[31..0]
SK4
SIMM Socket 72p
M4
SIMM MODULE
EDO SIMM 60ns 4/8/16/32/64M 1k/2k/4k rfsh (not 8k)
V+5
V+3
GND
VCC (DRAM, QUICKSW)
VCCINT
VCCIO
GND
VSS (DRAM)
XC95144XL-5TQ100C
U149
QDC-DRAM
TP23
HEADER 8X2
Test Header
Keep tracks short!
/PCIENB
U129
QS32X861
PA[11..0]
/PWE
/PRAS[0..1]
/PCAS[0..3]
D[47..0]
MD[31..0]
PD[31..0]
XC9572XL-7TQ100C
U137
QDC-DRAMDATA
XC9572XL-7TQ100C
U138
QDC-DRAMDATA
QS32X245
U128
QS32X245
U127
Title
DSP DRAM Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: DRAM:BOTTOM/LEFT
Created: Thursday, February 12, 1998
Date: Friday, July 16, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1

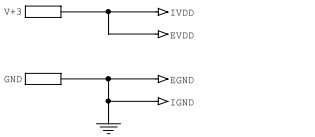

QDC-TSB
XC95144XL-5TQ100C
U107
To be mounted close
to edge conector
QDC-TSBDATA
XC9572XL-7TQ100C
U92
TERM
TSB_TERM
TEKTEST
CY7B991V-5JC
U75
Only one resistor to
be fitted on 1F0 -
to be determined
Bypass Caps to be placed as
close as possible to CY7B991
(see roboclock app note)
TCLKF
length of this track to match total delay from EC through
CY7B991 to QDC-TSB minus max output skew of CY7B991
Title
TSB Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: TSBIF
Created: Wednesday, February 04, 1998
Date: Thursday, May 06, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1

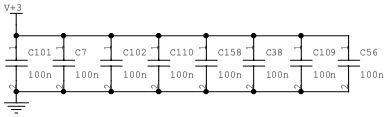

QDC-TSB
XC95144XL-5TQ100C
U107
To be mounted close
to edge conector
QDC-TSBDATA
XC9572XL-7TQ100C
U92
TERM
TSB_TERM
TP9A
TP7A
TP9B
TP7B
TP9C
TP7C
TP9D
TP7D
TEKTEST
Only one resistor to
be fitted on 1F0 -
to be determined
Bypass Caps to be placed as
close as possible to CY7B991
(see roboclock app note)
CY7B991V-5JC
U75
TCLKF
length of this track to match total delay from EC through
CY7B991 to QDC-TSB minus max output skew of CY7B991
Title
TSB Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: TSBIF
Created: Wednesday, February 04, 1998
Date: Thursday, May 06, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1

DRAFT

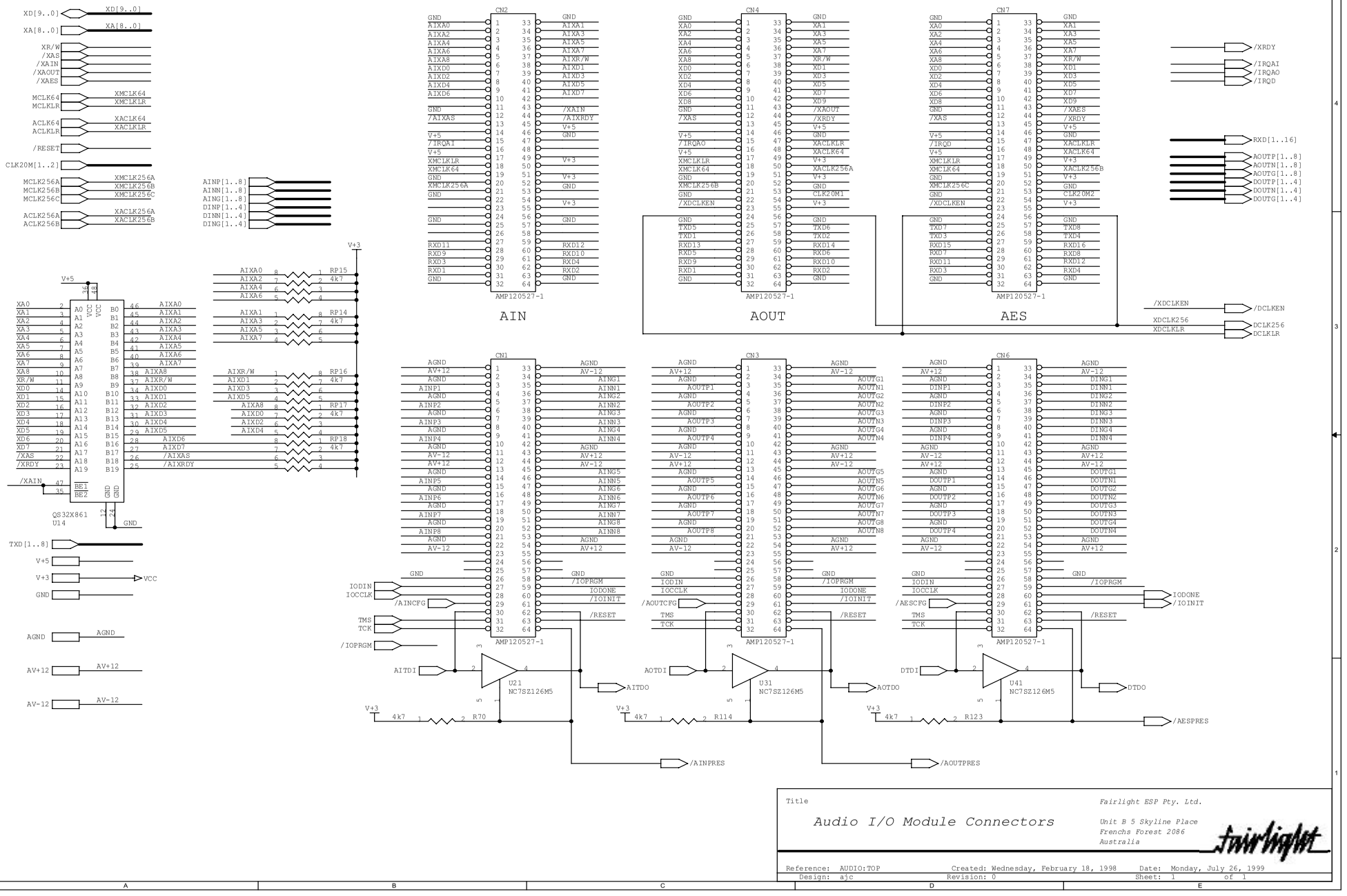
DRAFT







Title	SHARC - CPU
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	SHARC:TOP/RIGHT/PRIM
Created:	Thursday, February 12, 1998
Date:	Wednesday, May 05, 1999
Design:	ajc
Revision:	0
Sheet:	1 of 1



Title	*Audio I/O Module Connectors*
Fairlight ESP Pty. Ltd.	*Unit B 5 Skyline Place, Frenchs Forest 2086, Australia*
Reference: AUDIO:TOP	Created: Wednesday, February 18, 1998
Design: ajc	Revision: 0
Date: Monday, July 26, 1999	Sheet: 1 of 1

DRAFT

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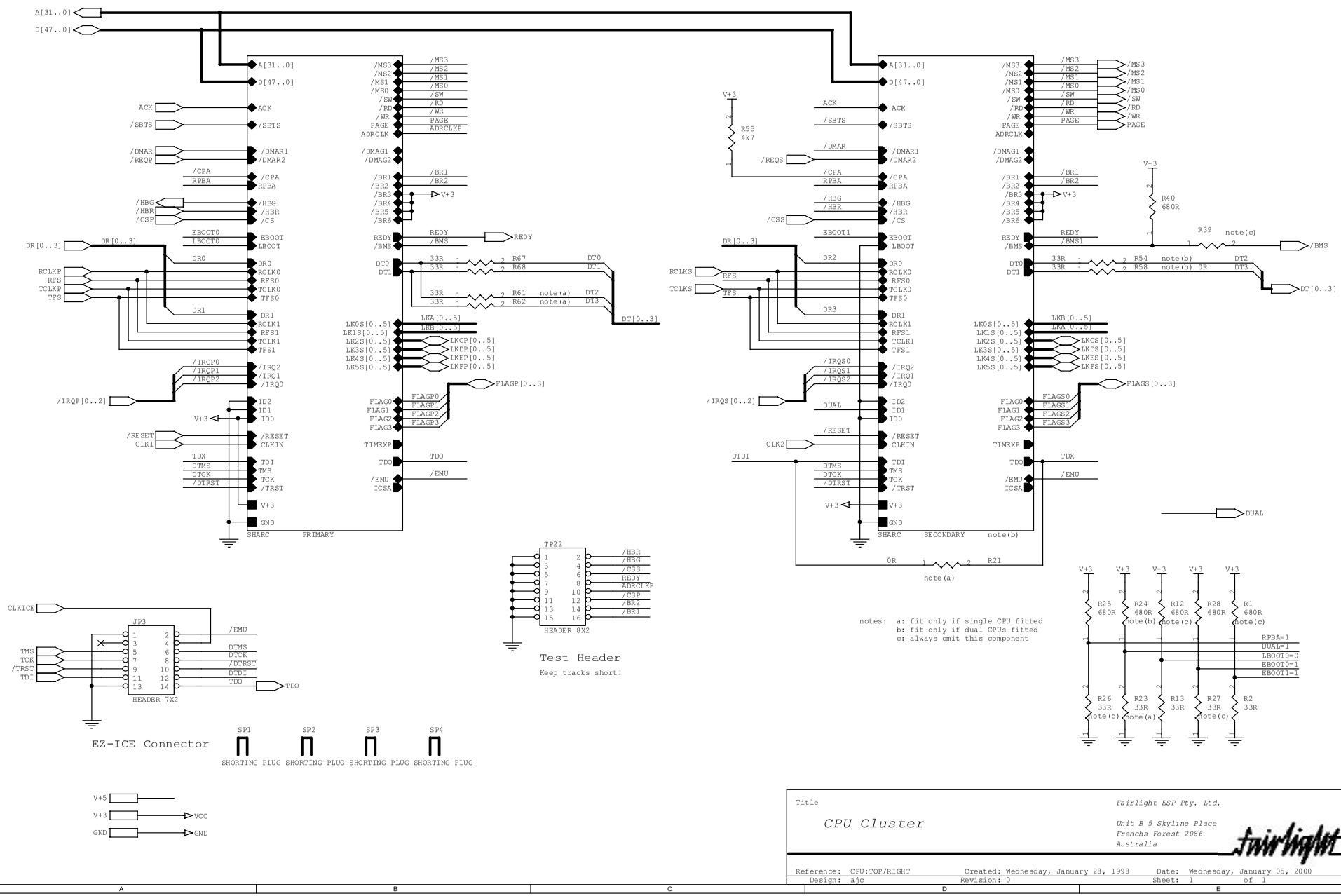


Title

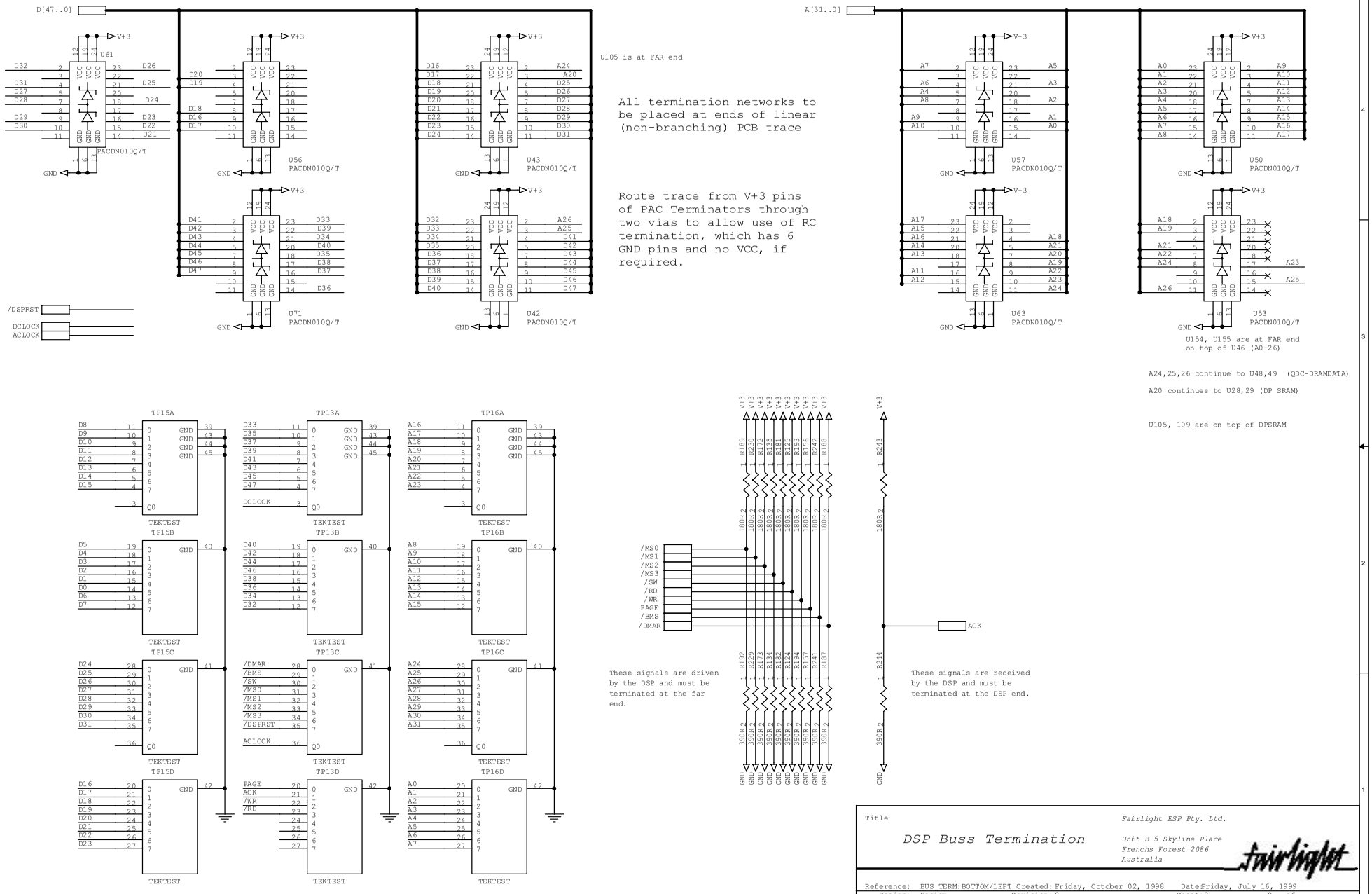
CPU Cluster

Fairlight ESP Pty. Ltd.

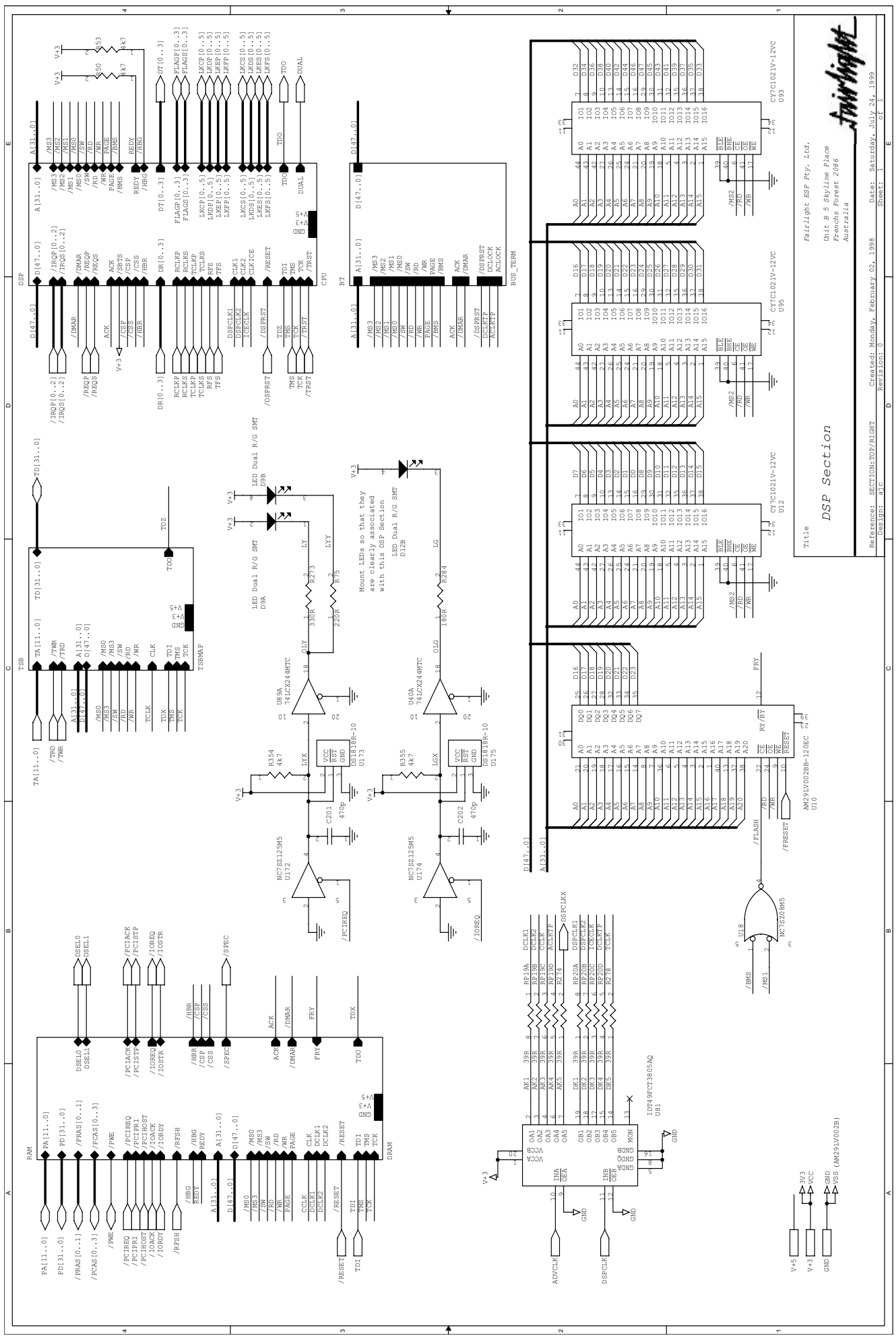
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

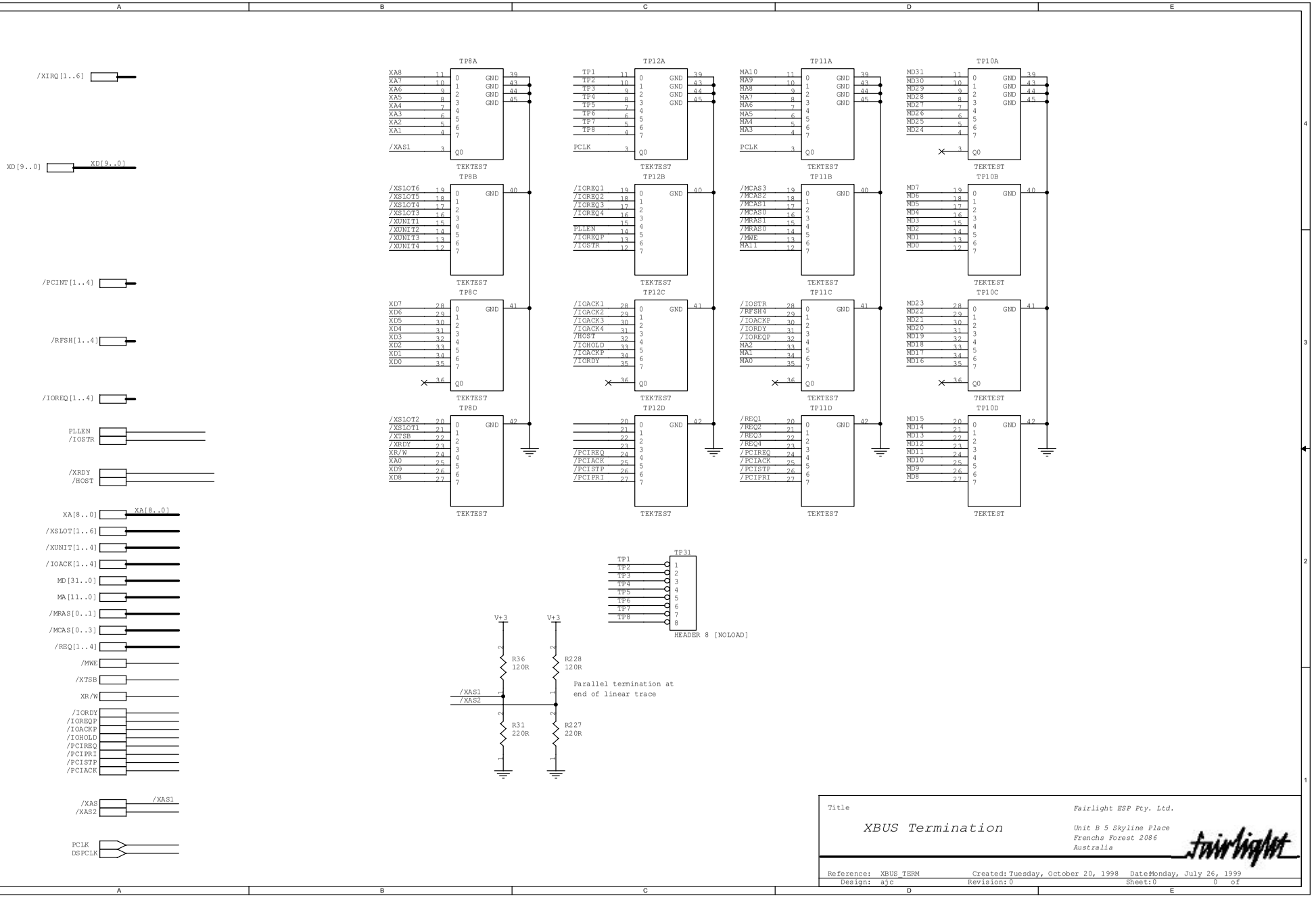
Reference: CPU:TOP/RIGHT Created: Wednesday, January 28, 1998 Date: Wednesday, January 05, 2000

Design: ajc Revision: 0 Sheet: 1 of 1



Title	*DSP Buss Termination*
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	BUS_TERM:BOTTOM/LEFT Created: Friday, October 02, 1998
Date:	Friday, July 16, 1999
Design:	Design
Revision:	0
Sheet:	0 of 0


DSP Section
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
References: SECTION:TOP/RIGHT
Design: ajc
Created: Monday, February 02, 1998
Revision: 0
Date: Saturday, July 24, 1999
Sheet: 1 of 1
DSP
CPU
BT
BUS_TERM
RAM
DRAM
TSB
TSBMAP
LED Dual R/G SMT D9A
LED Dual R/G SMT D9B
LED Dual R/G SMT D12B
Mount LEDs so that they are clearly associated with this DSP Section
U89A 74LCX244MTC
U40A 74LCX244MTC
DS18118R-10 U173
DS18118R-10 U175
NC7SZ125M5 U172
NC7SZ125M5 U174
CY7C1021V-12VC U12
CY7C1021V-12VC U95
CY7C1021V-12VC U93
AM29LV002BB-120EC U10
IDT49FCT3805AQ U81
NC7SZ08M5 U18



Title

XBUS Termination

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: XBUS_TERM Created: Tuesday, October 20, 1998 Date: Monday, July 26, 1999
Design: ajc Revision: 0 Sheet: 0 0 of

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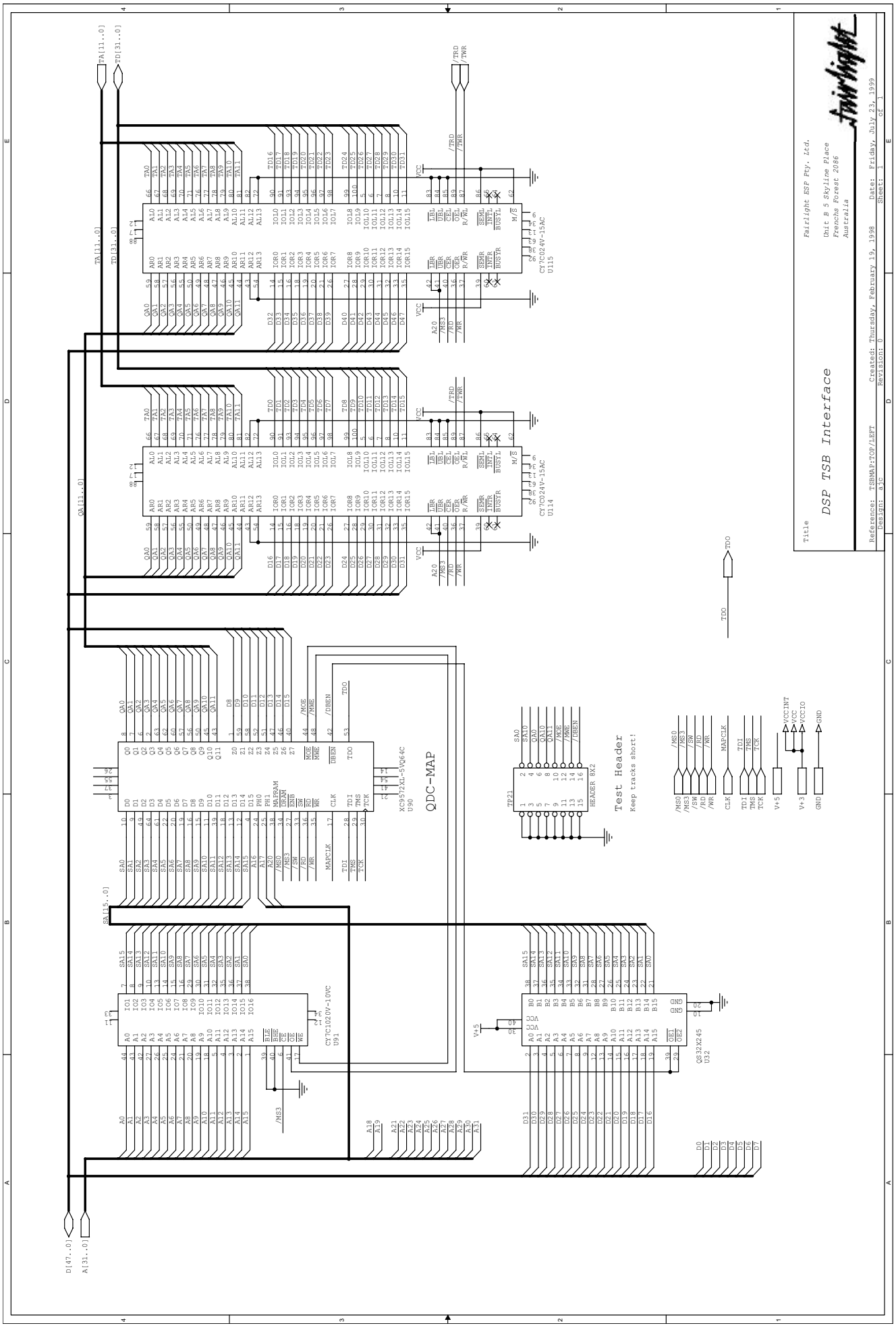
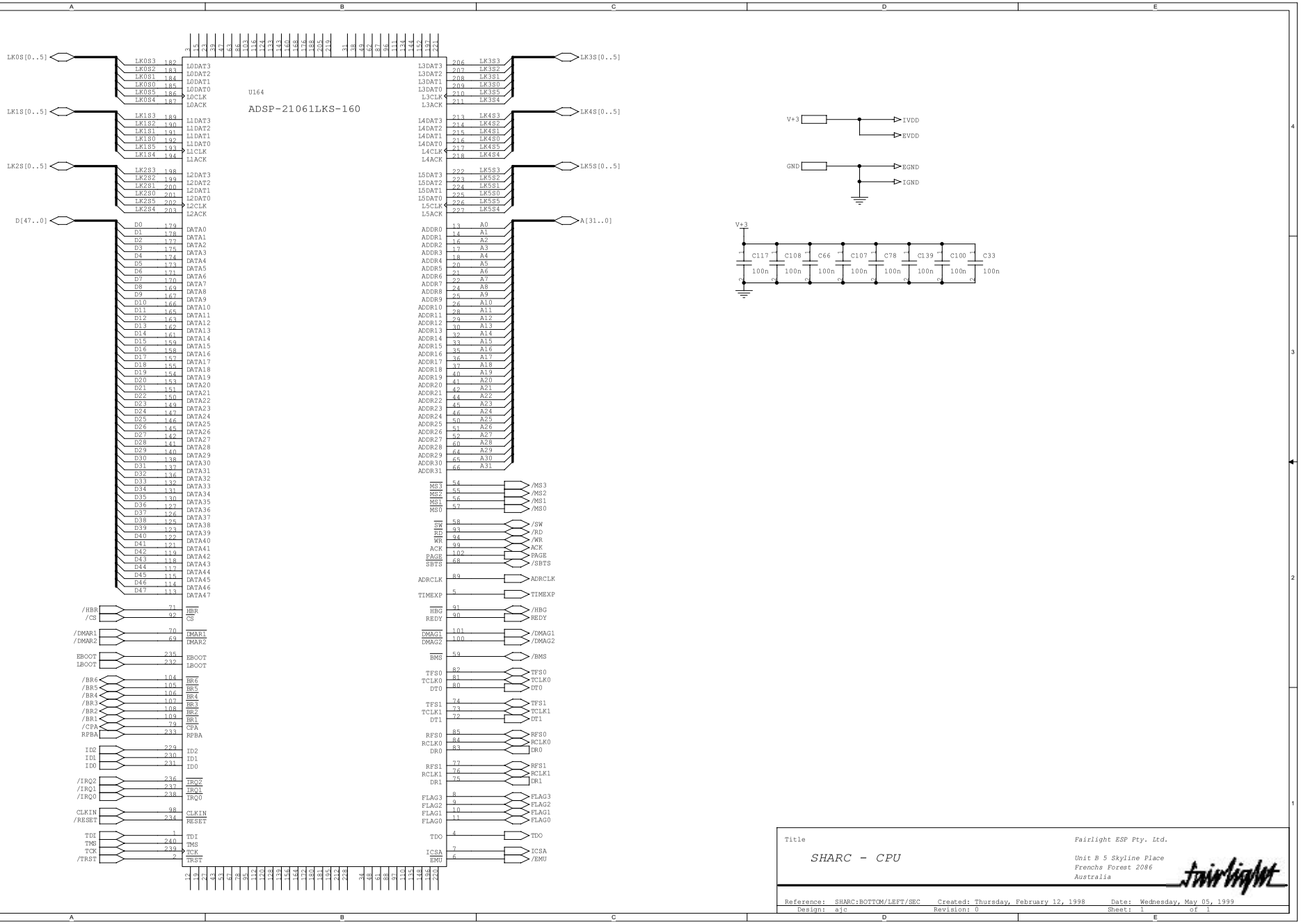
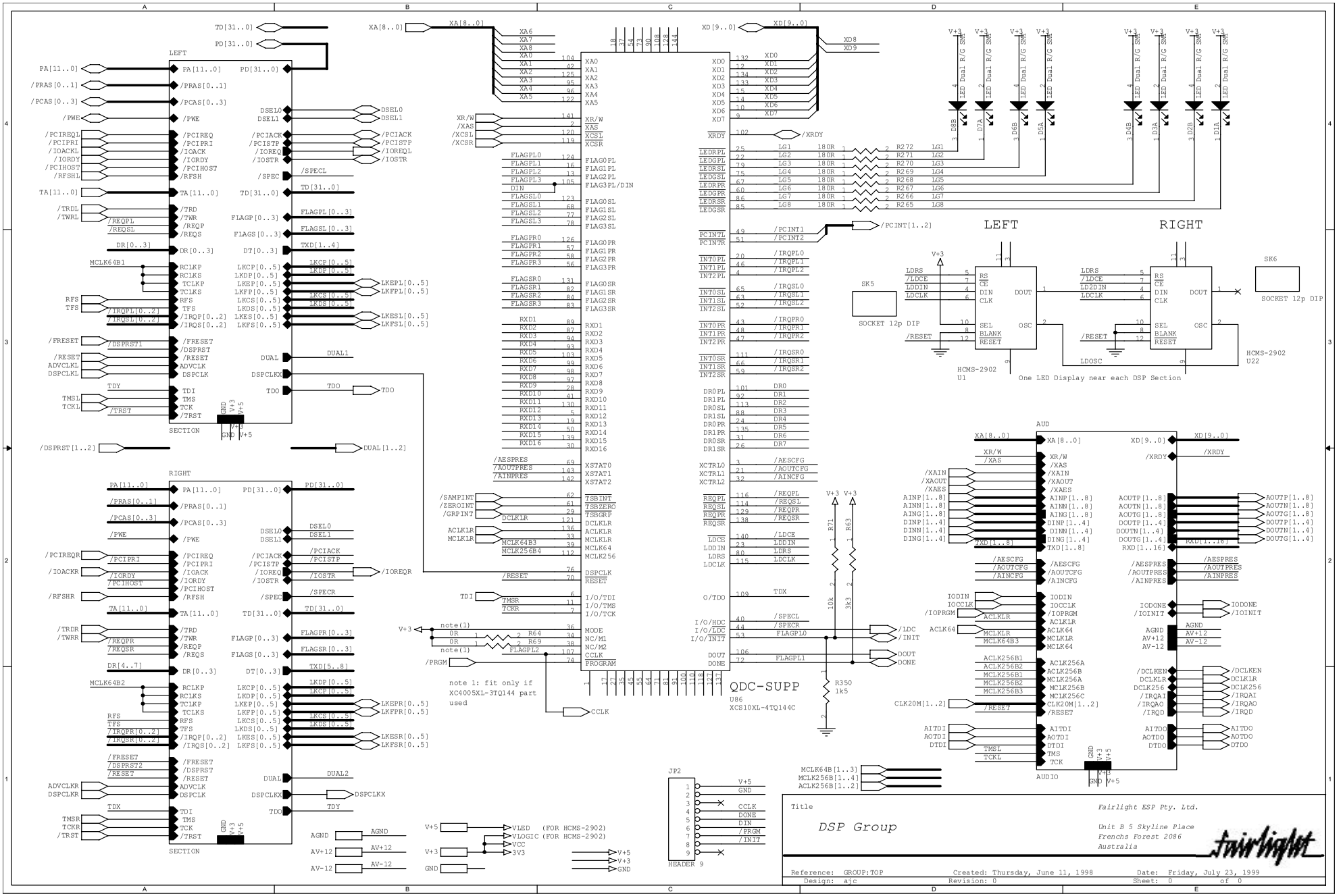
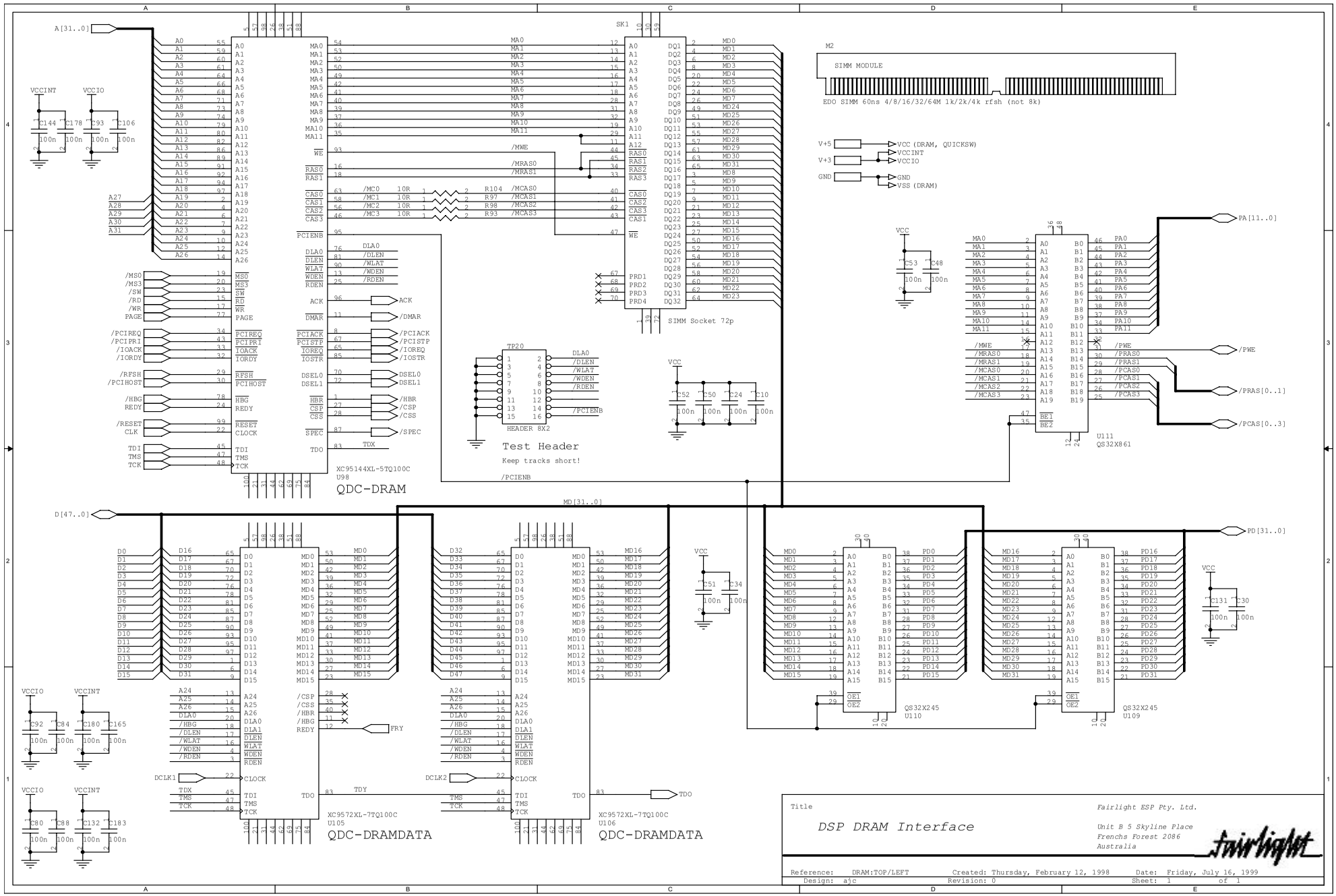
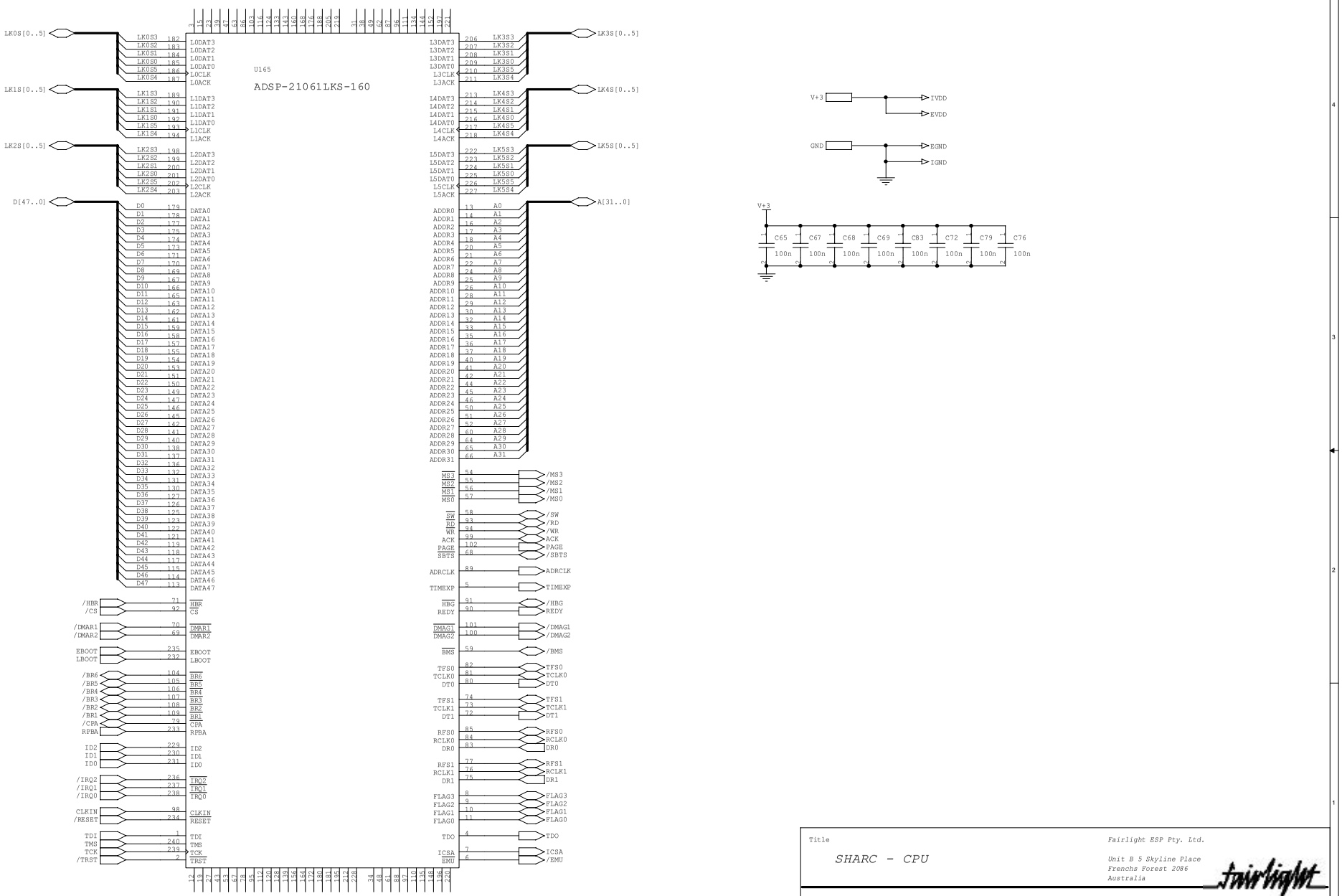

DSP TSB Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: TSBMAP7OP/LEFT
Created: Thursday, February 19, 1998
Date: Friday, July 23, 1999
Revision: 0
Sheet: 1 of 1
Design: gjc
QDC-MAP
XC9572XL-5VQ64C
U90
CY7C1020V-10VC
U91
CY7C024V-15AC
U114
CY7C024V-15AC
U115
QS32X245
U32
Test Header
Keep tracks short!
HEADER 8X2
TP21
TA[11..0]
TD[31..0]
QA[11..0]
SA[15..0]
D[47..0]
A[31..0]
/TRD
/TWR
/MS0
/MS3
/SW
/RD
/WR
MAPCLK
TDI
TMS
TCK
TDO
/DBEN
/MODE
/MWE
V+5
V+3
VCCINT
VCCIO
GND


U164
ADSP-21061LKS-160
LK0S[0..5]
LK1S[0..5]
LK2S[0..5]
D[47..0]
LK3S[0..5]
LK4S[0..5]
LK5S[0..5]
A[31..0]
V+3
IVDD
EVDD
GND
EGND
IGND
C117 100n
C108 100n
C66 100n
C107 100n
C78 100n
C139 100n
C100 100n
C33 100n
Title
SHARC - CPU
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: SHARC:BOTTOM/LEFT/SEC
Created: Thursday, February 12, 1998
Date: Wednesday, May 05, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1


QDC-SUPP
U86
XCS10XL-4TQ144C
LEFT
SECTION
RIGHT
SECTION
HCMS-2902
U1
HCMS-2902
U22
One LED Display near each DSP Section
SOCKET 12p DIP
SOCKET 12p DIP
AUD
AUDIO
JP2
HEADER 9
note 1: fit only if XC4005XL-3TQ144 part used
Title
DSP Group
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: GROUP:TOP
Created: Thursday, June 11, 1998
Date: Friday, July 23, 1999
Design: ajc
Revision: 0
Sheet: 0 of 0


A[31..0]
SK1
SIMM Socket 72p
M2
SIMM MODULE
EDO SIMM 60ns 4/8/16/32/64M 1k/2k/4k rfsh (not 8k)
V+5
V+3
GND
VCC (DRAM, QUICKSW)
VCCINT
VCCIO
GND
VSS (DRAM)
PA[11..0]
/PWE
/PRAS[0..1]
/PCAS[0..3]
U111
QS32X861
TP20
HEADER 8X2
Test Header
Keep tracks short!
/PCIENB
XC95144XL-5TQ100C
U98
QDC-DRAM
D[47..0]
MD[31..0]
PD[31..0]
QS32X245
U110
QS32X245
U109
DCLK1
DCLK2
FRY
TDX
TDY
TDO
XC9572XL-7TQ100C
U105
QDC-DRAMDATA
XC9572XL-7TQ100C
U106
QDC-DRAMDATA
Title
DSP DRAM Interface
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: DRAM:TOP/LEFT
Created: Thursday, February 12, 1998
Date: Friday, July 16, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1



Title

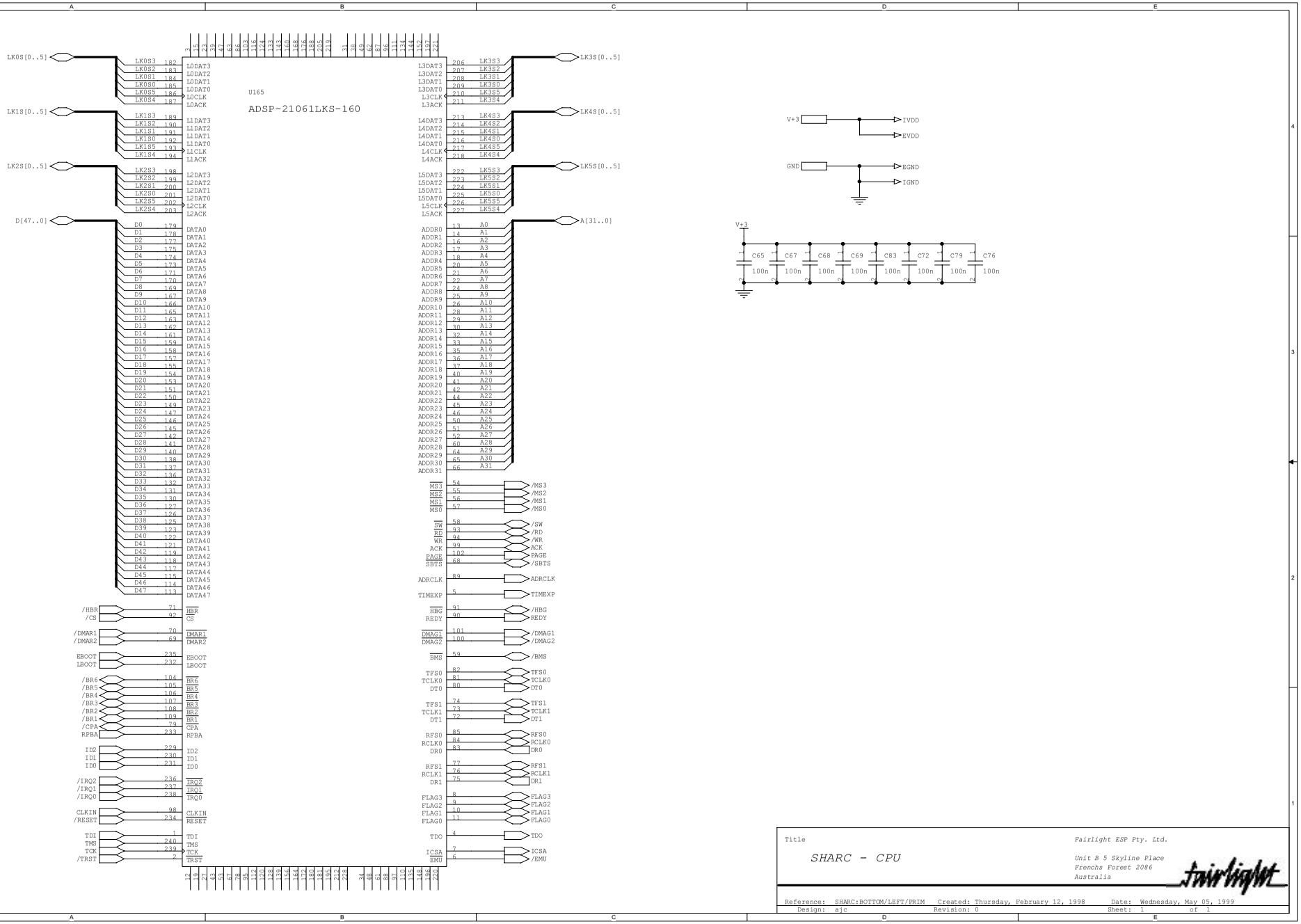
SHARC - CPU

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: SHARC:BOTTOM/LEFT/PRIM Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999

Design: ajc Revision: 0 Sheet: 1 of 1



Title

SHARC - CPU

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: SHARC:BOTTOM/LEFT/PRIM Created: Thursday, February 12, 1998 Date: Wednesday, May 05, 1999
Design: ajc Revision: 0 Sheet: 1 of 1

DRAFT

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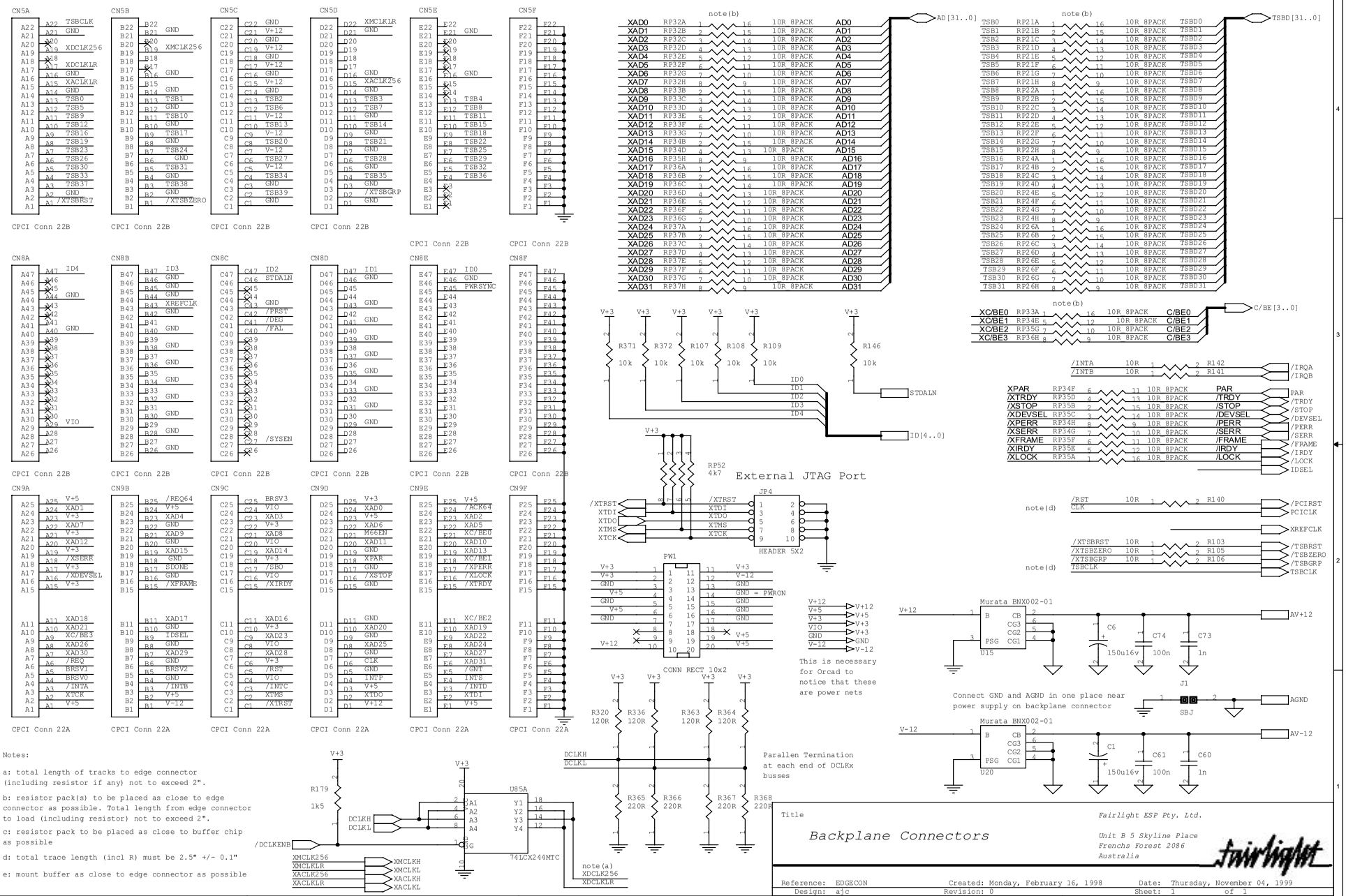


Notes:

a: total length of tracks to edge connector (including resistor if any) not to exceed 2".

b: resistor pack(s) to be placed as close to edge connector as possible. Total length from edge connector to load (including resistor) not to exceed 2".

c: resistor pack to be placed as close to buffer chip as possible

d: total trace length (incl R) must be 2.5" +/- 0.1"

e: mount buffer as close to edge connector as possible

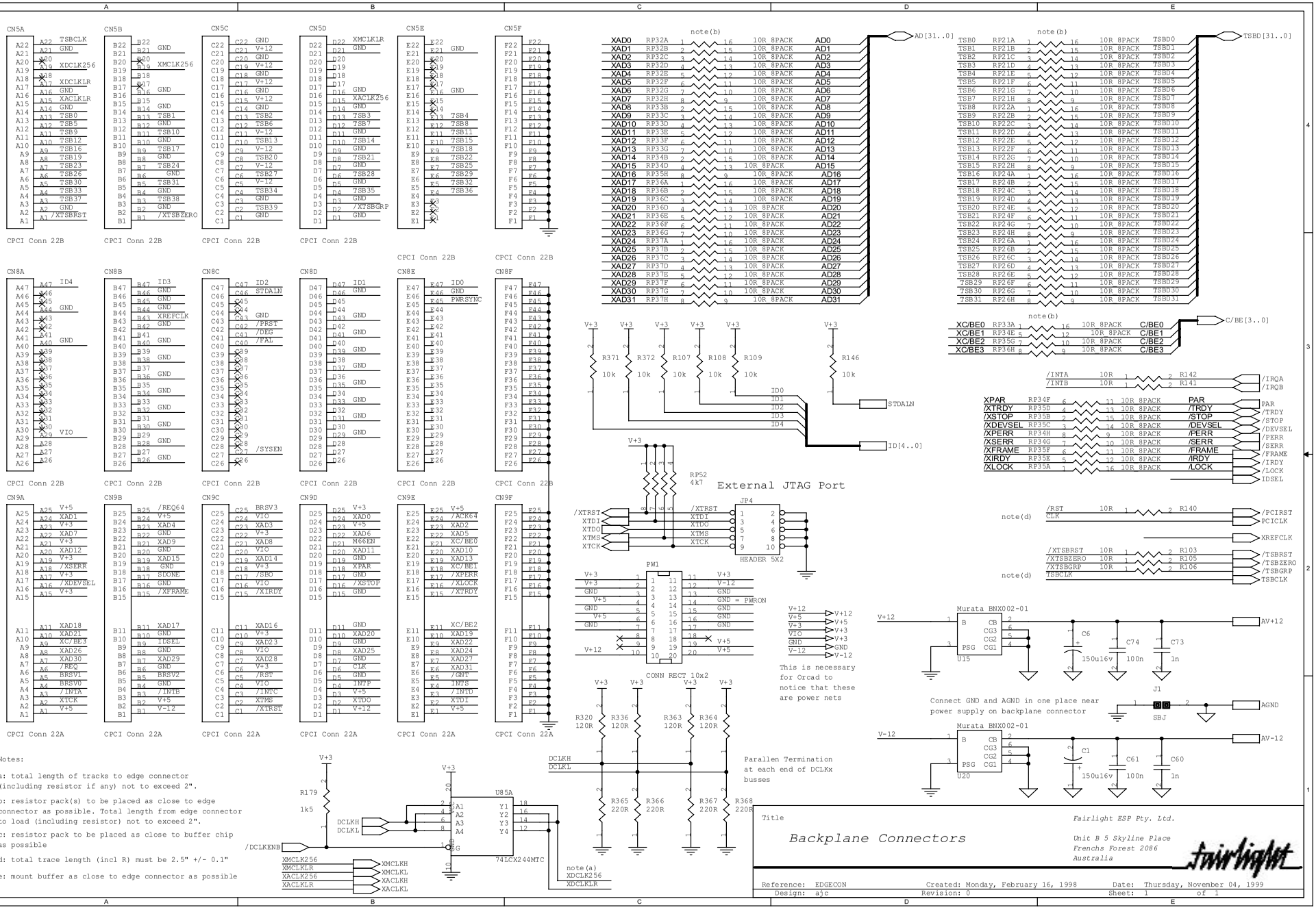
Title

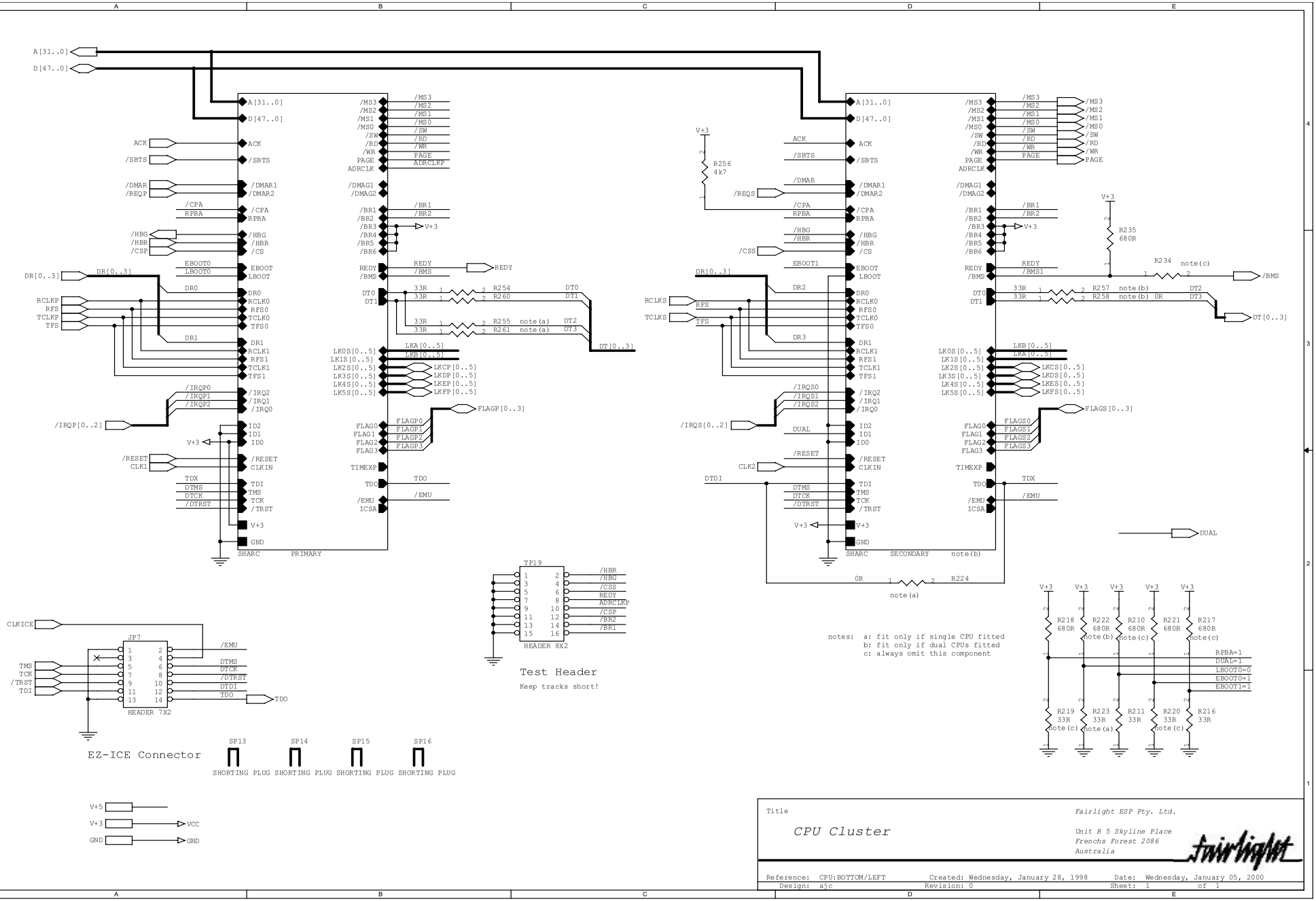
Backplane Connectors

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: EDGECON
Design: ajc
Created: Monday, February 16, 1998
Revision: 0
Date: Thursday, November 04, 1999
Sheet: 1 of 1


CN5A
CN5B
CN5C
CN5D
CN5E
CN5F
CPCI Conn 22B
CN8A
CN8B
CN8C
CN8D
CN8E
CN8F
CN9A
CN9B
CN9C
CN9D
CN9E
CN9F
CPCI Conn 22A
TSBCLK
XDCLK256
XMCLK256
XDCLKLR
XACLKLR
XMCLKLR
XACLK256
/XTSBSRST
/XTSBZERO
/XTSBGRP
/SYSEN
VIO
V+5
V+3
V+12
V-12
GND
note(b)
AD[31..0]
TSBD[31..0]
C/BE[3..0]
XAD0 RP32A
XAD1 RP32B
XAD2 RP32C
XAD3 RP32D
XAD4 RP32E
XAD5 RP32F
XAD6 RP32G
XAD7 RP32H
XAD8 RP33B
XAD9 RP33C
XAD10 RP33D
XAD11 RP33E
XAD12 RP33F
XAD13 RP33G
XAD14 RP34B
XAD15 RP34D
XAD16 RP35H
XAD17 RP36A
XAD18 RP36B
XAD19 RP36C
XAD20 RP36D
XAD21 RP36E
XAD22 RP36F
XAD23 RP36G
XAD24 RP37A
XAD25 RP37B
XAD26 RP37C
XAD27 RP37D
XAD28 RP37E
XAD29 RP37F
XAD30 RP37G
XAD31 RP37H
10R 8PACK
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
AD8
AD9
AD10
AD11
AD12
AD13
AD14
AD15
AD16
AD17
AD18
AD19
AD20
AD21
AD22
AD23
AD24
AD25
AD26
AD27
AD28
AD29
AD30
AD31
TSB0 RP21A
TSB1 RP21B
TSB2 RP21C
TSB3 RP21D
TSB4 RP21E
TSB5 RP21F
TSB6 RP21G
TSB7 RP21H
TSB8 RP22A
TSB9 RP22B
TSB10 RP22C
TSB11 RP22D
TSB12 RP22E
TSB13 RP22F
TSB14 RP22G
TSB15 RP22H
TSB16 RP24A
TSB17 RP24B
TSB18 RP24C
TSB19 RP24D
TSB20 RP24E
TSB21 RP24F
TSB22 RP24G
TSB23 RP24H
TSB24 RP26A
TSB25 RP26B
TSB26 RP26C
TSB27 RP26D
TSB28 RP26E
TSB29 RP26F
TSB30 RP26G
TSB31 RP26H
TSBD0
TSBD1
TSBD2
TSBD3
TSBD4
TSBD5
TSBD6
TSBD7
TSBD8
TSBD9
TSBD10
TSBD11
TSBD12
TSBD13
TSBD14
TSBD15
TSBD16
TSBD17
TSBD18
TSBD19
TSBD20
TSBD21
TSBD22
TSBD23
TSBD24
TSBD25
TSBD26
TSBD27
TSBD28
TSBD29
TSBD30
TSBD31
XC/BE0 RP33A
XC/BE1 RP34E
XC/BE2 RP35G
XC/BE3 RP36H
C/BE0
C/BE1
C/BE2
C/BE3
R371 10k
R372 10k
R107 10k
R108 10k
R109 10k
R146 10k
ID0
ID1
ID2
ID3
ID4
STDALN
ID[4..0]
/INTA
/INTB
R142
R141
/IRQA
/IRQB
XPAR RP34F
/XTRDY RP35D
/XSTOP RP35B
/XDEVSEL RP35C
/XPERR RP34H
/XSERR RP34G
/XFRAME RP35F
/XIRDY RP35E
/XLOCK RP35A
PAR
/TRDY
/STOP
/DEVSEL
/PERR
/SERR
/FRAME
/IRDY
/LOCK
IDSEL
RP52 4k7
External JTAG Port
/XTRST
XTDI
XTDO
XTMS
XTCK
JP4
HEADER 5X2
PW1
CONN RECT 10x2
GND = PWRON
This is necessary for Orcad to notice that these are power nets
/RST
CLK
R140
/PCIRST
PCICLK
XREFCLK
/XTSBRST
/XTSBZERO
/XTSBGRP
TSBCLK
R103
R105
R106
/TSBRST
/TSBZERO
/TSBGRP
/TSBCLK
note(d)
Murata BNX002-01
U15
U20
C6 150u16v
C74 100n
C73 1n
C1 150u16v
C61 100n
C60 1n
AV+12
AV-12
Connect GND and AGND in one place near power supply on backplane connector
J1
SBJ
AGND
R320 120R
R336 120R
R363 120R
R364 120R
R365 220R
R366 220R
R367 220R
R368 220R
Parallen Termination at each end of DCLKx busses
DCLKH
DCLKL
R179 1k5
/DCLKENB
U85A
74LCX244MTC
note(a)
XDCLK256
XDCLKLR
XMCLKH
XMCLKL
XACLKH
XACLKL
Notes:
a: total length of tracks to edge connector (including resistor if any) not to exceed 2".
b: resistor pack(s) to be placed as close to edge connector as possible. Total length from edge connector to load (including resistor) not to exceed 2".
c: resistor pack to be placed as close to buffer chip as possible
d: total trace length (incl R) must be 2.5" +/- 0.1"
e: mount buffer as close to edge connector as possible
Title
Backplane Connectors
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: EDGECON
Created: Monday, February 16, 1998
Date: Thursday, November 04, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1



Title

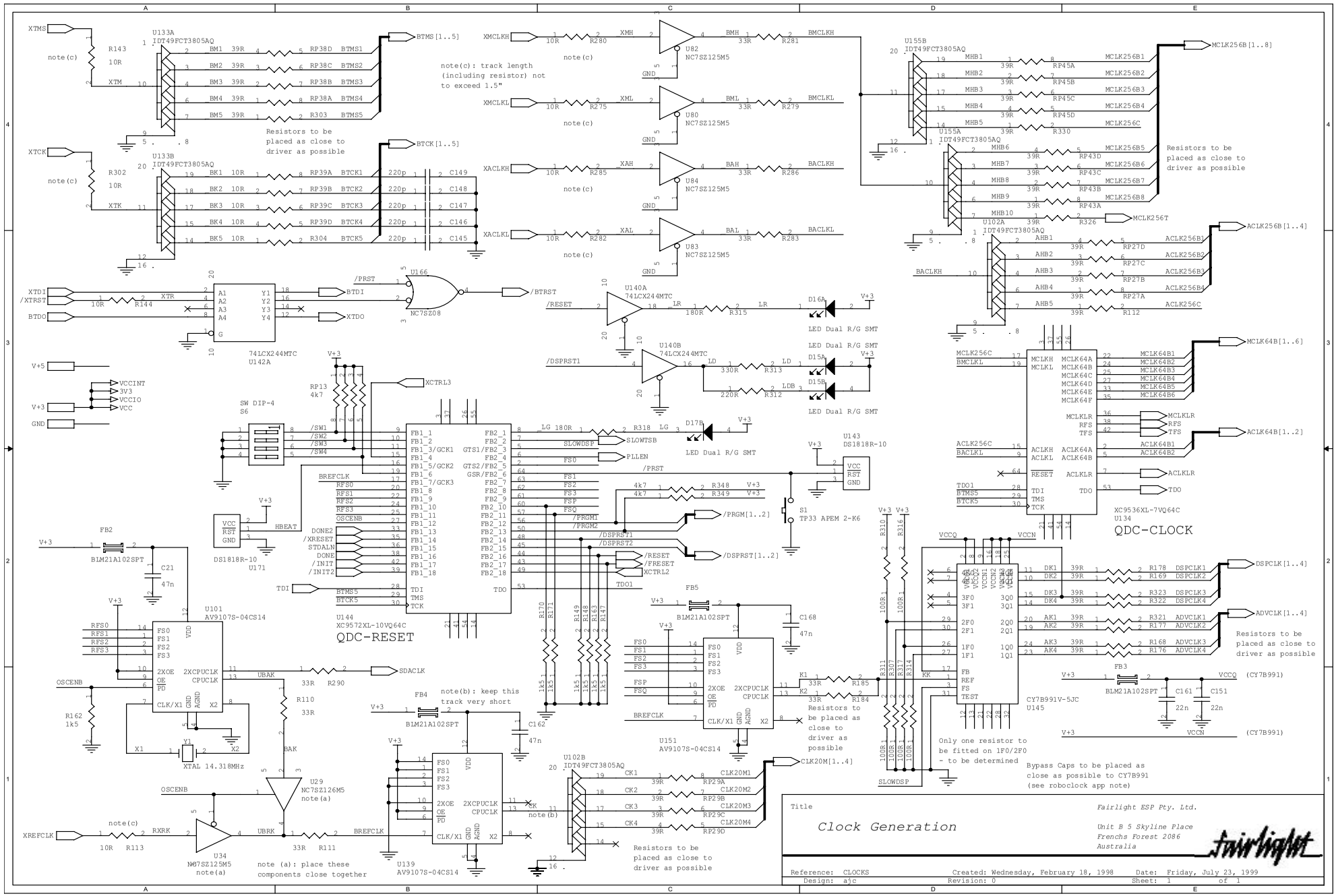
CPU Cluster

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: CPU:BOTTOM/LEFT Created: Wednesday, January 28, 1998 Date: Wednesday, January 05, 2000

Design: ajc Revision: 0 Sheet: 1 of 1


Clock Generation
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: CLOCKS
Created: Wednesday, February 18, 1998
Date: Friday, July 23, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1
QDC-RESET
QDC-CLOCK
note(c): track length (including resistor) not to exceed 1.5"
Resistors to be placed as close to driver as possible
note(b): keep this track very short
note (a): place these components close together
Only one resistor to be fitted on 1F0/2F0 - to be determined
Bypass Caps to be placed as close as possible to CY7B991 (see roboclock app note)
XC9572XL-10VQ64C
XC9536XL-7VQ64C
CY7B991V-5JC
AV9107S-04CS14
NC7SZ125M5
NC7SZ08
74LCX244MTC
IDT49FCT3805AQ
DS1818R-10
SW DIP-4
TP33 APEM 2-K6
LED Dual R/G SMT
BLM21A102SPT
XTAL 14.318MHz

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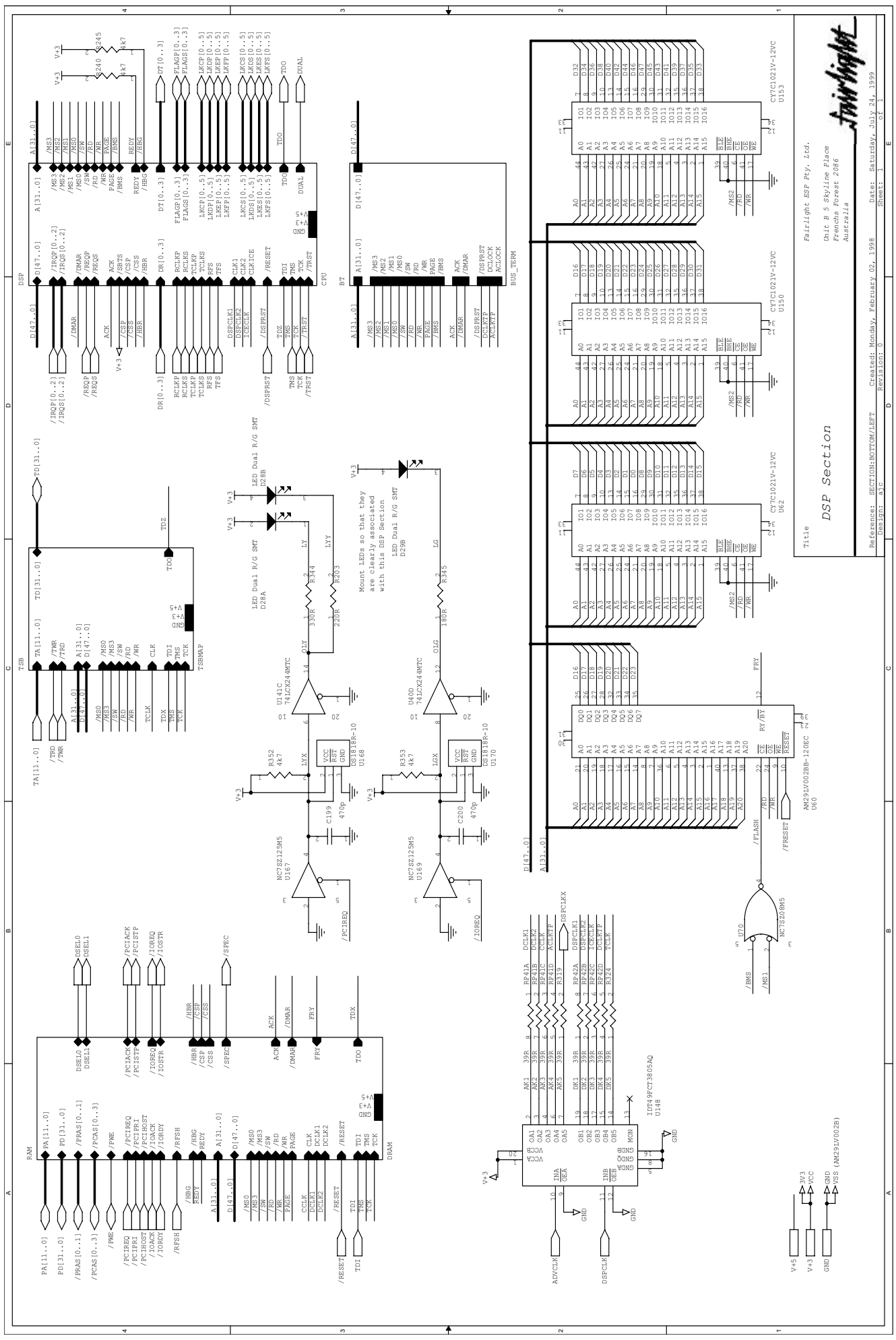
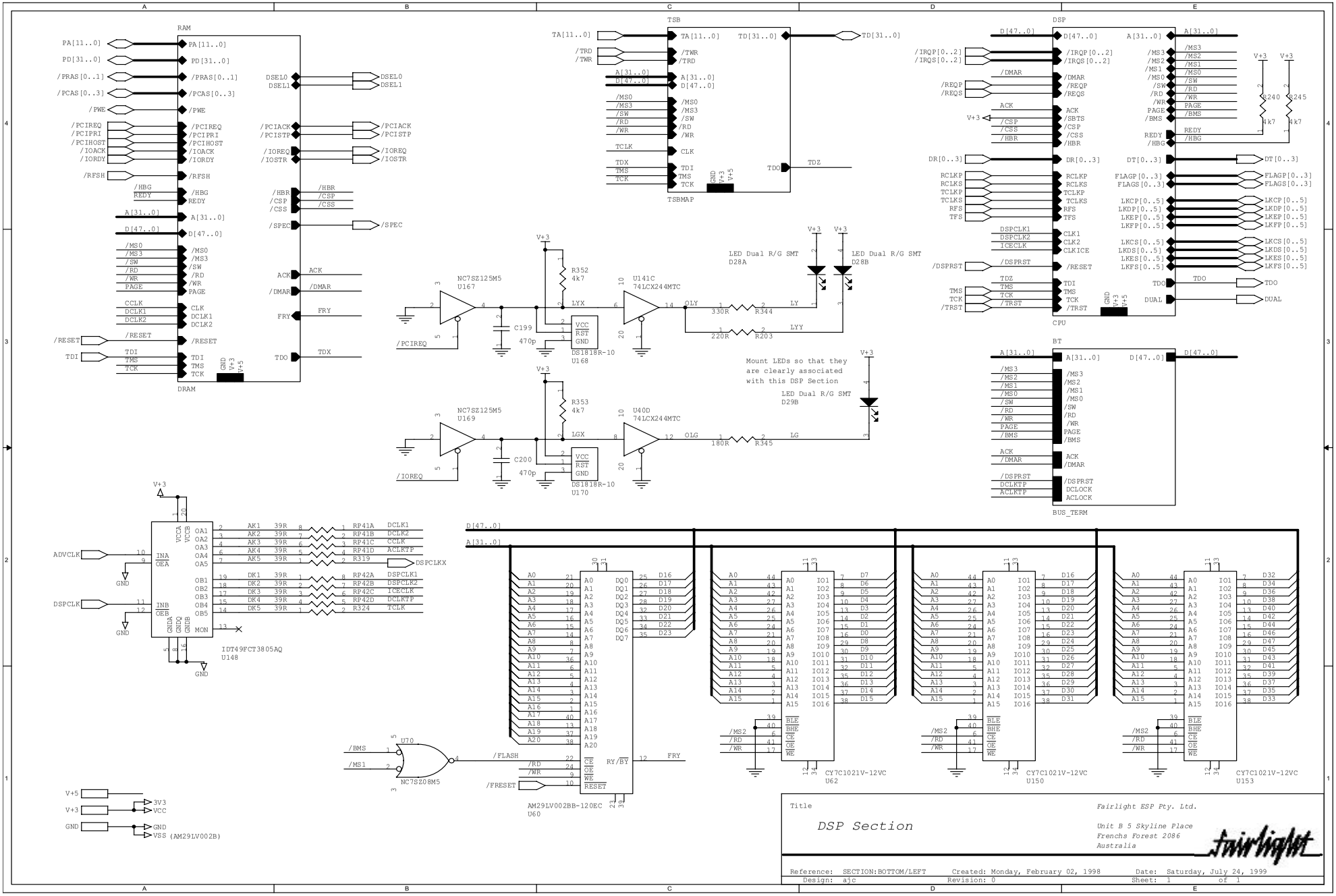
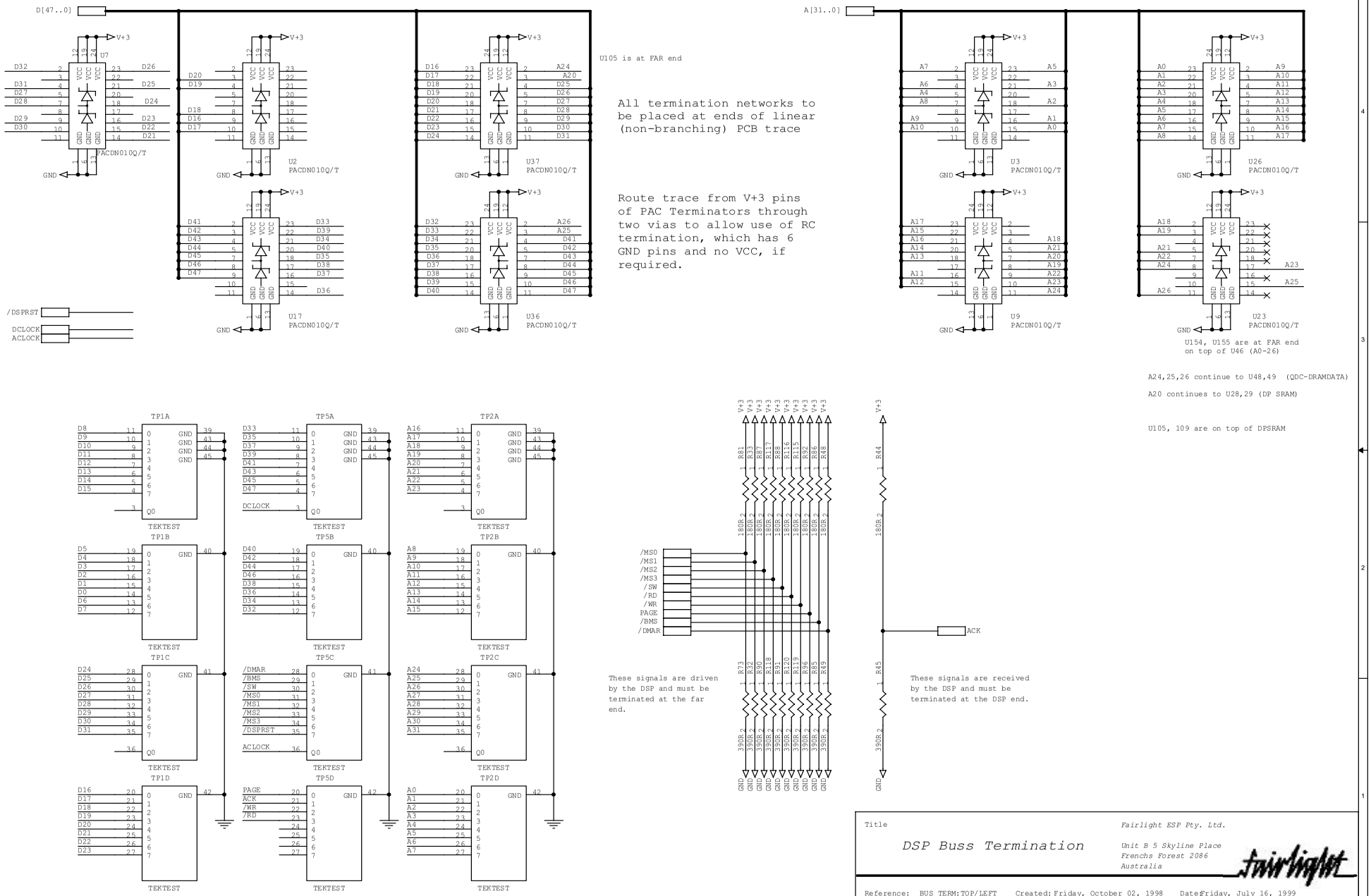

DSP Section
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
References: SECTION:BOTTOM/LEFT
Design: ajc
Created: Monday, February 02, 1998
Revision: 0
Date: Saturday, July 24, 1999
Sheet: 1 of 1
DSP
CPU
BT
TSB
TSBMAP
RAM
DRAM
BUS_TERM
LED Dual R/G SMT D28A
LED Dual R/G SMT D28B
LED Dual R/G SMT D29B
Mount LEDs so that they are clearly associated with this DSP Section
CY7C1021V-12VC U62
CY7C1021V-12VC U150
CY7C1021V-12VC U153
AM29LV002BB-120EC U60
74LCX244MTC U141C
74LCX244MTC U40D
NC7SZ125M5 U167
NC7SZ125M5 U169
DS1818R-10 U168
DS1818R-10 U170
IDT49FCT3805AQ U148
NC7SZ08M5 U70
R344 330R
R203 220R
R345 180R
R352 4k7
R353 4k7
C199 470p
C200 470p
R440 4k7
R245 4k7
RP41A 39R
RP41B 39R
RP41C 39R
RP41D 39R
RP42A 39R
RP42B 39R
RP42C 39R
RP42D 39R
R319
R324
ADVCLK
DSPCLK
V+3
V+5
GND
VCC
VSS (AM29LV002B)


RAM
DRAM
TSB
TSBMAP
DSP
CPU
BT
BUS_TERM
Mount LEDs so that they are clearly associated with this DSP Section
LED Dual R/G SMT D28A
LED Dual R/G SMT D28B
LED Dual R/G SMT D29B
IDT49FCT3805AQ U148
AM29LV002BB-120EC U60
CY7C1021V-12VC U62
CY7C1021V-12VC U150
CY7C1021V-12VC U153
NC7SZ08M5 U70
Title
DSP Section
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: SECTION:BOTTOM/LEFT
Created: Monday, February 02, 1998
Date: Saturday, July 24, 1999
Design: ajc
Revision: 0
Sheet: 1 of 1



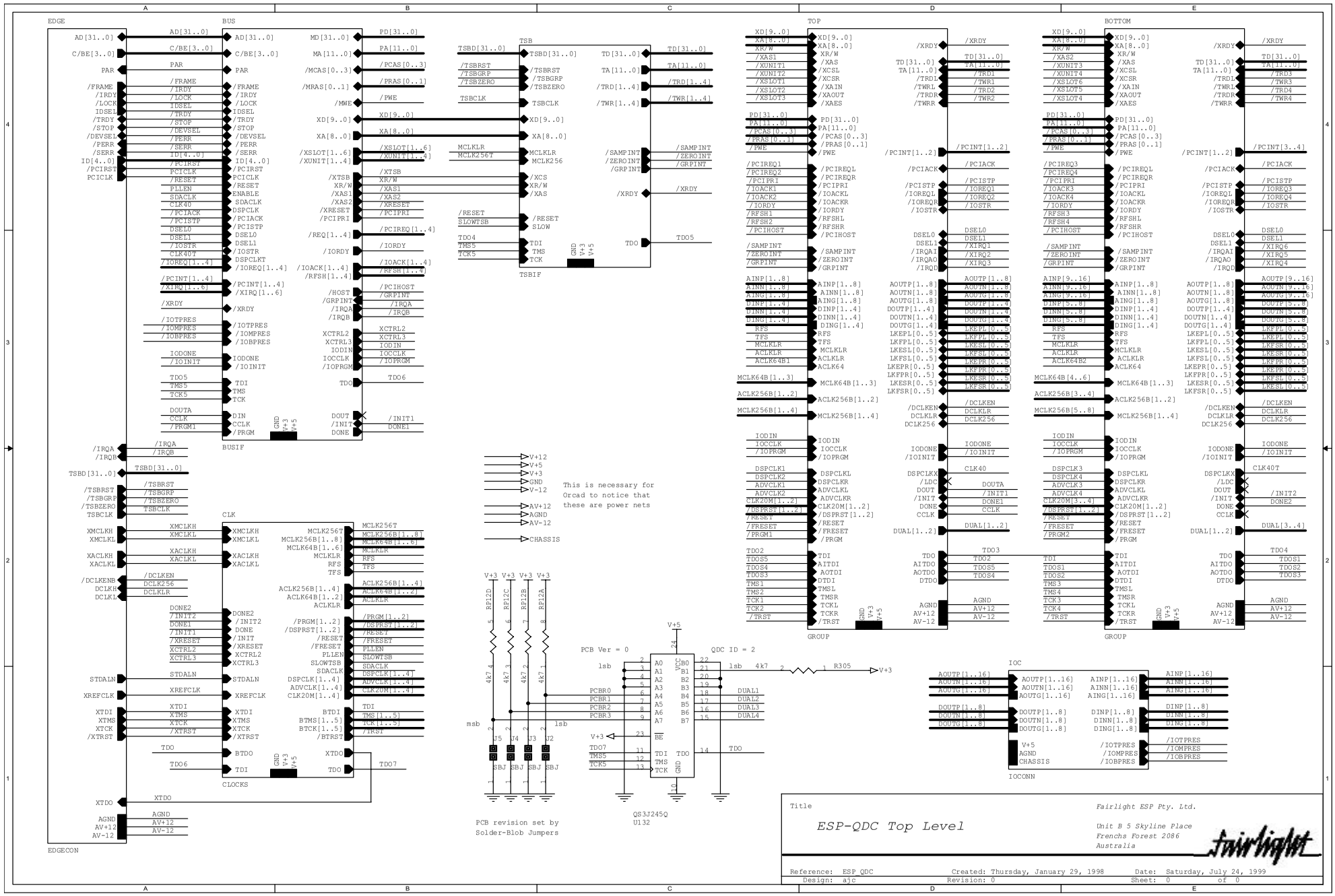
Title

DSP Buss Termination

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: BUS_TERM:TOP/LEFT Created: Friday, October 02, 1998 Date: Friday, July 16, 1999
Design: Design Revision: 0 Sheet: 0 0 of


EDGE
BUS
TSB
TOP
BOTTOM
EDGECON
BUSIF
TSBIF
GROUP
CLK
CLOCKS
IOC
IOCONN
This is necessary for Orcad to notice that these are power nets
PCB Ver = 0
QDC ID = 2
PCB revision set by Solder-Blob Jumpers
QS3J245Q U132
Title
ESP-QDC Top Level
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: ESP_QDC
Created: Thursday, January 29, 1998
Date: Saturday, July 24, 1999
Design: ajc
Revision: 0
Sheet: 0 of 0

AO1 AI1 AES1 JTAG TESTING

1. Connect the power supply to the QDC board.

2. Connect the Xilinx pod to the QDC as follows:

VCC to JP2 or JP5 pin 1
GND to JP2 or JP5 pin 2
TDI to JP4 pin 3
TDO to JP4 pin 5
TMS to JP4 pin 7
TCK to JP4 pin 9

as shown below:

	TCK	TMS	TDO	TDI	
JP4	0	0	0	0	1
JP4	0	0	0	0	0

3. Plug the AI1 under test into the QDC at position 1 and/or 6.

4. Plug the AO1 under test into the QDC at position 2 and/or 5.

5. Plug the AES1 under test into the QDC at position 3 and/or 4.

6. Switch on PSU.

7. Open a DOS window on the PC and 'CD' to C:\Mw4\jtag-qdc (Use QDC JTAG shortcut)

8. Run the command: jtag -v atest

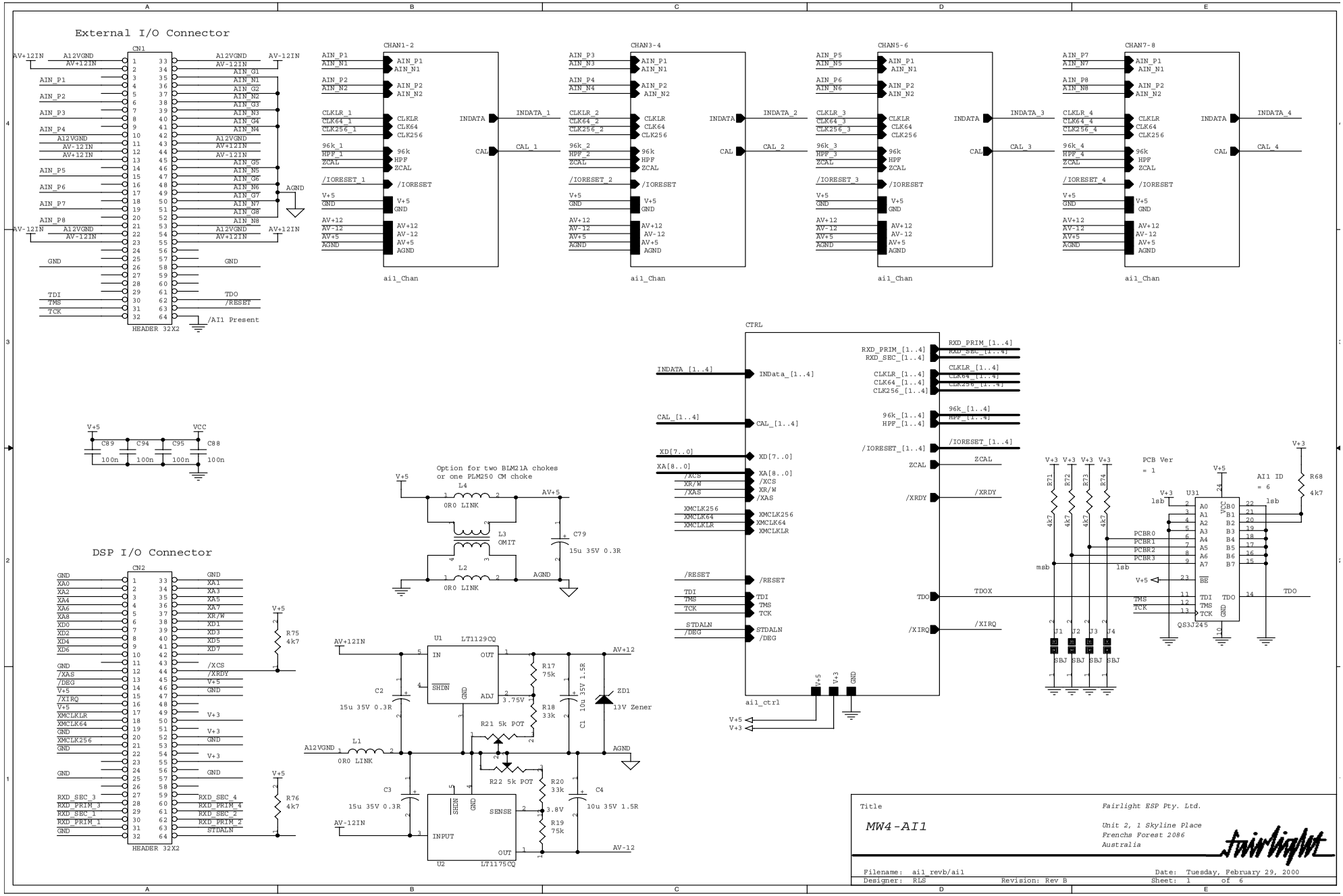
This will do the jtag testing:

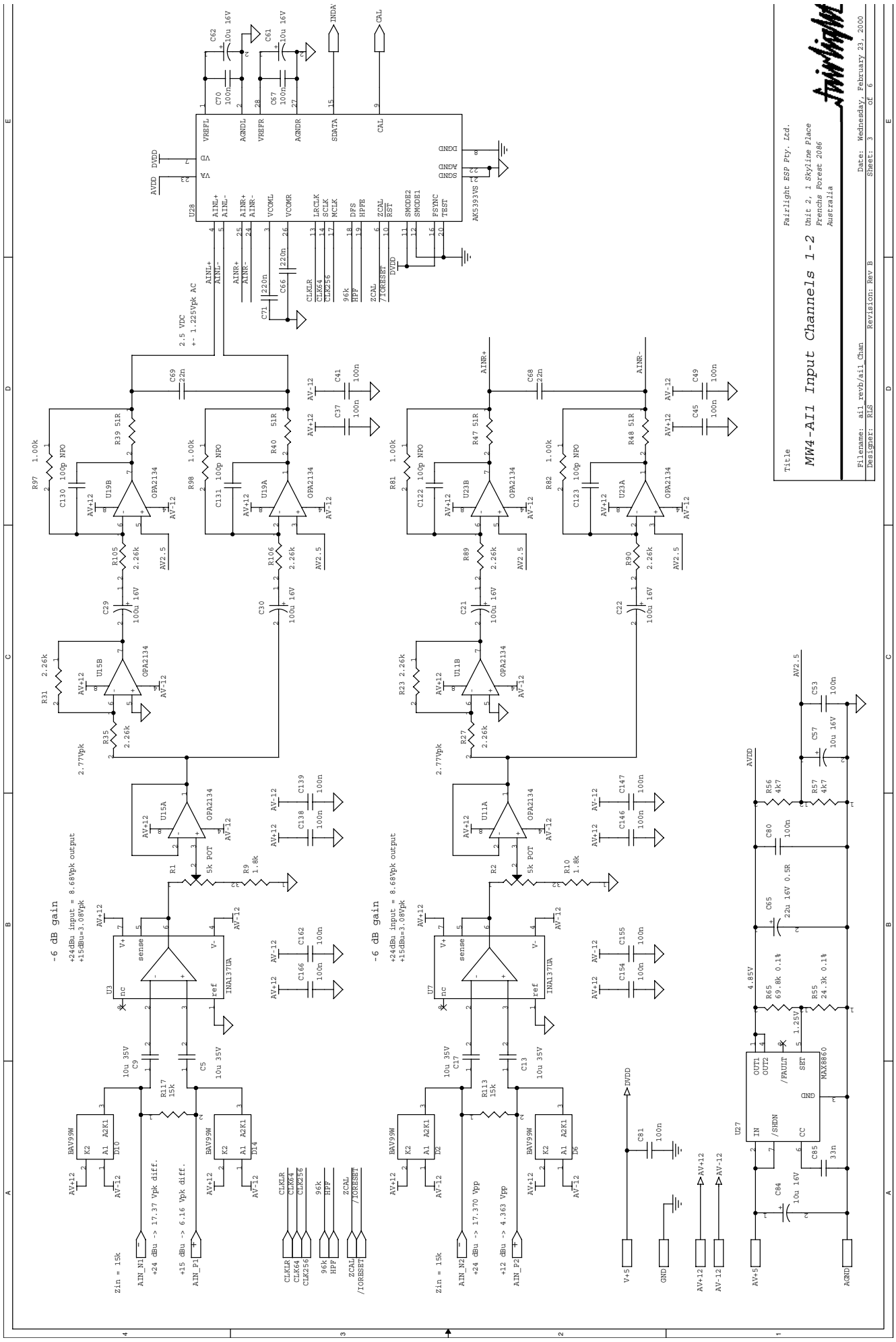
The following is for AI1 only:

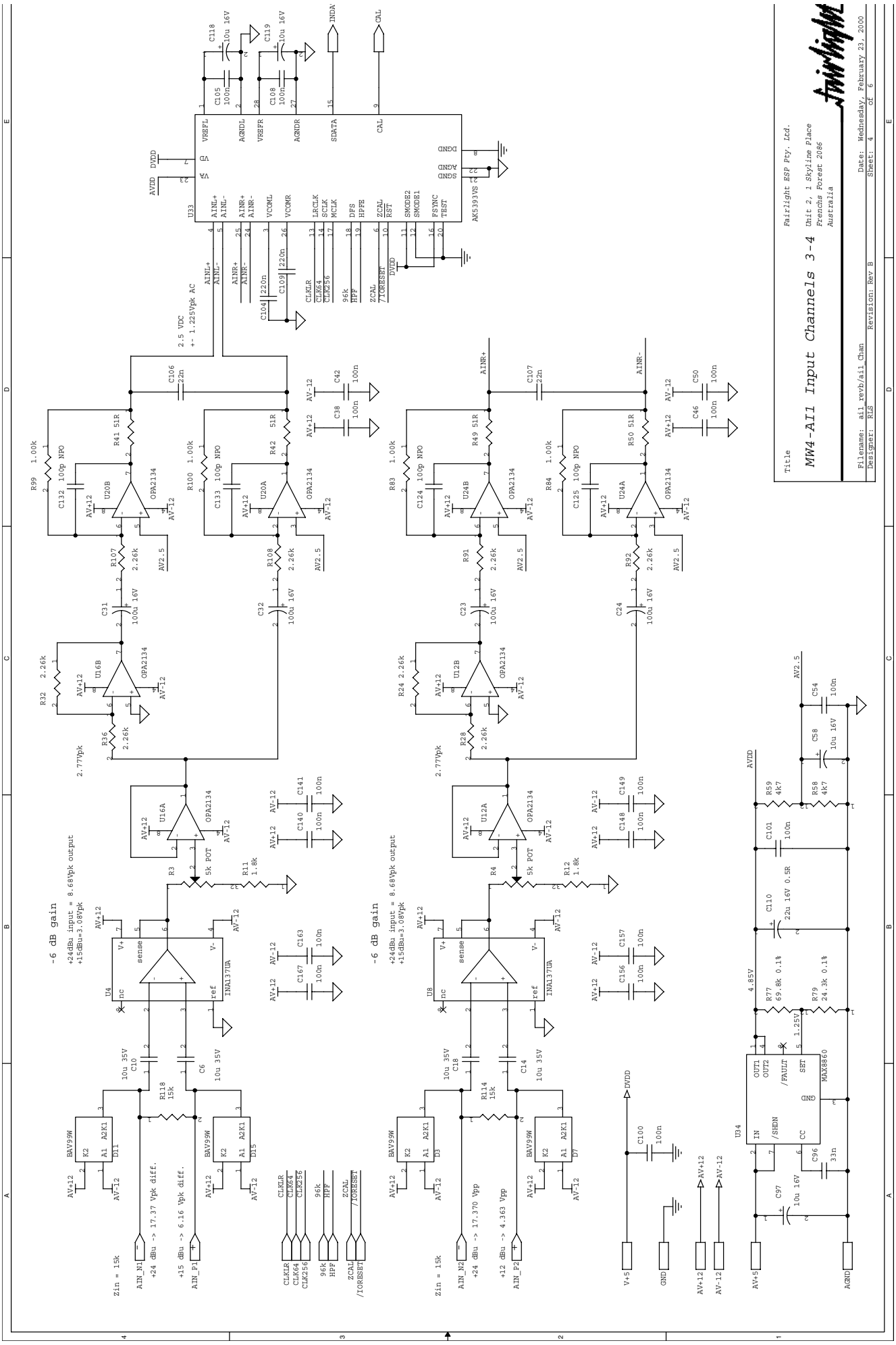
9. Open a DOS window on the PC and 'CD' to C:\Mw4\jtag-qdc

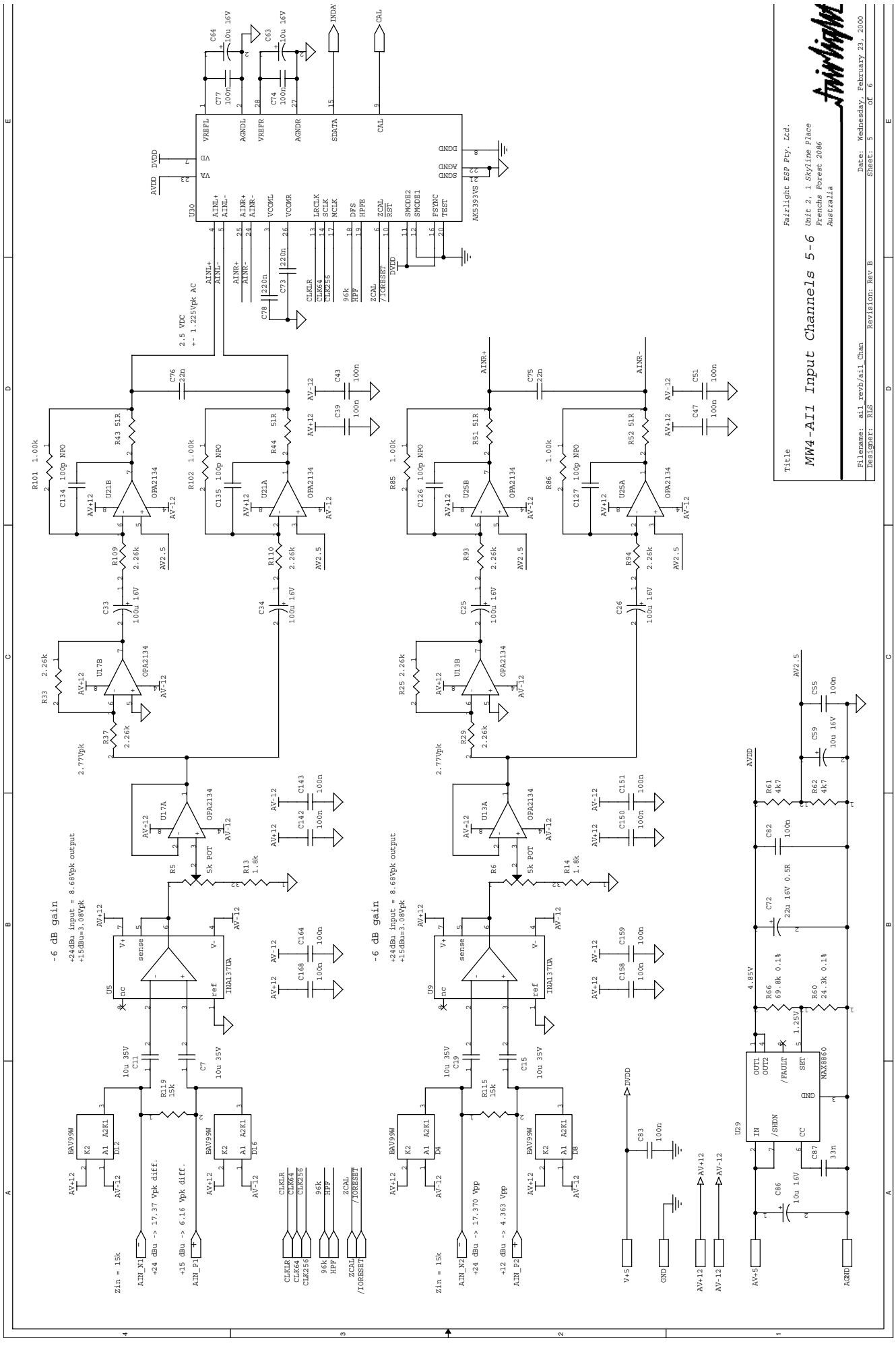
10. Run the command: jtag -v ai1prog
This will program the cpld on ai1.

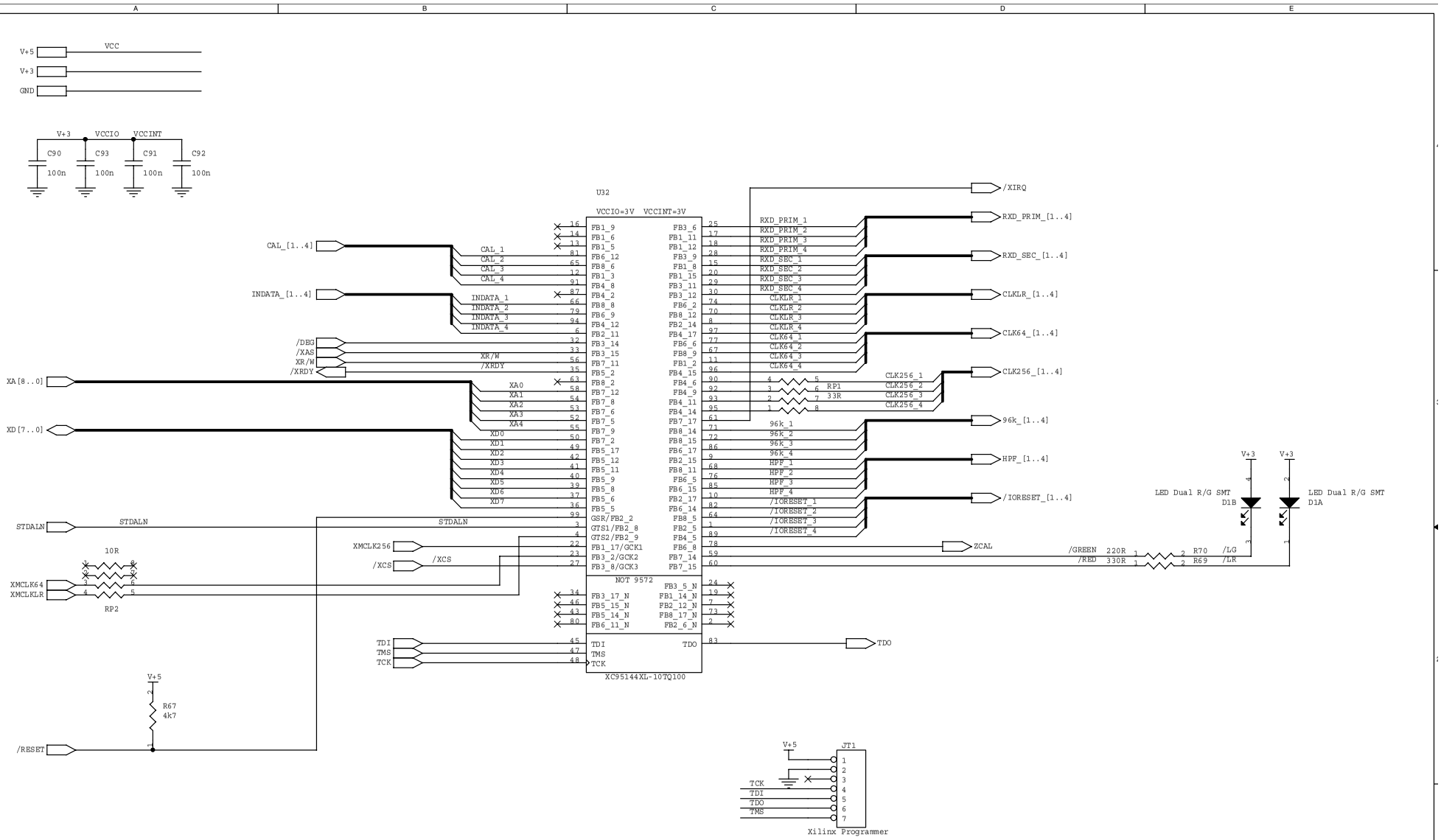
11. Turn off PSU and remove card under test.


External I/O Connector
CN1
HEADER 32X2
/AI1 Present
CHAN1-2
CHAN3-4
CHAN5-6
CHAN7-8
ai1_Chan
DSP I/O Connector
CN2
HEADER 32X2
Option for two BLM21A chokes
or one PLM250 CM choke
0R0 LINK
L3
OMIT
C79
15u 35V 0.3R
U1
LT1129CQ
R17
75k
R18
33k
R21 5k POT
R22 5k POT
R20
33k
R19
75k
ZD1
13V Zener
C1
10u 35V 1.5R
C2
15u 35V 0.3R
C3
15u 35V 0.3R
C4
10u 35V 1.5R
U2
LT1175CQ
CTRL
ai1_ctrl
PCB Ver
= 1
AI1 ID
= 6
U31
QS3J245
R68
4k7
R71
R72
R73
R74
J1
J2
J3
J4
SBJ
Title
MW4-AI1
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ai1_revb/ai1
Date: Tuesday, February 29, 2000
Designer: RLS
Revision: Rev B
Sheet: 1 of 6


Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Title
MW4-AI1 Input Channels 1-2
Filename: ai1 revb/ai1_Chan
Designer: RLS
Revision: Rev B
Date: Wednesday, February 23, 2000
Sheet: 3 of 6
-6 dB gain
+24dBu input = 8.689Vpk output
+15dBu=3.08Vpk
2.77Vpk
5k POT
INA137UA
OPA2134
AK5393VS
MAX8860
2.5 VDC
+- 1.225Vpk AC
Zin = 15k
+24 dBu -> 17.37 Vpk diff.
+15 dBu -> 6.16 Vpk diff.
+12 dBu -> 4.363 Vpp
+24 dBu -> 17.370 Vpp
AIN_N1
AIN_P1
AIN_N2
AIN_P2
BAV99W
CLKLR
CLK64
CLK256
96k
HPF
ZCAL
/IORESET
V+5
GND
AV+12
AV-12
AV2.5
AVDD
DVDD
AGND
DGND
SDATA
CAL
INDA


Title
MW4-AI1 Input Channels 3-4
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ai1 rev b/ai1_Chan
Designer: RJS
Revision: Rev B
Date: Wednesday, February 23, 2000
Sheet: 4 of 6
-6 dB gain
+24dBu input = 8.66Vpk output
+15dBu=3.08Vpk
2.77Vpk
2.5 VDC
+- 1.225Vpk AC
Zin = 15k
+24 dBu -> 17.37 Vpk diff.
+15 dBu -> 6.16 Vpk diff.
+12 dBu -> 4.363 Vpp
+24 dBu -> 17.370 Vpp
AIN_N1
AIN_P1
AIN_N2
AIN_P2
OPA2134
INA137UA
BAV99W
MAX8860
AK5393VS


Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Title
MW4-AI1 Input Channels 5-6
Filename: ai1 revb/ai1_Chan
Designer: RLS
Revision: Rev B
Date: Wednesday, February 23, 2000
Sheet: 5 of 6
-6 dB gain
+24dBu input = 8.689Vpk output
+15dBu=3.08Vpk
2.77Vpk
2.5 VDC
+- 1.225Vpk AC
AK5393VS
INRA
CAL
AIN_N1
AIN_P1
AIN_N2
AIN_P2
Zin = 15k
+24 dBu -> 17.37 Vpk diff.
+15 dBu -> 6.16 Vpk diff.
+24 dBu -> 17.370 Vpp
+12 dBu -> 4.363 Vpp
MAX8860
OPA2134
INA137UA
BAV99W
5k POT
AV+12
AV-12
AV2.5
AVDD
DVDD
V+5
AGND
DGND



Title	*Fairlight ESP Pty. Ltd.*
MW4-AI1 Control Logic	*Unit 2, 1 Skyline Place* *Frenchs Forest 2086* *Australia*
Filename: ai1_revb/ai1_ctrl	Date: Wednesday, February 23, 2000
Designer: RLS Revision: Rev B	Sheet: 2 of 6

DRAFT

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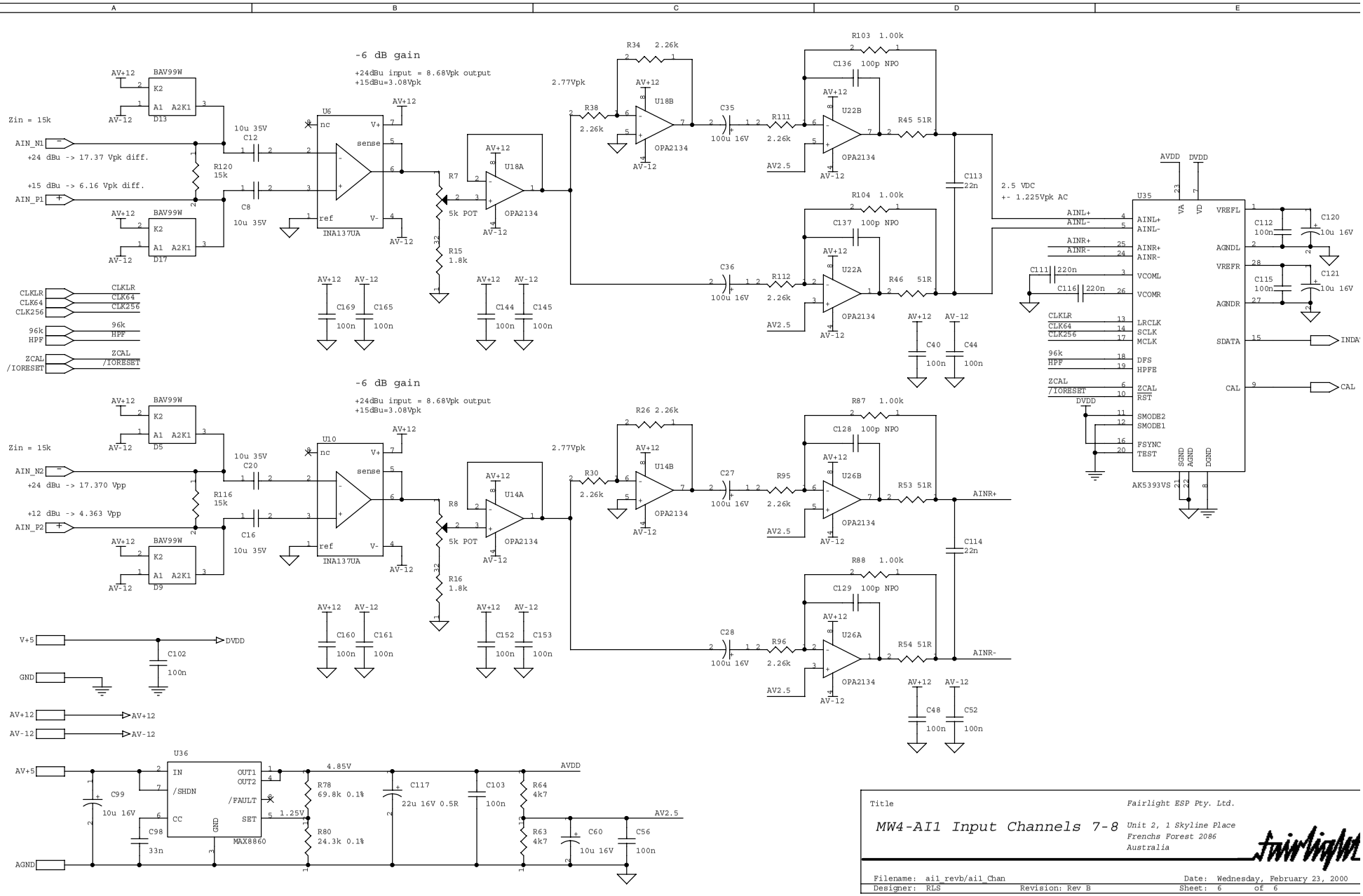
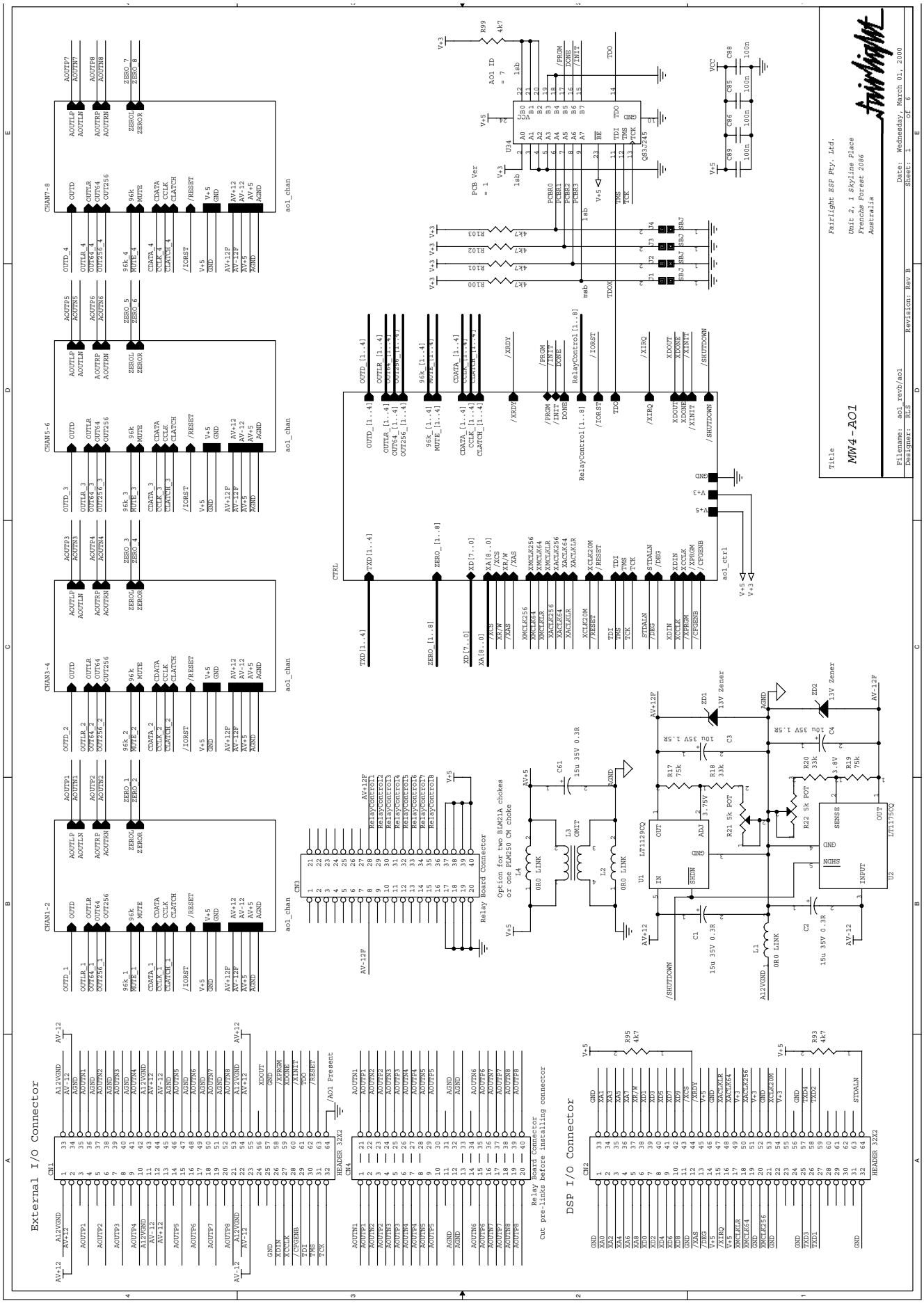


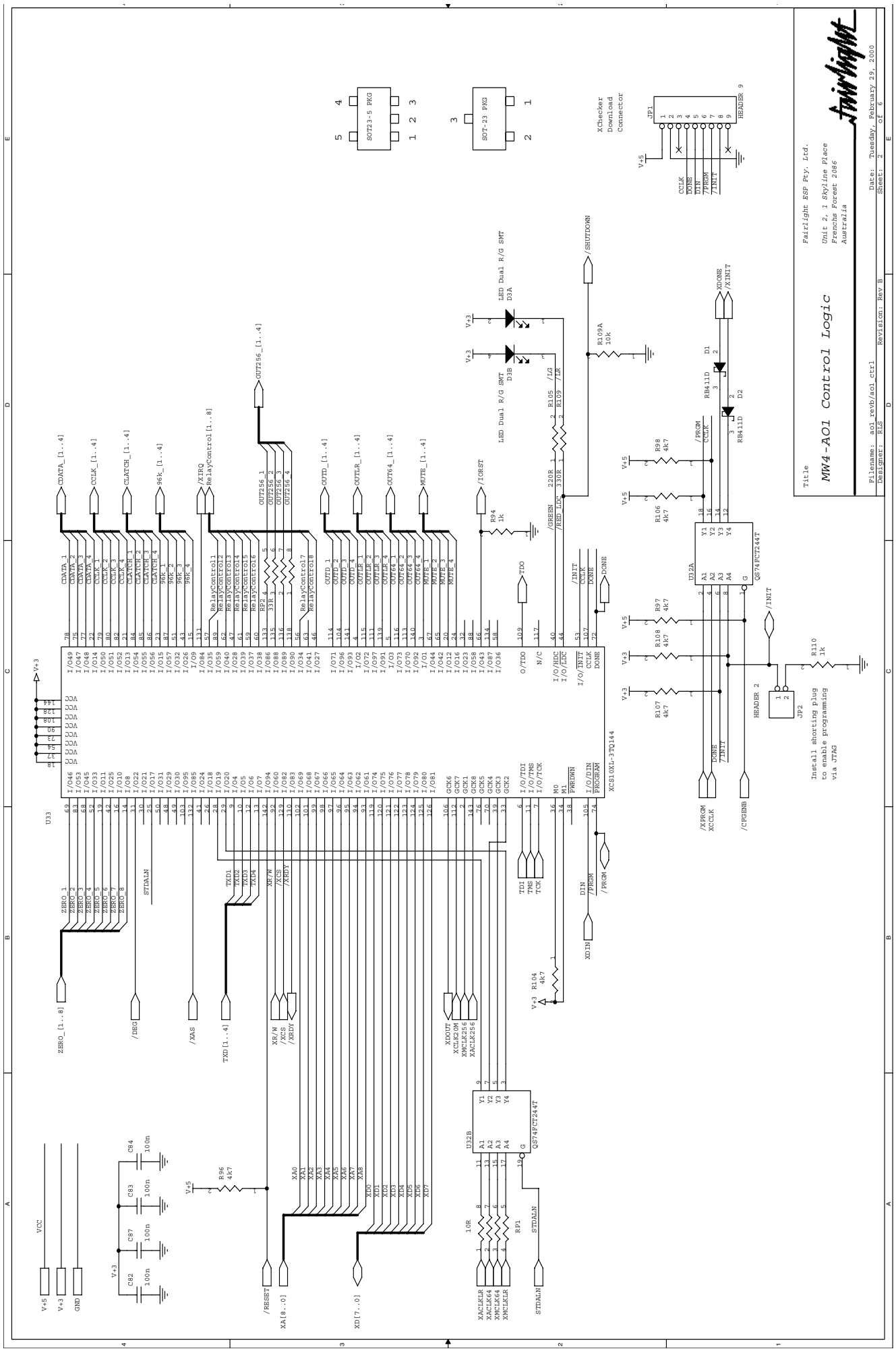
Title

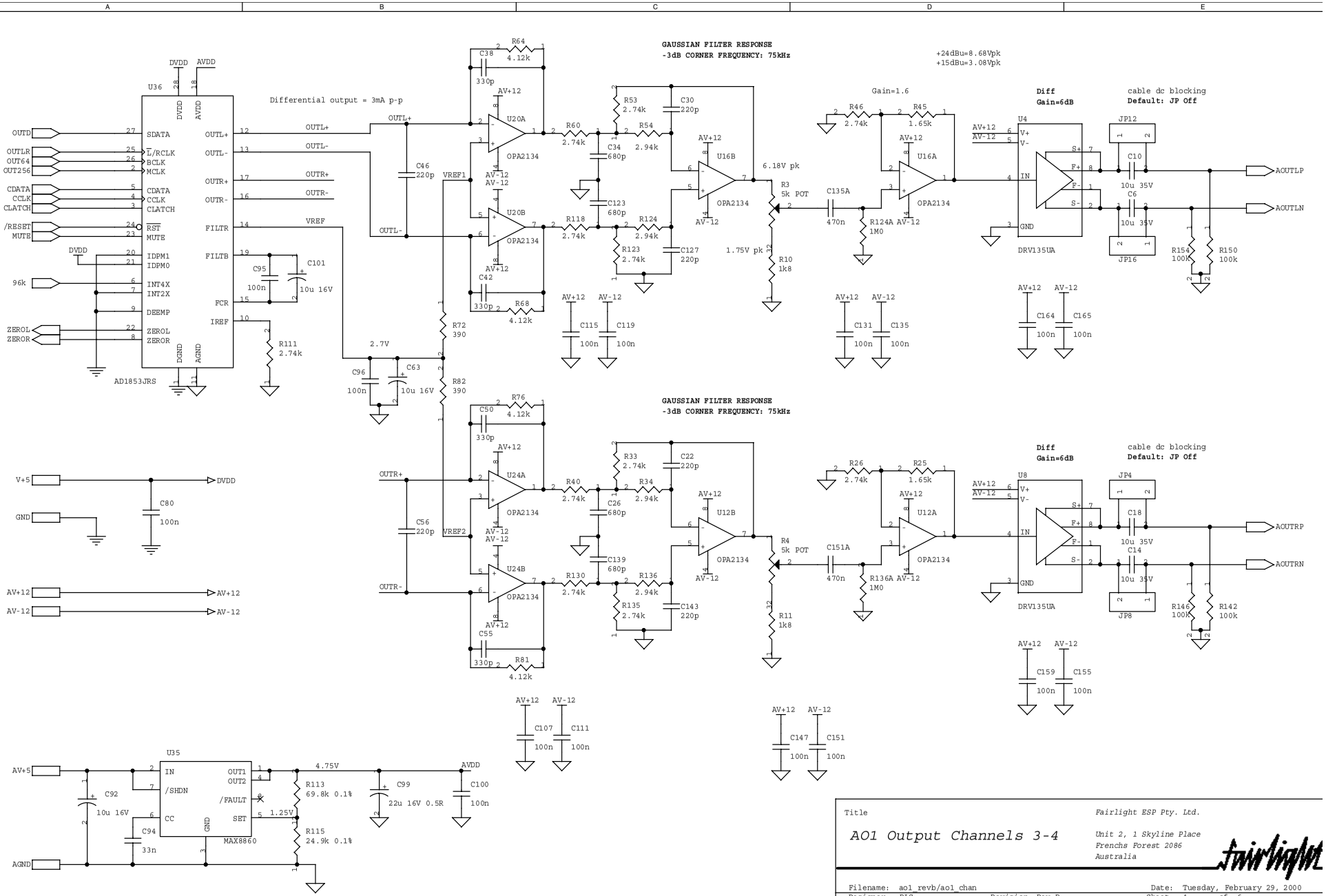
MW4-AI1 Input Channels 7-8

Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia

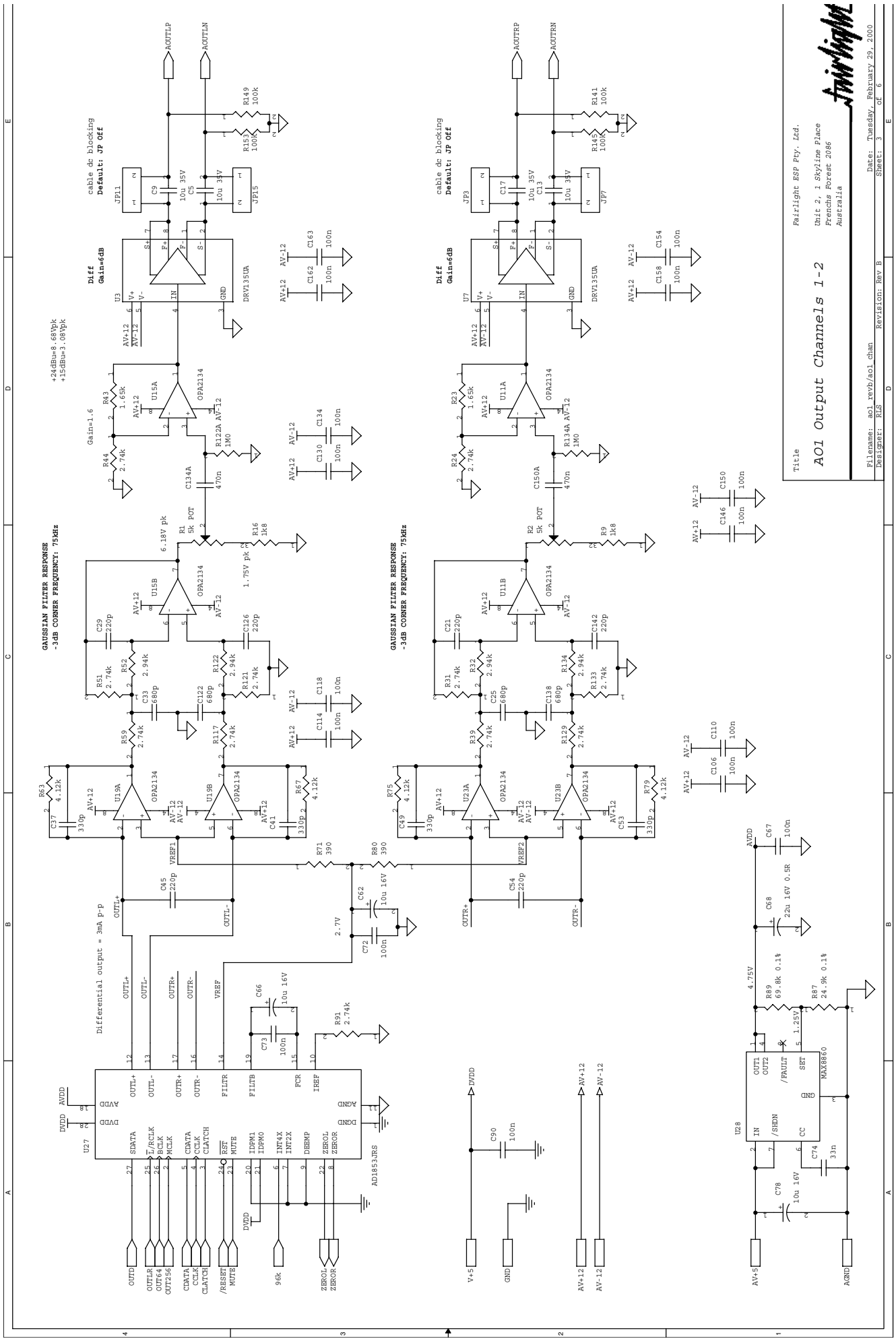
Filename: ai1_revb/ai1_Chan
Designer: RLS
Revision: Rev B
Date: Wednesday, February 23, 2000
Sheet: 6 of 6

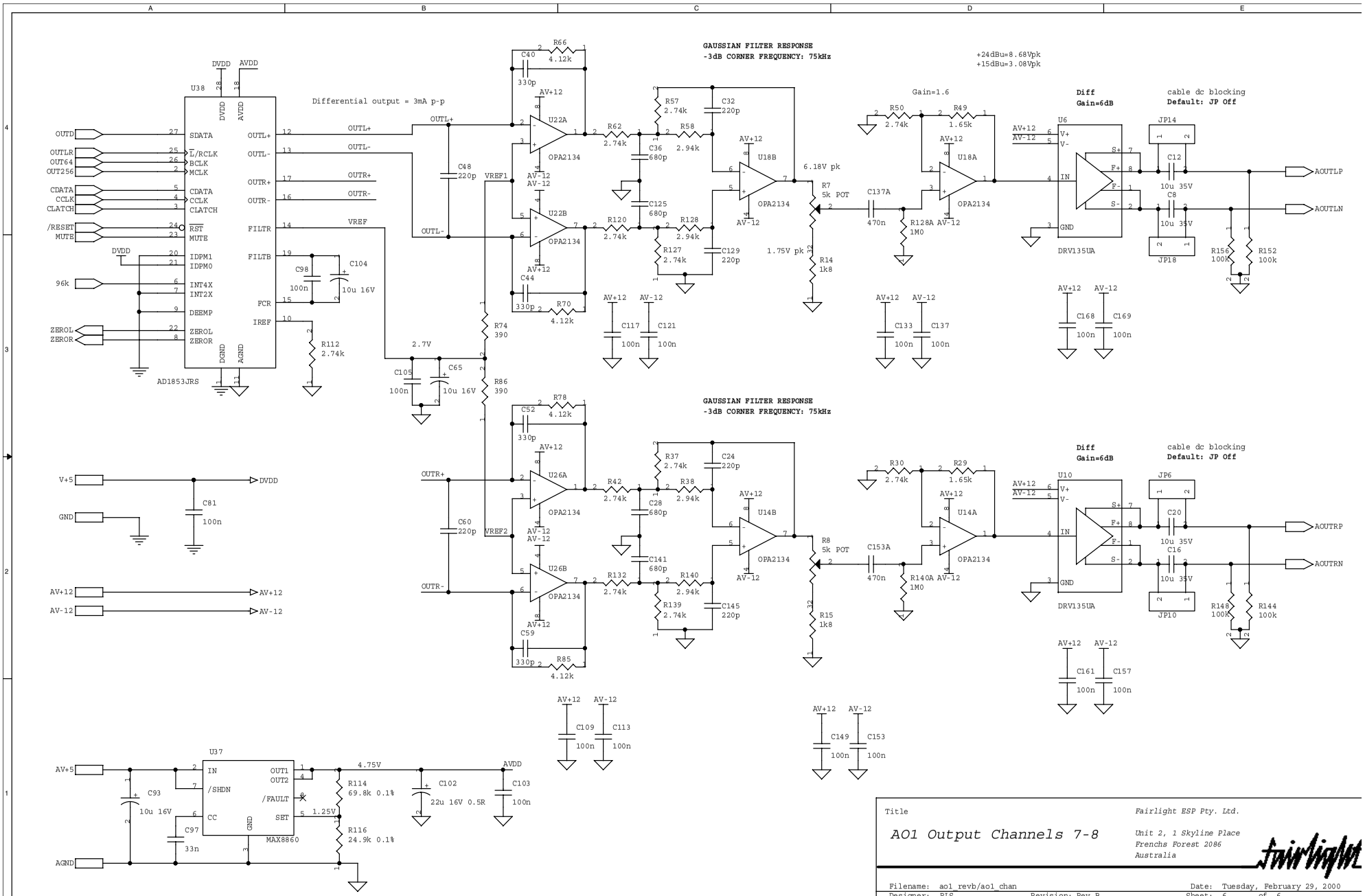

External I/O Connector
DSP I/O Connector
Relay Board Connector
Cut pre-links before installing connector
Option for two BLM21A chokes or one PLM250 CM choke
aol_ctrl
aol_chan
CHAN1-2
CHAN3-4
CHAN5-6
CHAN7-8
Title
MW4-AO1
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
French Forest 2086
Australia
Filename: aol_revb/aol
Revision: Rev B
Date: Wednesday, March 01, 2000
Designer: RLS
Sheet: 1 of 6

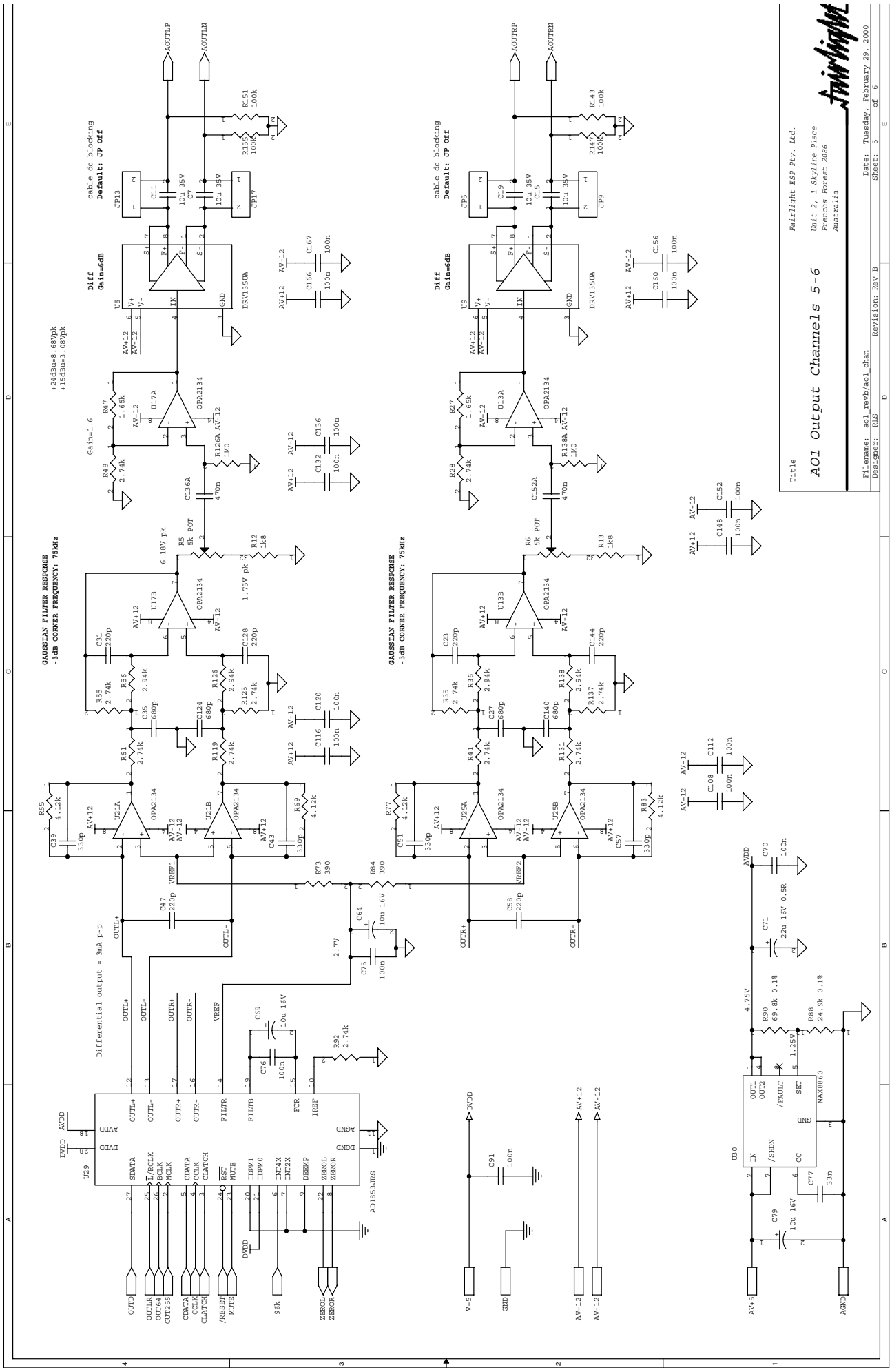

Title
MW4-AO1 Control Logic
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ao1_revb/ao1_ctrl
Revision: Rev B
Designer: RJS
Date: Tuesday, February 29, 2000
Sheet: 2 of 6
U33
XCS10XL-3TQ144
U32A
U32B
QS74FCT244T
SOT23-5 PKG
SOT-23 PKG
LED Dual R/G SMT
XChecker Download Connector
JP1
HEADER 9
JP2
HEADER 2
Install shorting plug to enable programming via JTAG
CDATA_[1..4]
CCLK_[1..4]
CLATCH_[1..4]
96k_[1..4]
/XIRQ
RelayControl[1..8]
OUT256_[1..4]
OUTD_[1..4]
OUTLR_[1..4]
OUT64_[1..4]
MUTE_[1..4]
/SHUTDOWN
/XDONE
/XINIT
/PRGM
/INIT
/RESET
XA[8..0]
XD[7..0]
ZERO_[1..8]
TXD[1..4]
/DBG
/XAS
XR/W
/XCS
/XRDY
XDOUT
XACLK24M
XACLK256
XACLK25.6
XACLKLR
XACLK64
XMCLK64
XMCLKLR
STDALN
TDI
TMS
TCK
M0
M1
PWRDWN
DIN
/PRGM
PROGRAM
CCLK
DONE
/INIT
/XFRGM
XCCLK
/CFGSNB
/1NIT
/1ORST
TDO
/GREEN
/RED_LDC
/LG
/LR
VCC
GND
V+5
V+3
R96 4k7
R94 1k
R104 4k7
R105 220R
R109 330R
R109A 10k
R106 4k7
R98 4k7
R97 4k7
R108 4k7
R107 4k7
R110 1k
RP1 10R
C82 100n
C83 100n
C84 100n
C87 100n
RB411D
D1
D2
D3A
D3B

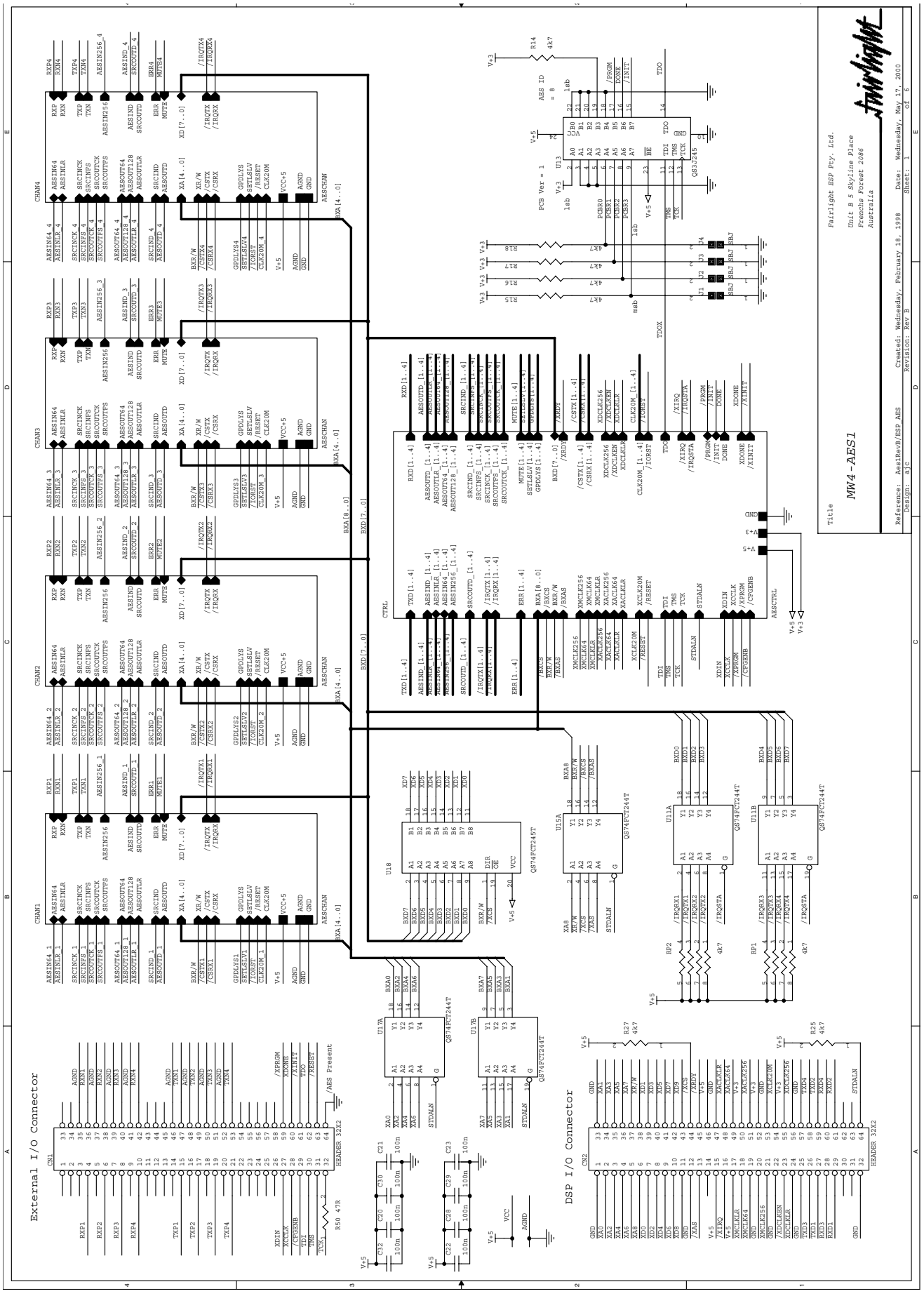

GAUSSIAN FILTER RESPONSE
-3dB CORNER FREQUENCY: 75kHz
+24dBu=8.68Vpk
+15dBu=3.08Vpk
Differential output = 3mA p-p
Gain=1.6
Diff
Gain=6dB
cable dc blocking
Default: JP Off
AD1853JRS
DRV135UA
MAX8860
OPA2134
6.18V pk
1.75V pk
2.7V
4.75V
AOUTLP
AOUTLN
AOUTRP
AOUTRN
Title
AO1 Output Channels 3-4
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ao1_revb/ao1_chan
Date: Tuesday, February 29, 2000
Designer: RLS
Revision: Rev B
Sheet: 4 of 6

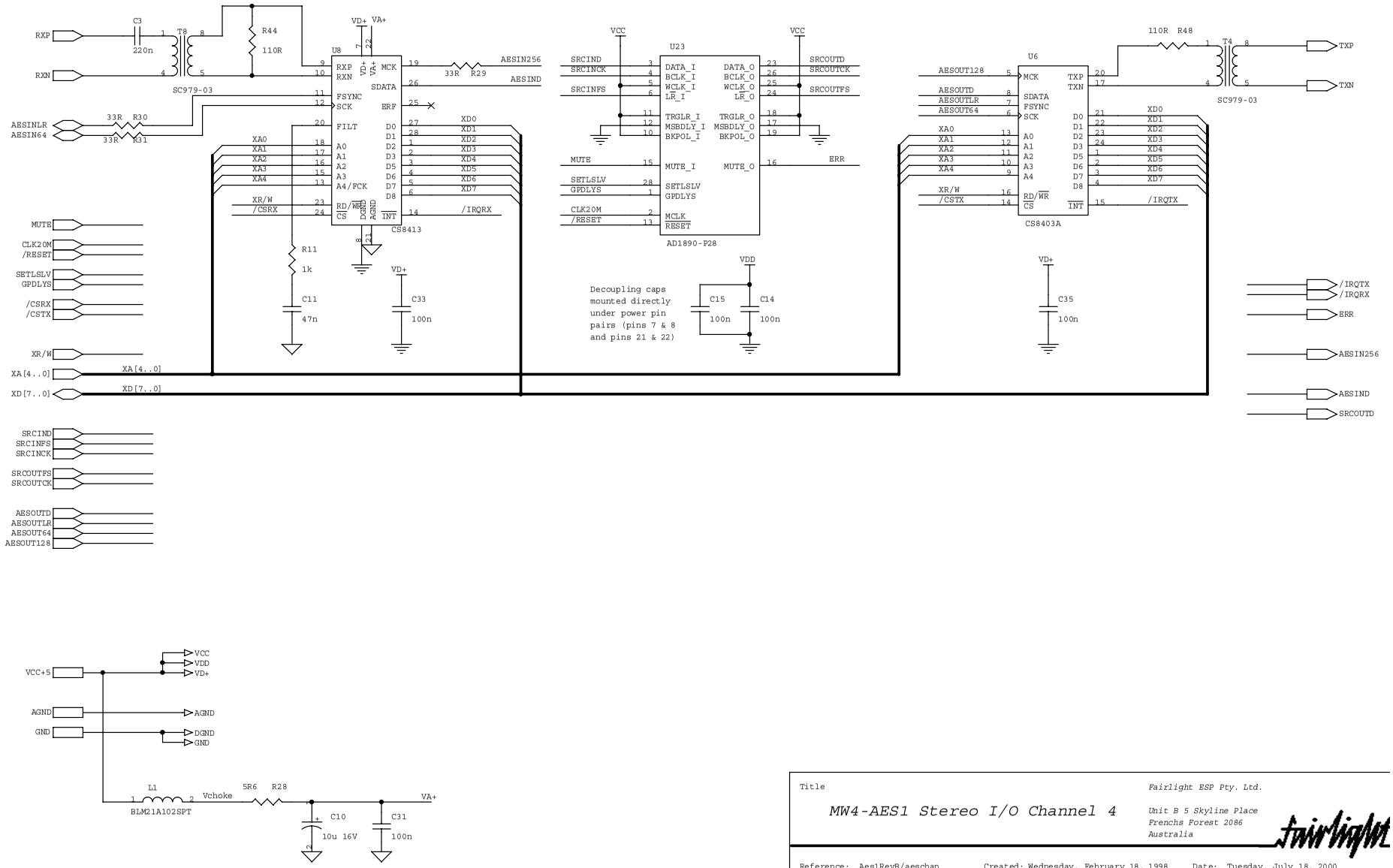
DRAFT


AO1 Output Channels 1-2
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ao1 revb/ao1 chan
Designer: RAS
Revision: Rev B
Date: Tuesday, February 29, 2000
Sheet: 3 of 6
AOUTLP
AOUTLN
AOUTRP
AOUTRN
cable dc blocking
Default: JP Off
Diff
Gain=6dB
DRV135UA
Gain=1.6
+24dBu=8.68Vpk
+15dBu=3.08Vpk
OPA2134
GAUSSIAN FILTER RESPONSE
-3dB CORNER FREQUENCY: 75kHz
6.18V pk
1.75V pk
Differential output = 3mA p-p
AD1853JRS
MAX8860
OUTD
OUTLR
OUT64
OUT256
CDATA
CCLK
CLATCH
/RESET
MUTE
96k
ZEROL
ZEROR
V+5
GND
AV+12
AV-12
AGND
AVDD
DVDD


GAUSSIAN FILTER RESPONSE
-3dB CORNER FREQUENCY: 75kHz
+24dBu=8.68Vpk
+15dBu=3.08Vpk
Differential output = 3mA p-p
Gain=1.6
Diff
Gain=6dB
cable dc blocking
Default: JP Off
AD1853JRS
DRV135UA
OPA2134
MAX8860
6.18V pk
1.75V pk
2.7V
4.75V
1.25V
AOUTLP
AOUTLN
AOUTRP
AOUTRN
Title
AO1 Output Channels 7-8
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
Frenchs Forest 2086
Australia
Filename: ao1_revb/ao1_chan
Date: Tuesday, February 29, 2000
Designer: RLS
Revision: Rev B
Sheet: 6 of 6


AO1 Output Channels 5-6
Fairlight ESP Pty. Ltd.
Unit 2, 1 Skyline Place
French's Forest 2086
Australia
Title
Filename: ao1_revb/ao1_chan
Revision: Rev B
Designer: RLS
Date: Tuesday, February 29, 2000
Sheet: 5 of 6
AOUTLP
AOUTLN
AOUTRP
AOUTRN
cable dc blocking
Default: JP Off
Diff
Gain=6dB
DRV135UA
Gain=1.6
+24dBu=8.68Vpk
+15dBu=3.08Vpk
GAUSSIAN FILTER RESPONSE
-3dB CORNER FREQUENCY: 75kHz
OPA2134
6.18V pk
1.75V pk
Differential output = 3mA p-p
AD1853JRS
MAX8860
4.75V
1.25V
AVDD
DVDD
AGND
DGND
V+5
GND
AV+12
AV-12
OUTD
OUTLR
OUT64
OUT256
CDATA
CCLK
CLATCH
/RESET
MUTE
96k
ZEROL
ZEROR


External I/O Connector
DSP I/O Connector
MW4-AES1
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French Forest 2086
Australia
Reference: Aes1Rev8/ESP_AES
Created: Wednesday, February 18, 1998
Date: Wednesday, May 17, 2000
Revision: Rev B
Sheet: 1 of 6
Design: a|c
CHAN1
CHAN2
CHAN3
CHAN4
CTRL
AESCTRL
PCB Ver = 1
AES ID = 8
HEADER 32X2
Q74FCT2244T
Q74FCT2245T
Q83J3245



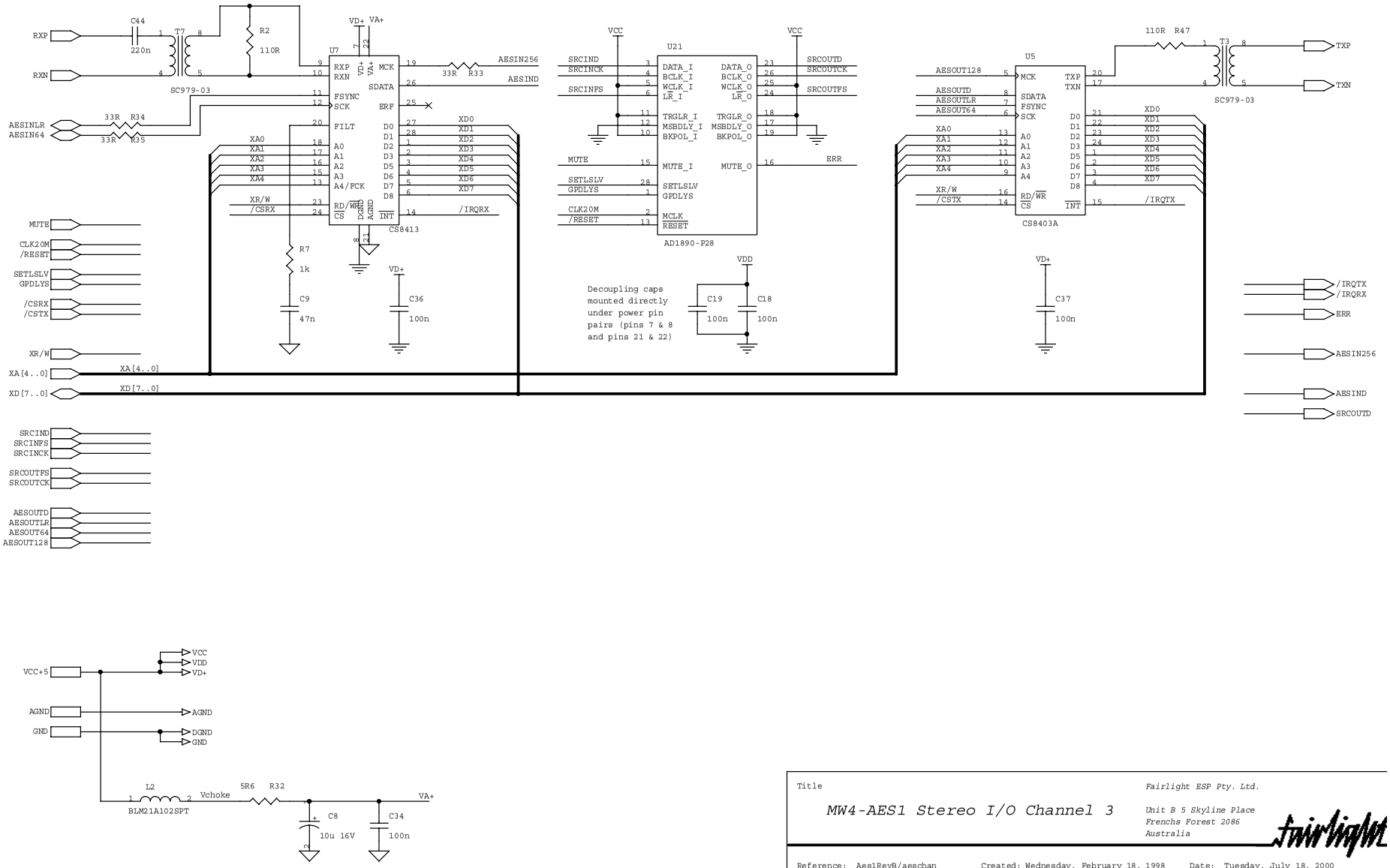
Title

MW4-AES1 Stereo I/O Channel 4

Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

Reference: Aes1RevB/aeschan
Created: Wednesday, February 18, 1998
Date: Tuesday, July 18, 2000
Design: ajc
Revision: Rev B
Sheet: 6 of 6



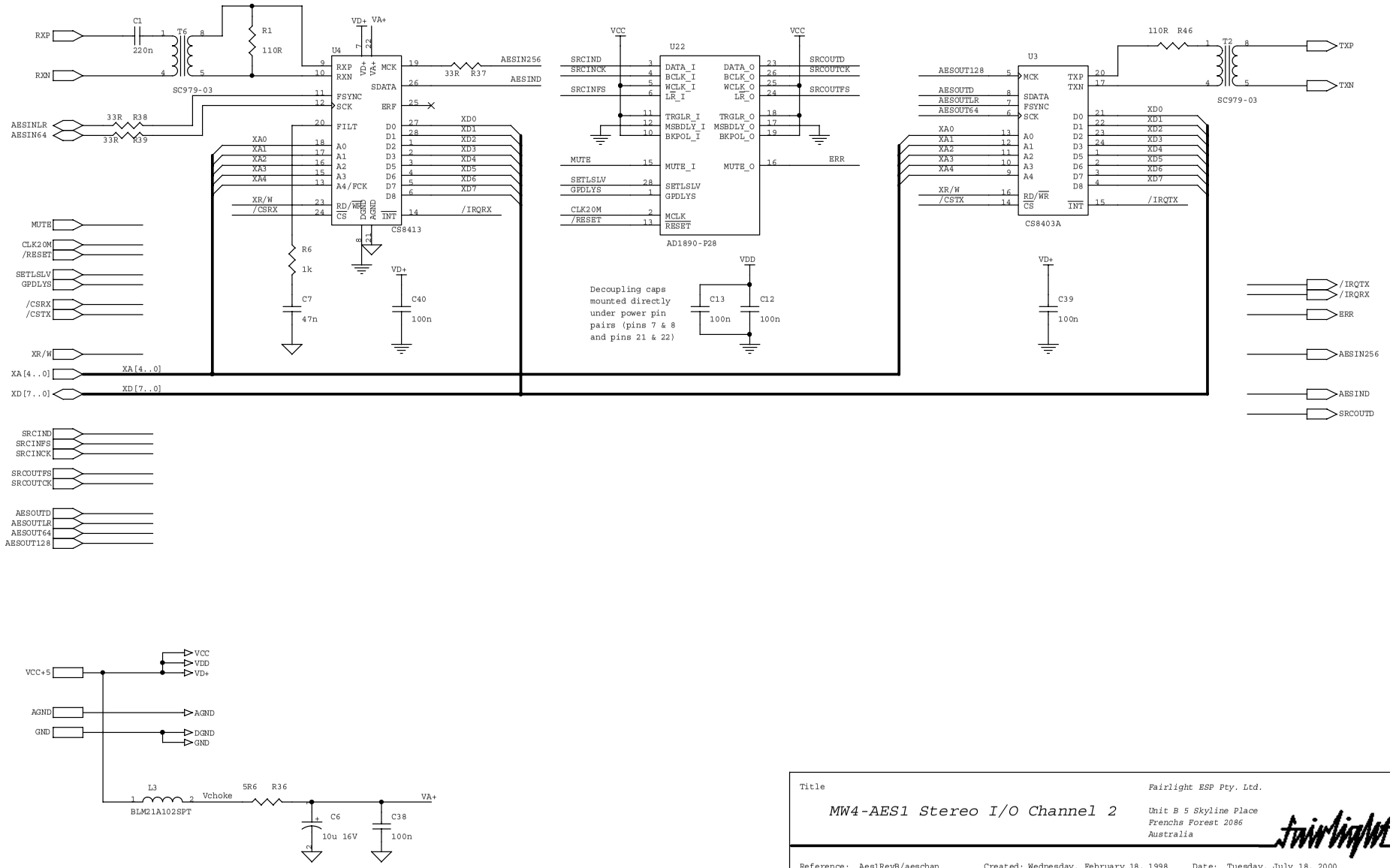
Title

MW4-AES1 Stereo I/O Channel 3

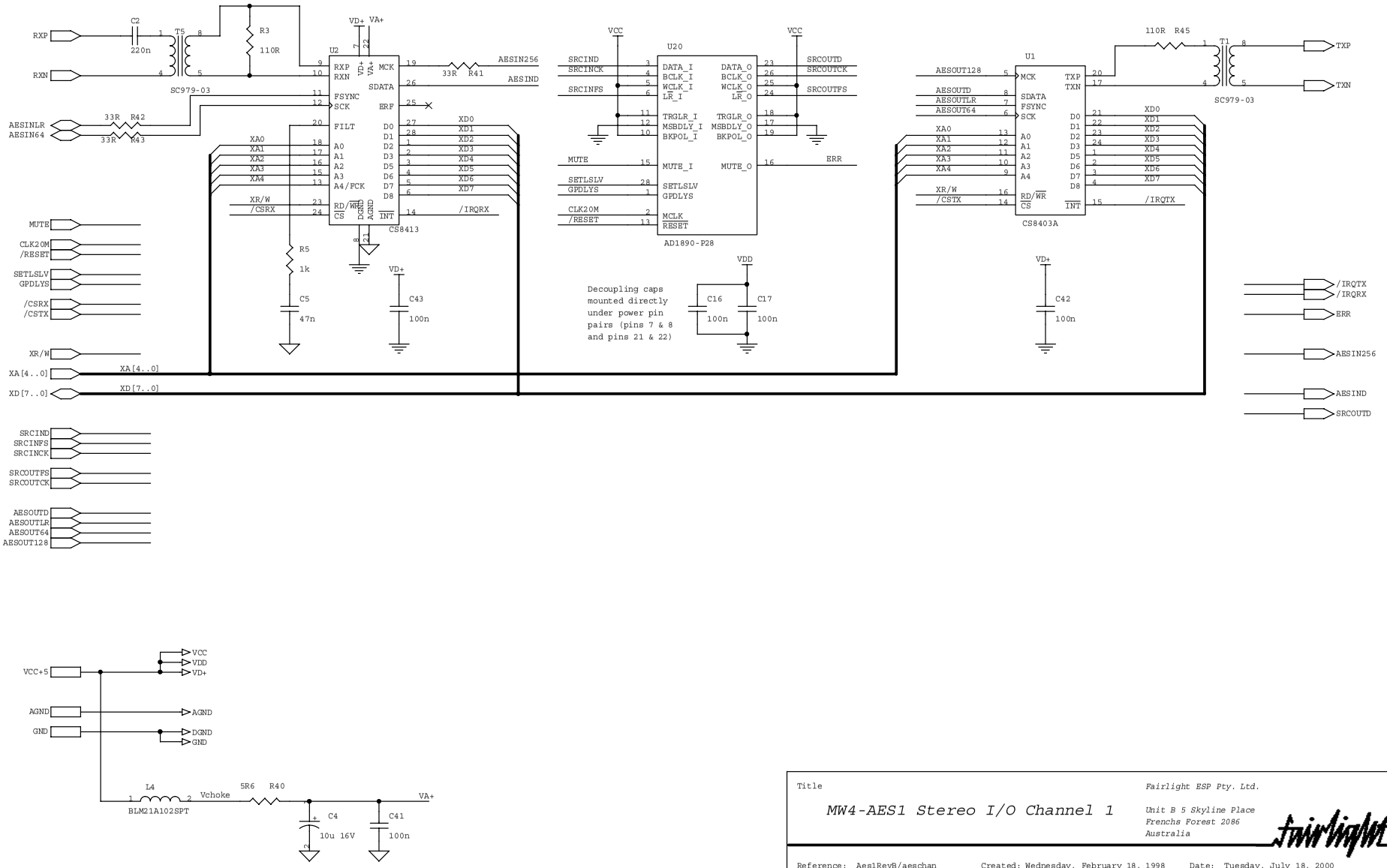
Fairlight ESP Pty. Ltd.

Unit B 5 Skyline Place
Frenchs Forest 2086
Australia

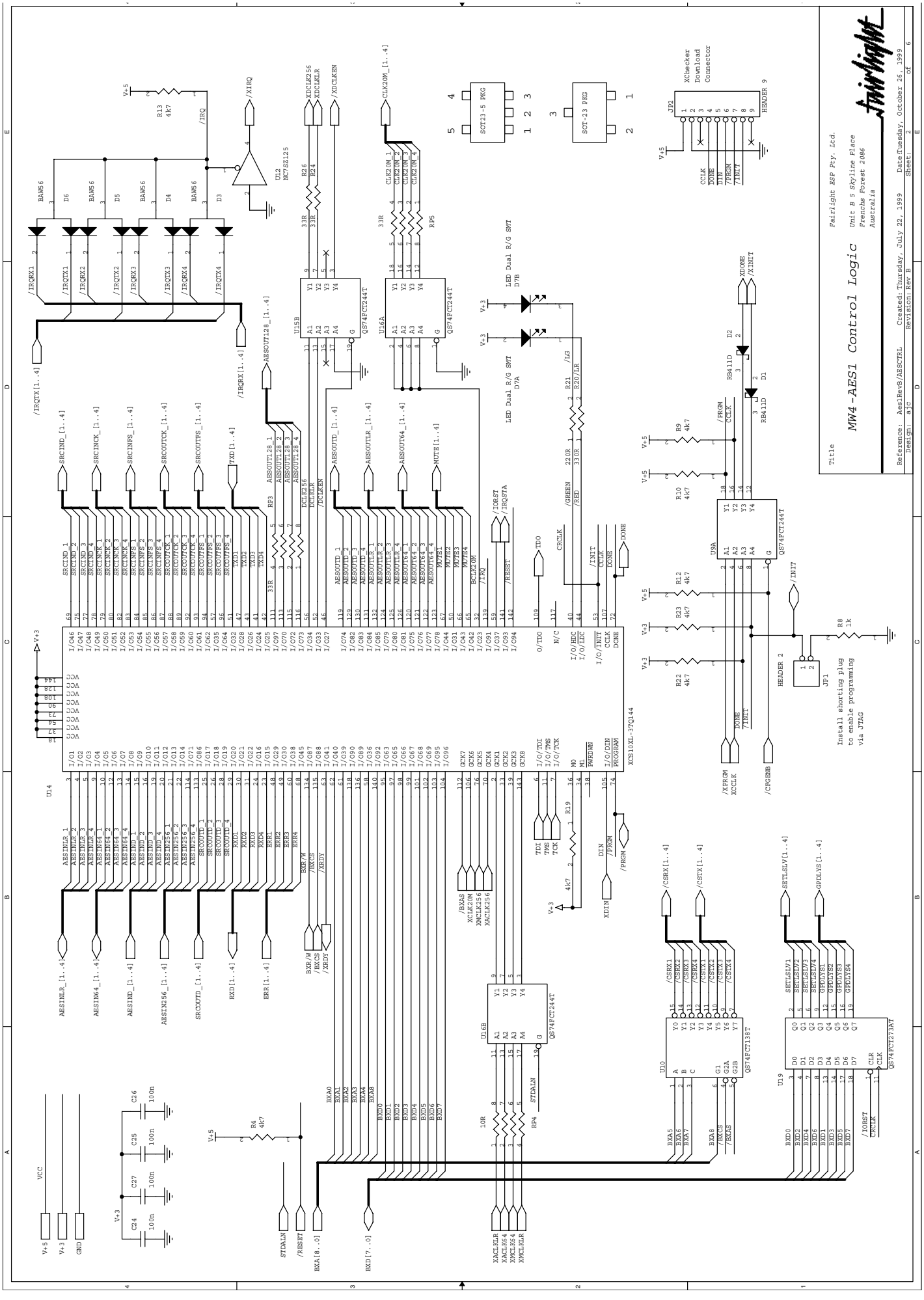
Reference: Aes1RevB/aeschan Created: Wednesday, February 18, 1998 Date: Tuesday, July 18, 2000
Design: ajc Revision: Rev B Sheet: 5 of 6



Title			*Fairlight ESP Pty. Ltd.*
MW4-AES1 Stereo I/O Channel 2			*Unit B 5 Skyline Place Prenchs Forest 2086 Australia*
Reference: Aes1RevB/aeschan	Created: Wednesday, February 18, 1998	Date: Tuesday, July 18, 2000	
Design: ajc	Revision: Rev B	Sheet: 4 of 6	



Title	*MW4-AES1 Stereo I/O Channel 1*
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference: Aes1RevB/aeschan	Created: Wednesday, February 18, 1998
Design: ajc	Revision: Rev B
Date: Tuesday, July 18, 2000	Sheet: 3 of 6


Title
MW4-AES1 Control Logic
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Aes1RevB/ABSCTRL
Created: Thursday, July 22, 1999
Date: Tuesday, October 26, 1999
Design: a3c
Revision: Rev B
Sheet: 2 of 6
XCS10XL-3TQ144
QS74FCT244T
QS74FCT138T
QS74FCT273AT
SOT23-5 PKG
SOT-23 PKG
LED Dual R/G SMT
XChecker Download Connector
HEADER 9
HEADER 2
Install shorting plug to enable programming via JTAG

9MW4PS1 - Power Supply

Introduction

The PS1revD is a metal box with one PCB assembly that delivers sufficient power for a fully loaded M4 chassis including 4 disks, 6 fully loaded QDCs and 2 QDCs with no analog mezzanines fitted.

M4 rails are 5.1v, 3.3v, +12.6v (disks), +-12.6v (audio).

The audio cards include low dropout (LDO) linear regulators that deliver +11.6v to the analog circuit rails, sufficient for +24 dBu differential input and output.

All analog converters are powered from the 5.1v rail again via LDO regulators that deliver 4.85v.

Features

The supply has an external on off switch near the power inlet.

In normal operation this switch remains on; power is turned on with a pushbutton at the front of the machine. Pressing the same button after the machine has started generates an interrupt that initiates a shutdown routine.

The supply can be synchronized to switch at a multiple of the audio clock, reducing the level of individual artifacts in the noise floor.

The supply delivers tightly regulated rails without adjustment and with low spectral noise. Consequently most of the losses usually associated with supplying clean analog rails have been eliminated. This reduces the number of rails, the operating temperature, and the amount of power required.

The supply includes control signals that lower the operating voltages to support production margin testing.

The supply includes a status signal that provides early warning of mains failure. This signal is used on QDC and the AO mezzanines to disconnect monitors before power transients can occur.

Supply does not include motion detect on the fan. It does includes thermal shutdown.

Cabling

Input is delivered via an IEC inlet and external power cable as usual.

DC power is delivered on two loom to the backplane and two looms to disks and fans.

A signal cable connects PS1 to the backplane and carries sync, voltage level control, and off signaling.

A mains potential cable connects the supply to the front panel switch to start the supply.

Input Specifications

Input voltage 85-270VAC
Frequency 49-63Hz
Power Factor0.99

Output Specifications

Output Voltage and Current:
#1: +5.1V @ 35A
#2: +3.4V @ 35A shared with #1
#3: +12V @ 9A
#4: *12V@7A
Minimum Load: 2.5A on #1, none on others.
Voltage Adjustment: None
Ripple and Noise: 50mV pk-pk on all outputs with user supplied final filter capacitors.
Regulation: *2% for all conditions including initial accuracy.
Over-voltage Protection: Supply trips off at 120% on all outputs.
Overload Protection: Supply trips off at 5% overcurrent for any output.
Paralleling: Outputs #1 & #2 can be paralleled with other supplies with the connection of a current share pin for each output.
Auto Recovery from Trip: None. Supply must be manually restarted.

Control features

Non-isolated remote "on" contacts, momentary operation, connected to mains potential.

Isolated remote "off", 1mA, 3V drop.

Isolated sync input for synchronizing switching frequency to external square wave
7mA, 3V drop, 174-196kHz 25-75% duty cycle for 87-98kHz switching frequency.

Power Fail TTL "0"

Operating Specifications

Efficiency: 75% typical
Switching frequency without sync signal: 92kHz.
Thermal Protection: Supply trips off on over temperature

ENVIRONMENTAL SPECIFICATIONS

Operating Temperature: 0 to 40*C

Cooling: Fan cooled

Standards and Approvals

Safety: UL1950, IEC950
EMI/RFI: to be decided

Connectors

The supply has two wire looms terminated in ATX plugs to carry 5v, 3.3v and +-12v to the backplane.

The supply has a 5-pin connector that carries sync (2), power off (1), status (1), and GND (1) to the backplane.

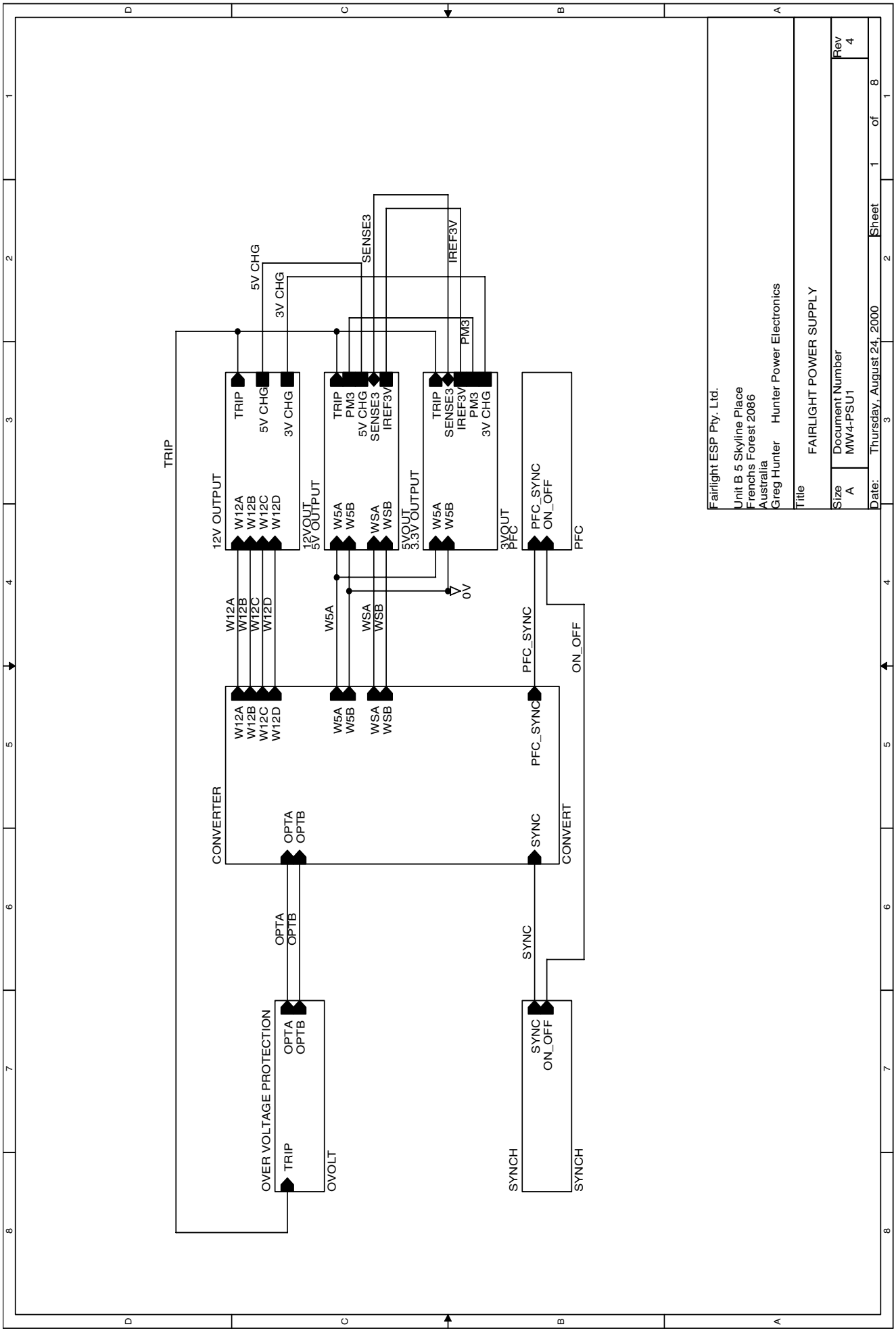
The supply has two disk power looms terminated in the usual 4 pin disk connector.

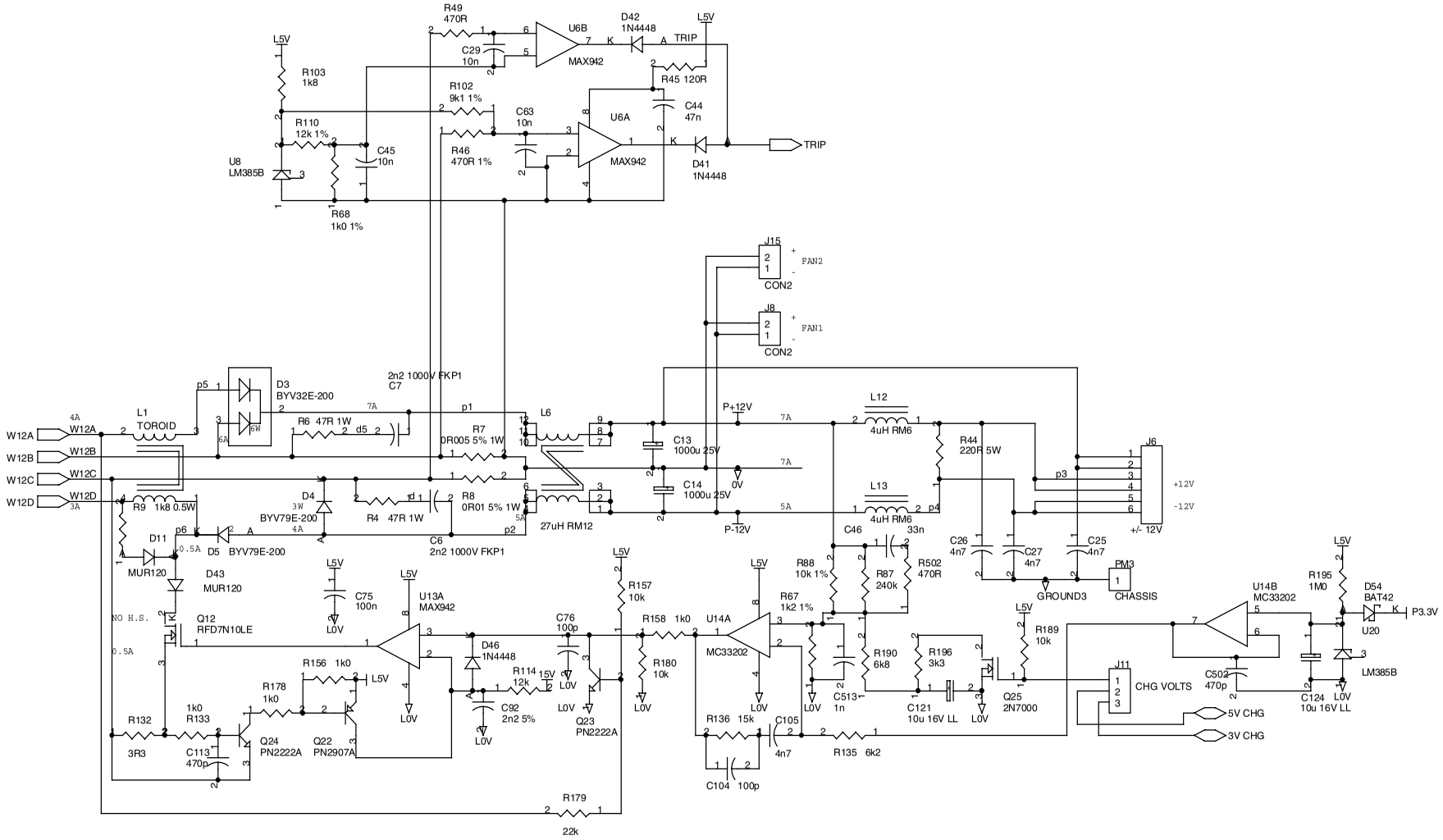
Backplane

The backplane has continuous GND, 5v and 3.3v planes. The +-12v planes are split between slots 5 and 6.

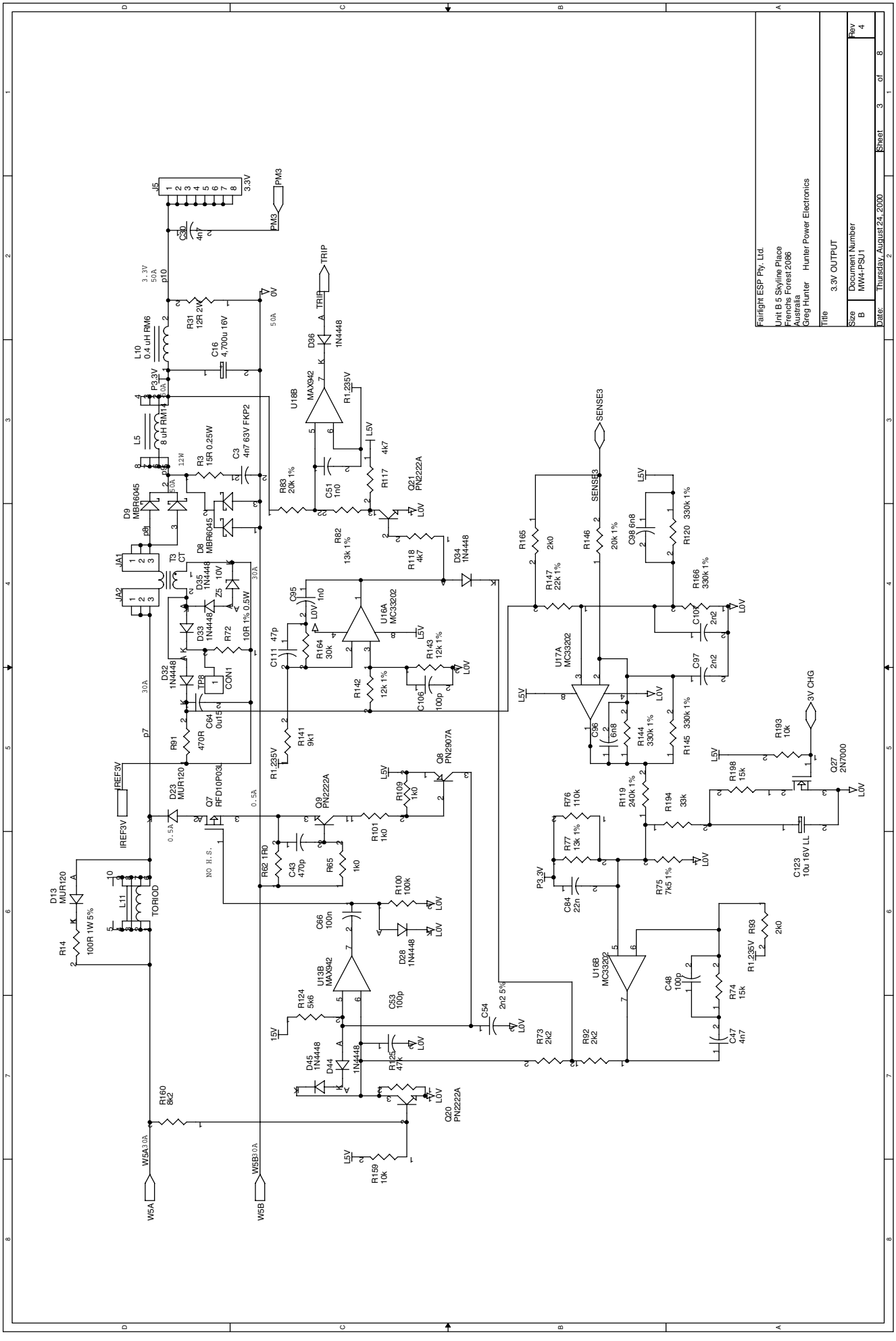
The backplane has four mating friction lock headers, two on each side of the +-12v split.

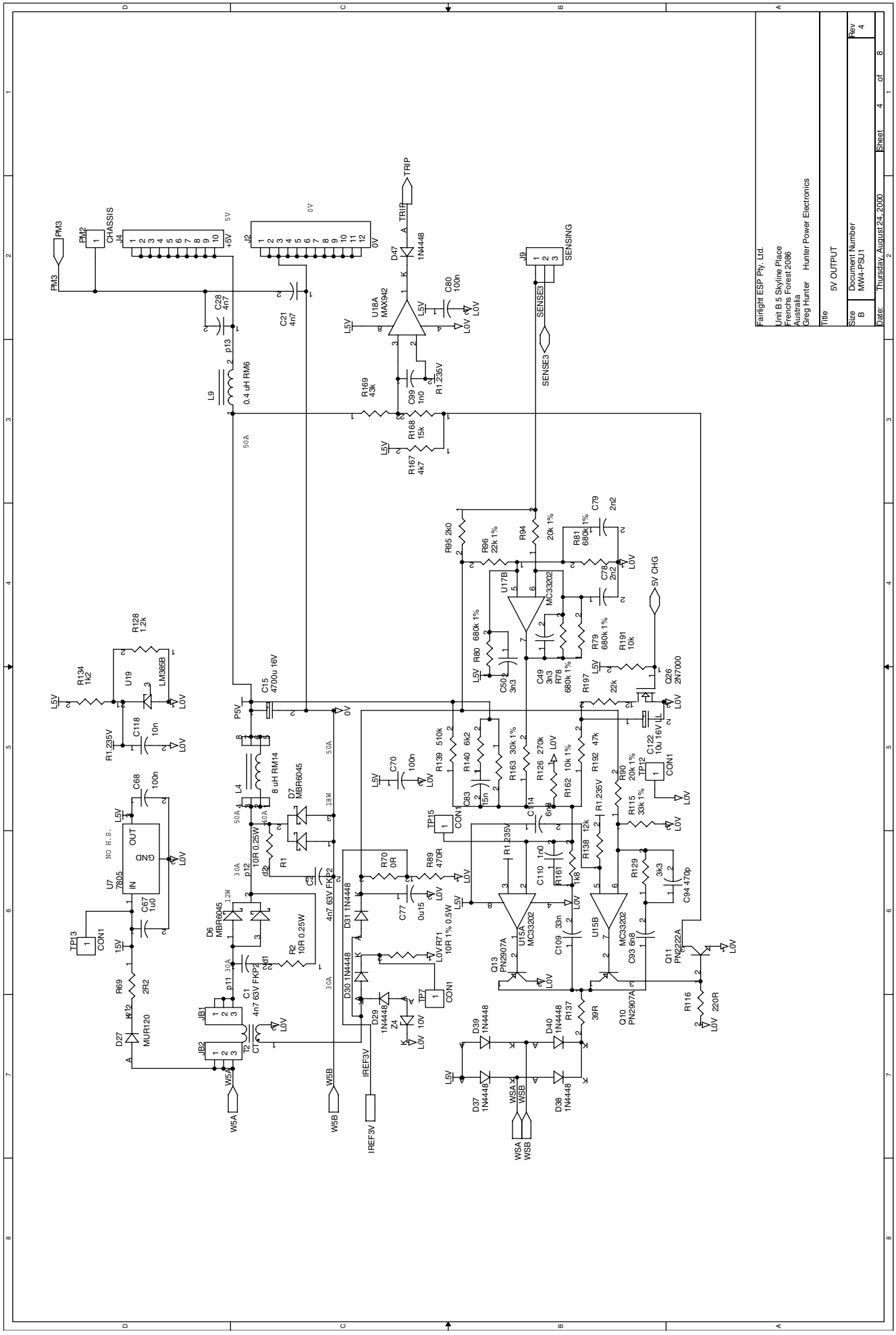
One of the two ATX plugs from PS1 should be plugged into each side of the split. Typically they are plugged into the far left hand and the far right hand positions.

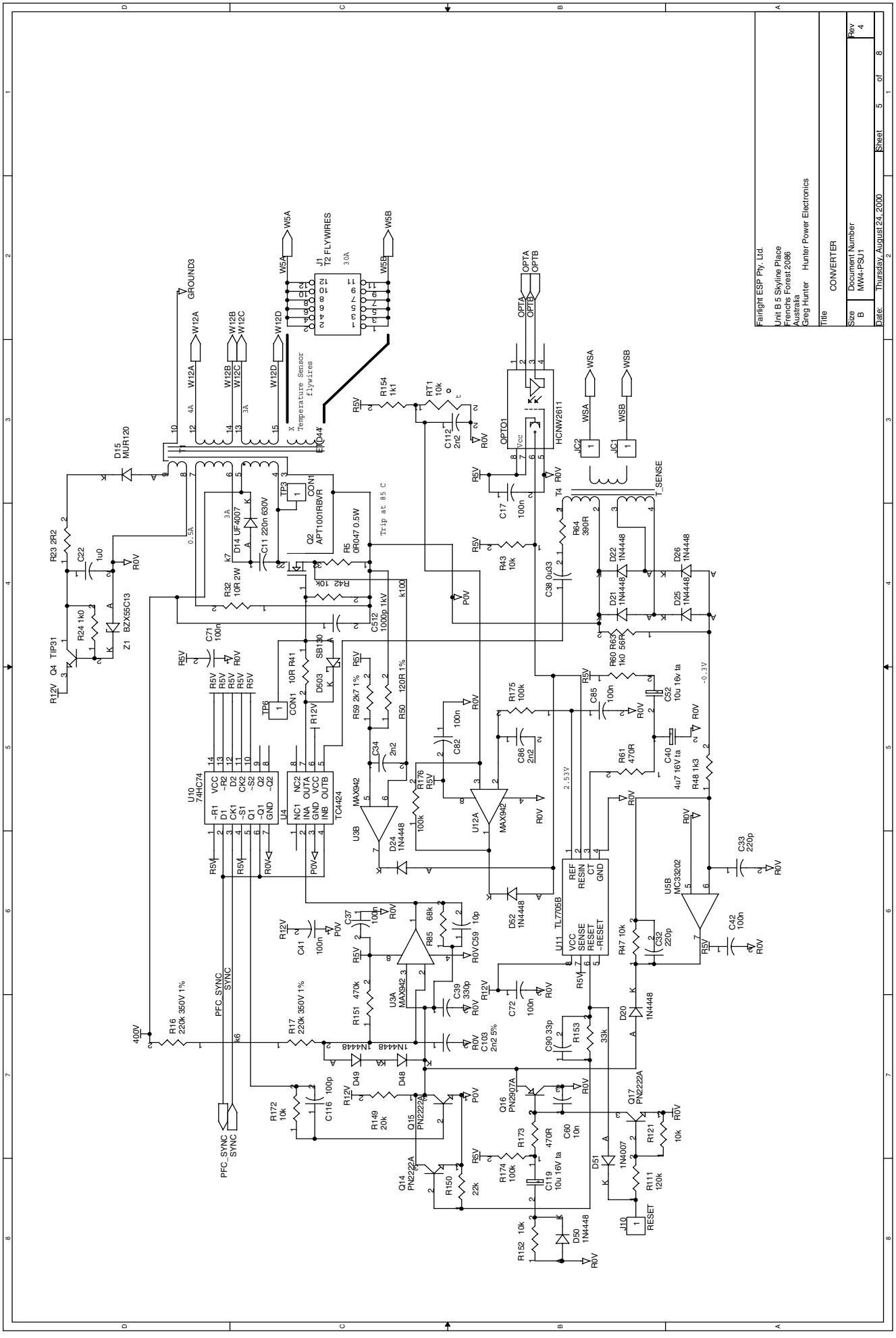

TRIP
5V CHG
3V CHG
SENSE3
IREF3V
PM3
12V OUTPUT
12VOUT
5V OUTPUT
5VOUT
3.3V OUTPUT
3VOUT
PFC
W12A
W12B
W12C
W12D
W5A
W5B
WSA
WSB
0V
PFC_SYNC
ON_OFF
CONVERTER
CONVERT
OPTA
OPTB
SYNC
OVER VOLTAGE PROTECTION
OVOLT
SYNCH
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
FAIRLIGHT POWER SUPPLY
Size A
Document Number MW4-PSU1
Rev 4
Date: Thursday, August 24, 2000
Sheet 1 of 8

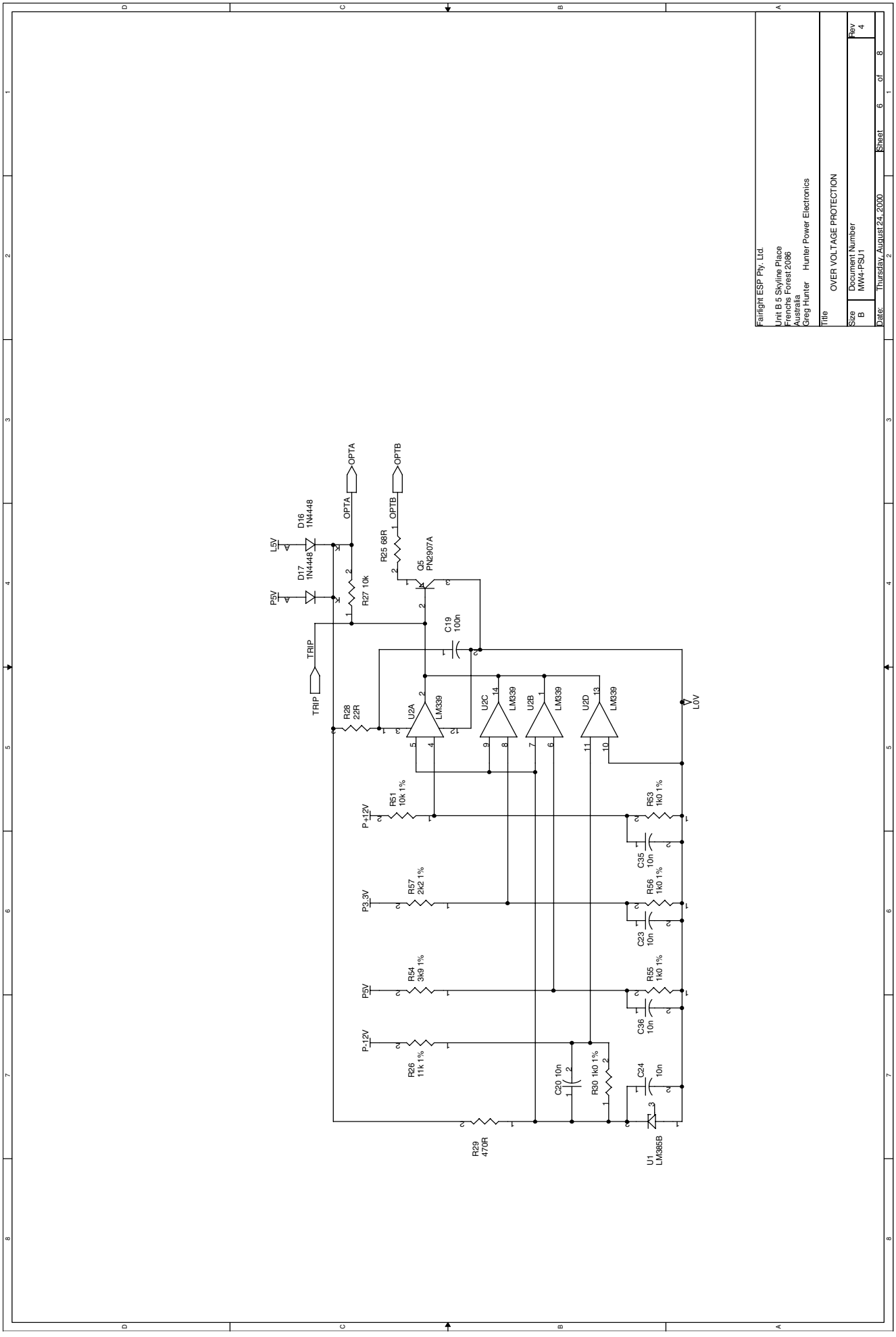


Fairlight ESP Pty. Ltd.		
Unit B 5 Skyline Place Frenchs Forest 2086 Australia Greg Hunter Hunter Power Electronics		
Title: 12V OUTPUT		
Size: B	Document Number: MW4-PSU1	Rev: 4
Date: Thursday, August 24, 2000	Sheet 2 of 8	


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
3.3V OUTPUT
Size B
Document Number MW4-PSU I
Rev 4
Date: Thursday, August 24, 2000
Sheet 3 of 8
J5
PM3
3.3V
C30 4n7
L10 0.4 uH RM6
R31 12R 2W
C16 4,700u 16V
L5 8 uH RM14
R3 15R 0.25W
C3 4n7 63V FKP2
D9 MBR6045
D8 MBR6045
T3 CT
JA1
JA2
D35 1N4448
Z5 10V
D33 1N4448
R72 10R 1% 0.5W
D32 1N4448
TP8
CON1
C64 0u15
R91 470R
D23 MUR120
Q7 RFD10P03L
IREF3V
NO H.S.
D13 MUR120
R14 100R 1W 5%
L11
TORIOD
R62 1R0
C43 47p
R65 1k0
Q9 PN2222A
R109 1k0
Q8 PN2907A
R101 1k0
R141 9k1
R1.235V
C111 47p
R164 30k
C95 L0V 1n0
U16A MC33202
R143 12k 1%
R142 12k 1%
C106 100p
U18B MAX942
D36 1N4448
TRIP
R83 20k 1%
C51 1n0
R117 4k7
Q21 PN2222A
R82 13k 1%
R118 4k7
D34 1N4448
R100 100k
C66 100n
D28 1N4448
U13B MAX942
R124 5k6
C53 100p
C54 2n2 5%
R73 2k2
R92 2k2
D45 1N4448
D44 1N4448
R125 47k
Q20 PN2222A
R160 8k2
R159 10k
W5A
W5B
SENSE3
R165 2k0
R147 22k 1%
R146 20k 1%
C98 6n8
R120 330k 1%
R166 330k 1%
C102 2n2
C97 2n2
U17A MC33202
C96 6n8
R144 330k 1%
R145 330k 1%
R193 10k
3V CHG
Q27 2N7000
R198 15k
R119 240k 1%
R194 33k
R76 110k
R77 13k 1%
R75 7k5 1%
C84 22n
C123 10u 16V LL
U16B MC33202
R1.235V R93 2k0
C48 100p
R74 15k
C47 4n7


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
5V OUTPUT
Size B
Document Number MW4-PSU1
Rev 4
Date: Thursday, August 24, 2000
Sheet 4 of 8
PM3
PM2
CHASSIS
J4
J2
+5V
0V
TRIP
A_TRIP
D47 1N4448
U18A MAX942
C80 100n
C28 4n7
C21 4n7
L9 0.4 uH RM6
R169 43k
C99 1n0
R1 1.235V
R168 15k
R167 4k7
J9
SENSING
SENSE3
SENSE4
R95 2k0
R96 22k 1%
R94 20k 1%
R81 680k 1%
C79 2n2
C78 2n2
U17B MC33202
R80 680k 1%
C50 3n3
C49 3n3
R78 680k 1%
R79 680k 1%
R191 10k
5V CHG
Q26 2N7000
R197 22k
R128 1.2k
R134 1k2
U19 LM385B
C118 10n
C15 4700u 16V
L4 8 uH RM14
D7 MBR6045
C68 100n
U7 7805
NO H.S.
C67 1u0
TP13 CON1
R69 2R2
D27 MUR120
D6 MBR6045
R2 10R 0.25W
R1 10R 0.25W
C1 4n7 63V FKP2
C2 4n7 63V FKP2
JB1
JB2
T2
W5A
W5B
IREF3V
D31 1N4448
D30 1N4448
D29 1N4448
Z4
R70 0R
R89 470R
C77 0u15
R71 10R 1% 0.5W
C70 100n
R139 510k
R140 6k2
R163 30k 1%
R126 270k
R162 10k 1%
R192 47k
C122 10u 16V
TP15
TP12
R90 20k 1%
R115 33k 1%
C83 15n
C14 6n8
R138 12k
R161 1k8
C110 1n0
C109 33n
C93 6n8
R129 3k3
C94 470p
U15A MC33202
U15B MC33202
Q13 PN2907A
Q10 PN2907A
Q11 PN8222A
R116 220R
D39 1N4448
D40 1N4448
R137 39R
D37 1N4448
D38 1N4448


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
CONVERTER
Size B
Document Number MW4-PSU I
Rev 4
Date: Thursday, August 24, 2000
Sheet 5 of 8
T1
T2 FLYWIRES
Temperature Sensor flywires
HCNW2611
TL7705B
MAX942
TC4424
74HC74
MC33202
MUR120
UF4007
APT1001RBVR
BZX55C13
TIP31
SB130
PN2222A
PN2907A
1N4448
1N4007
GROUND3
W12A
W12B
W12C
W12D
W5A
W5B
W5SA
W5SB
OPTA
OPTB
T_SENSE
PFC_SYNC
SYNC
RESET
Trip at 85 C
400V
R12V
R5V
P0V
R0V


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
OVER VOLTAGE PROTECTION
Size B
Document Number MW4-PSU1
Rev 4
Date: Thursday, August 24, 2000
Sheet 6 of 8
OPTA
OPTB
D16 1N4448
D17 1N4448
L5V
P5V
R27 10k
R25 68R
Q5 PN2907A
C19 100n
TRIP
R28 22R
U2A LM339
U2C LM339
U2B LM339
U2D LM339
L0V
P-12V
R51 10k 1%
R53 1k0 1%
C35 10n
P3.3V
R57 2k2 1%
R56 1k0 1%
C23 10n
P5V
R54 3k9 1%
R55 1k0 1%
C36 10n
P-12V
R26 11k 1%
C20 10n
R30 1k0 1%
C24 10n
R29 470R
U1 LM385B

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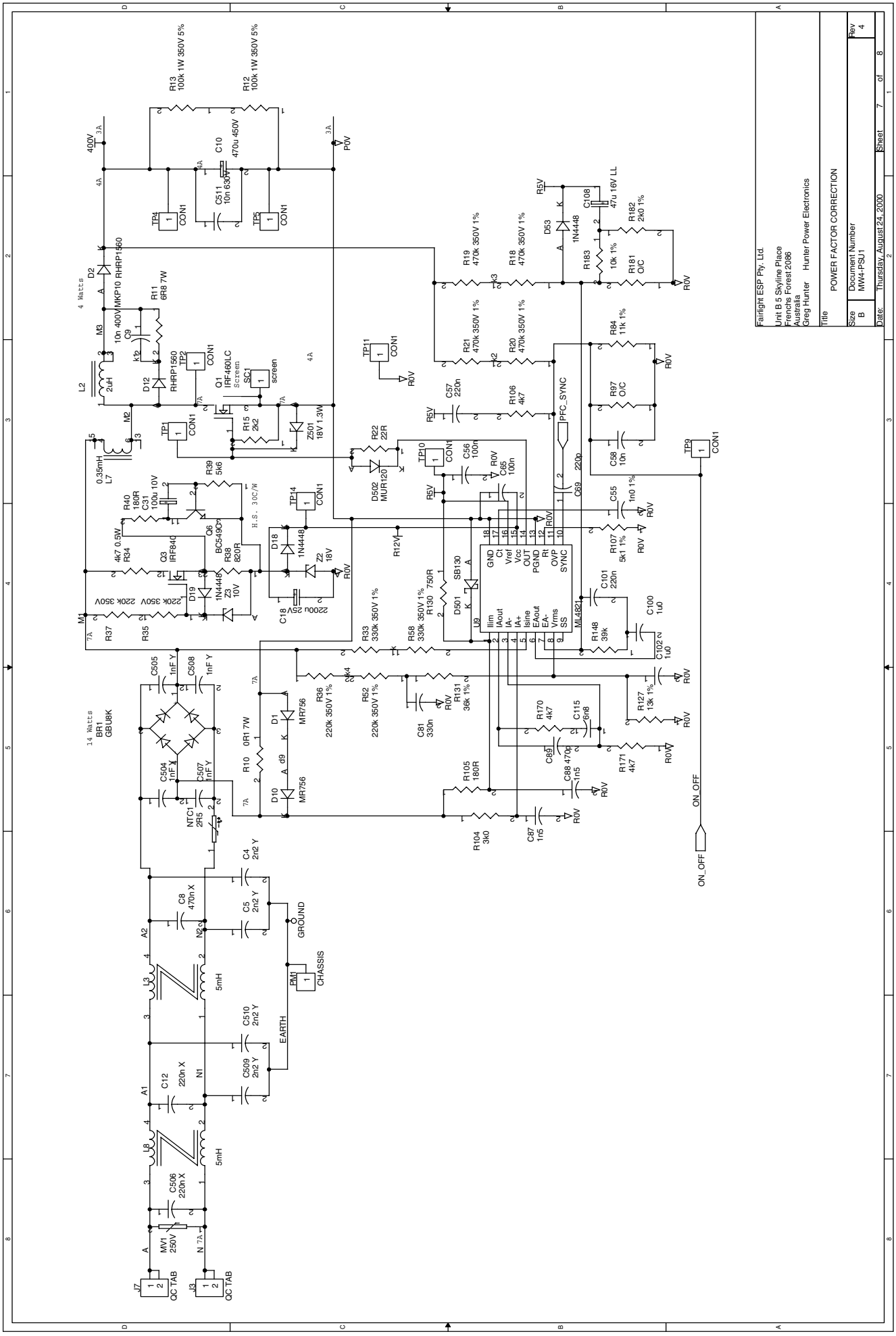
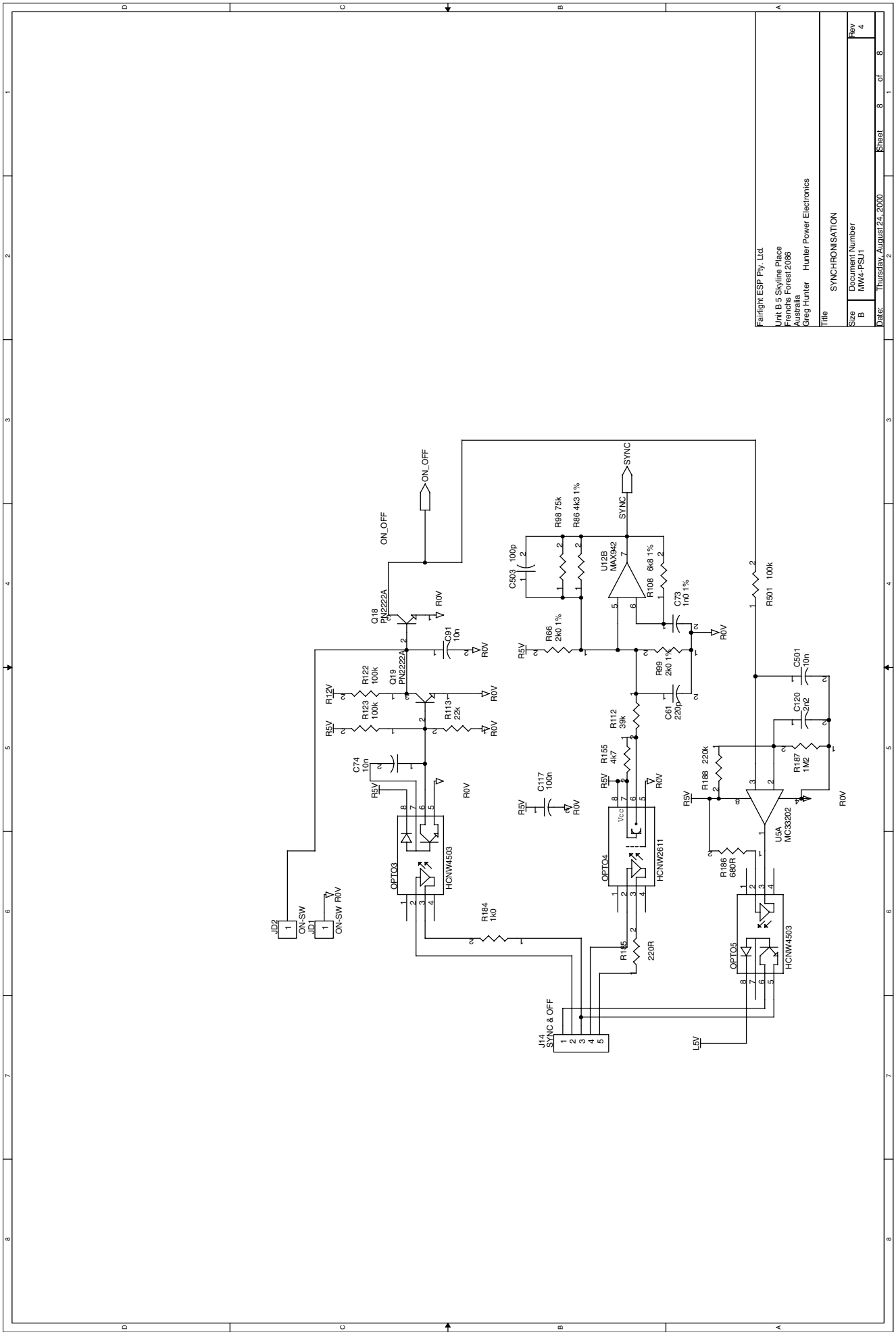
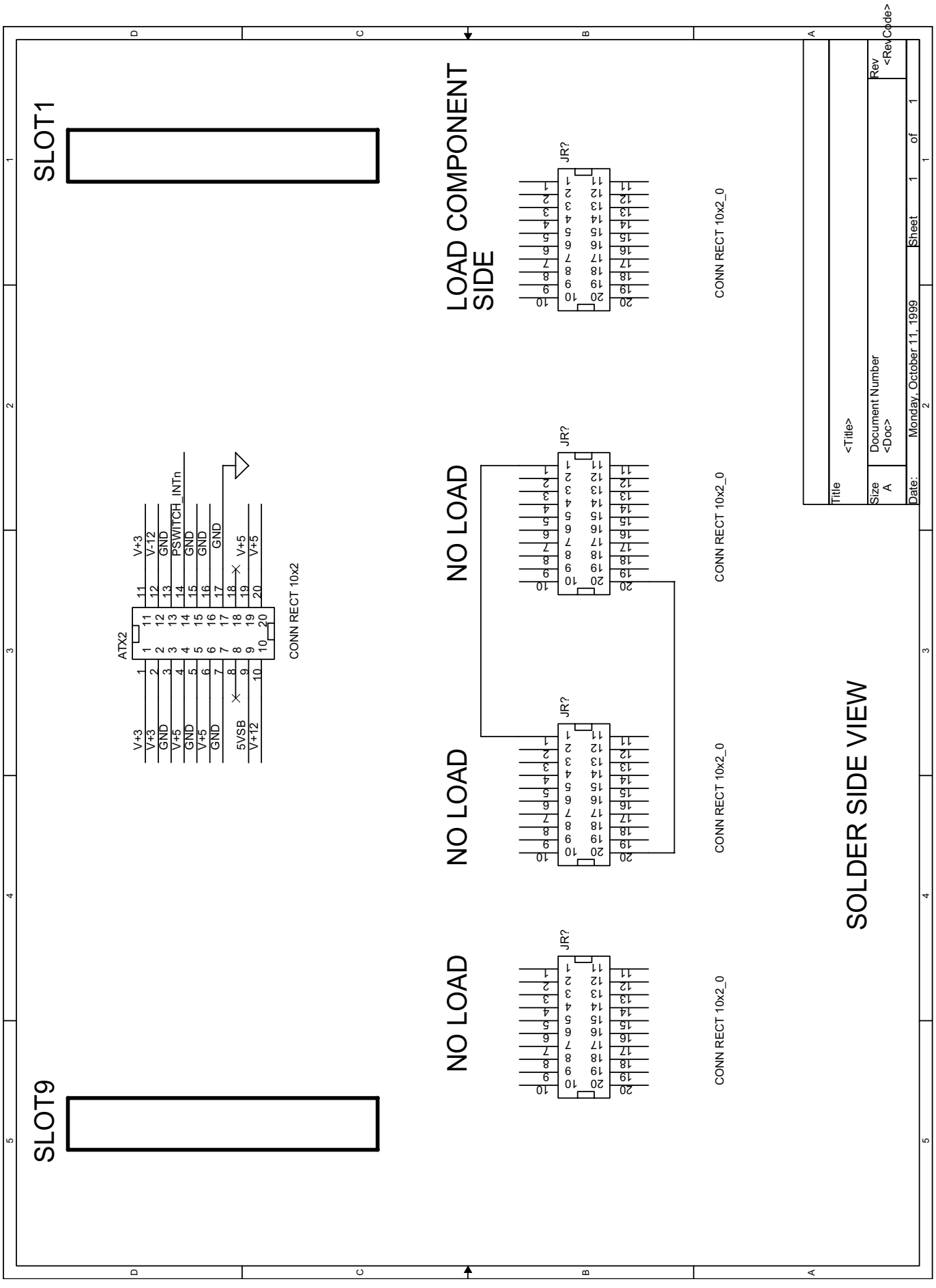
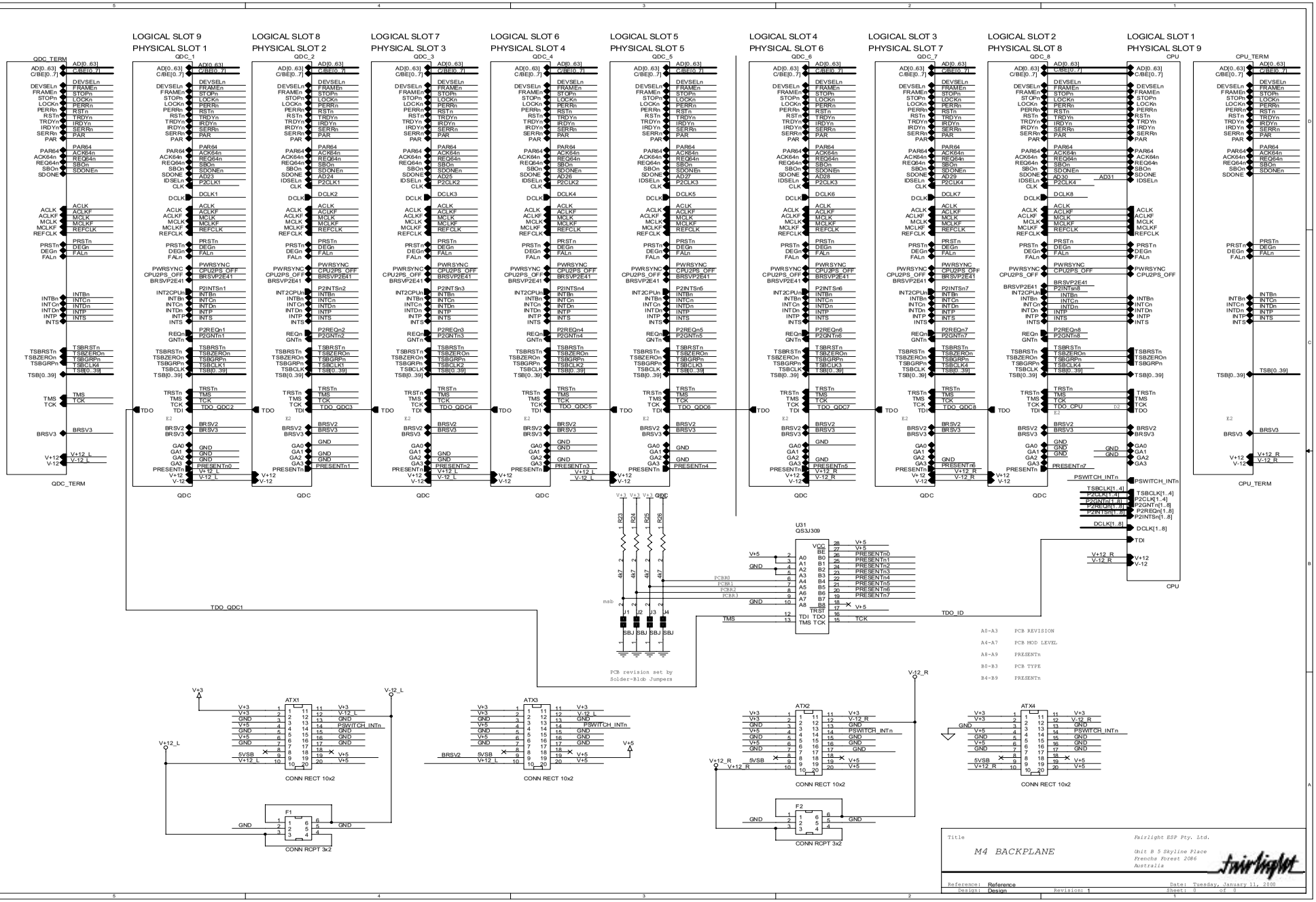

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
POWER FACTOR CORRECTION
Size B
Document Number MW4-PSU1
Rev 4
Date: Thursday, August 24, 2000
Sheet 7 of 8
400V
P0V
R13 100k 1W 350V 5%
R12 100k 1W 350V 5%
C10 470u 450V
C511 10n 630V
TP4 CON1
TP5 CON1
D2 MKP10 RHRP1560
4 Watts
R11 6R8 7W
C9 10n 400V
M3
L2 2uH
D12 RHRP1560
TP2 CON1
Q1 IRF460LC
Screen
SC1 screen
M2
TP1 CON1
R15 2k2
Z501 18V 1.3W
L5
L7 0.35mH
R39 5k6
R40 180R
C31 100u 10V
H.S. 30C/W
4k7 0.5W
R34
Q3 IRF840
BC549C
R38 820R
D18 1N4448
Z2 18V
D19 1N4448
Z3 10V
220k 350V 220k 350V
R37
R35
C18 2200u 25V
TP14 CON1
R12V
R22 22R
D502 MUR120
TP11 CON1
R19 470k 350V 1%
R18 470k 350V 1%
R21 470k 350V 1%
R20 470k 350V 1%
D53 1N4448
C108 47u 16V LL
R183 10k 1%
R182 2k0 1%
R181 O/C
R84 11k 1%
R97 O/C
C58 10n
C57 220n
R106 4k7
PFC_SYNC
TP10 CON1
C56 100n
C65 100n
C89 220n
C55 1n0 1%
R107 5k1 1%
TP9 CON1
SB130
D501
U9 ML4821
GND
CI
Vref
Vcc
OUT
PGND
Rt
OVP
SYNC
Ilim
IAout
IA-
IA+
ISine
EAout
EA-
Vrms
SS
R130 750R
R33 330k 350V 1%
R58 330k 350V 1%
R148 39k
C101 220n
C100 1u0
C102 1u0
R127 13k 1%
R171 4k7
C88 1n5
C87 1n5
R104 3k0
R105 180R
C69 470p
R170 4k7
C115 6n8
C81 330n
R131 36k 1%
R36 220k 350V 1%
R52 220k 350V 1%
D1 MR756
D10 MR756
R10 0R1 7W
14 Watts
BR1 GBU8K
C505 1nF Y
C508 1nF Y
C504 1nF Y
C507 1nF Y
NTC1 2R5
C4 2n2 Y
C8 470n X
C5 2n2 Y
GROUND
CHASSIS
EARTH
L3 5mH
L8 5mH
C510 2n2 Y
C509 2n2 Y
C12 220n X
C506 220n X
MV1 250V
J7 QC TAB
J3 QC TAB
ON_OFF


Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Greg Hunter Hunter Power Electronics
Title
SYNCHRONISATION
Size B
Document Number MW4-PSU1
Rev 4
Date: Thursday, August 24, 2000
Sheet 8 of 8
ON_OFF
SYNC
Q18 PN2222A
Q19 PN2222A
R0V
R5V
R12V
C91 10n
R122 100k
R123 100k
R113 22k
C74 10n
R184 1k0
R98 75k
R86 4k3 1%
C503 100p
U12B MAX942
R108 6k8 1%
C73 1n0 1%
R66 2k0 1%
R99 2k0 1%
C61 220p
R112 39k
R155 4k7
C117 100n
R501 100k
C501 10n
C120 2n2
R187 1M2
R188 220k
R186 680R
U5A MC33202
OPTO3 HCNW4503
OPTO4 HCNW2611
OPTO5 HCNW4503
R185 220R
JD2 ON-SW
JD1 ON-SW
J14 SYNC & OFF
L5V


SLOT1
SLOT9
LOAD COMPONENT SIDE
SOLDER SIDE VIEW
NO LOAD
NO LOAD
NO LOAD
ATX2
CONN RECT 10x2
JR?
CONN RECT 10x2_0
V+3
V+3
GND
V+5
GND
V+5
GND
5VSB
V+12
V-12
GND
PSWITCH_INTn
GND
GND
V+5
V+5
Title
<Title>
Size
A
Document Number
<Doc>
Rev
<RevCode>
Date:
Monday, October 11, 1999
Sheet
1
of
1


LOGICAL SLOT 9
PHYSICAL SLOT 1
LOGICAL SLOT 8
PHYSICAL SLOT 2
LOGICAL SLOT 7
PHYSICAL SLOT 3
LOGICAL SLOT 6
PHYSICAL SLOT 4
LOGICAL SLOT 5
PHYSICAL SLOT 5
LOGICAL SLOT 4
PHYSICAL SLOT 6
LOGICAL SLOT 3
PHYSICAL SLOT 7
LOGICAL SLOT 2
PHYSICAL SLOT 8
LOGICAL SLOT 1
PHYSICAL SLOT 9
QDC_TERM
QDC_1
QDC_2
QDC_3
QDC_4
QDC_5
QDC_6
QDC_7
QDC_8
CPU
CPU_TERM
QDC
CONN RECT 10x2
CONN RCPT 3x2
U31
QS3J309
PCB revision set by Solder-Blob Jumpers
PCB REVISION
PCB MOD LEVEL
PRESENTn
PCB TYPE
M4 BACKPLANE
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference
Design
Tuesday, January 11, 2000

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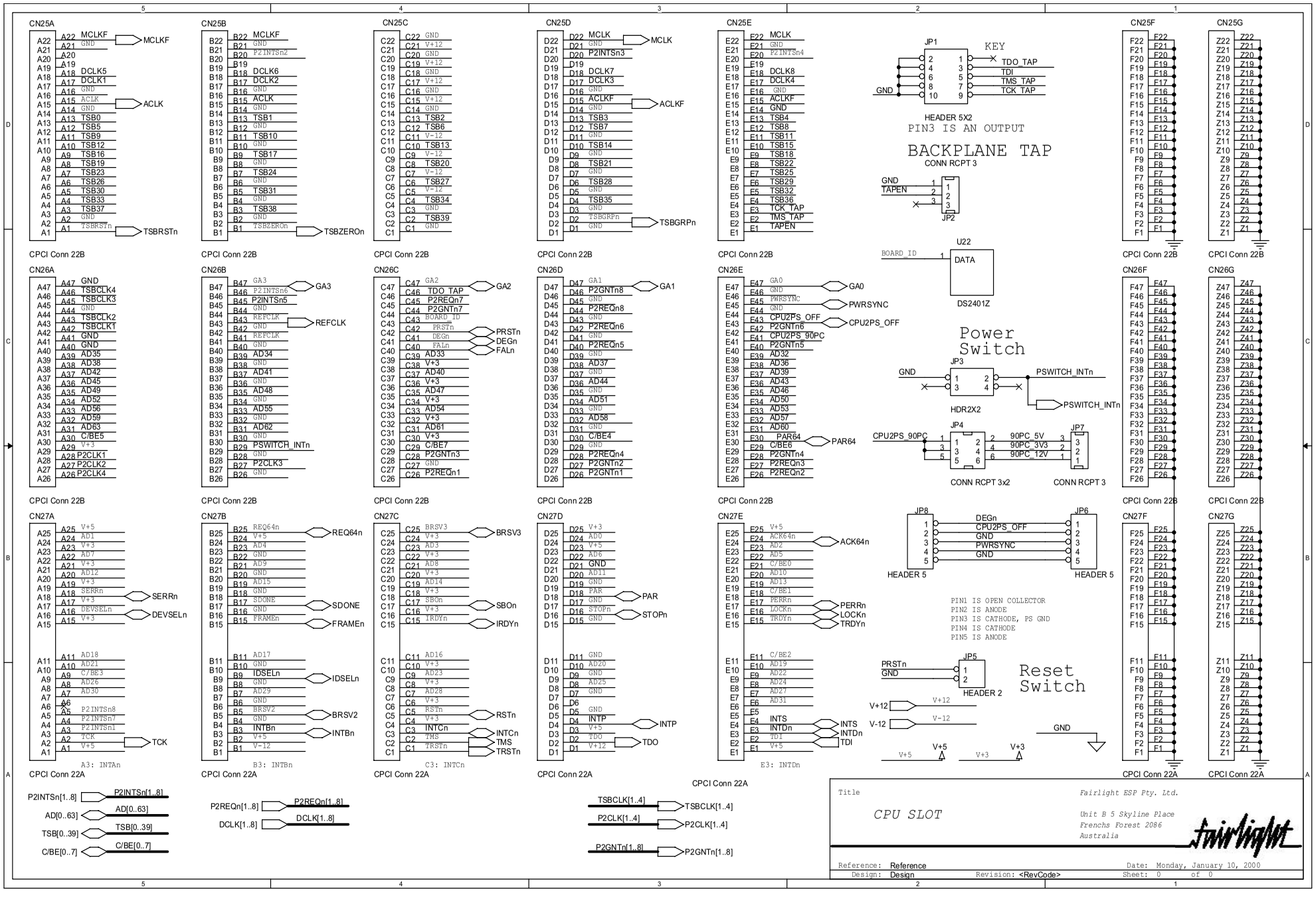
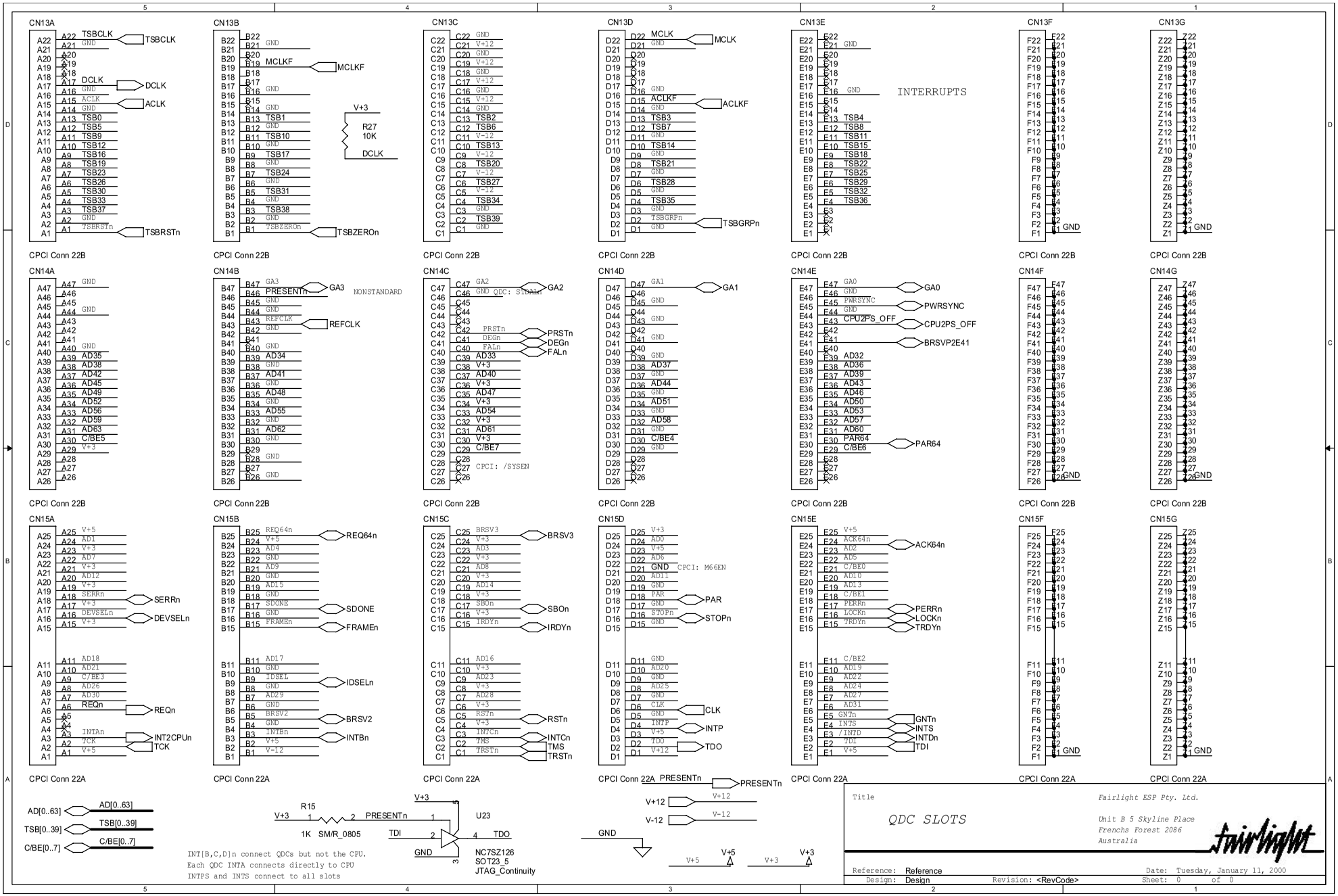
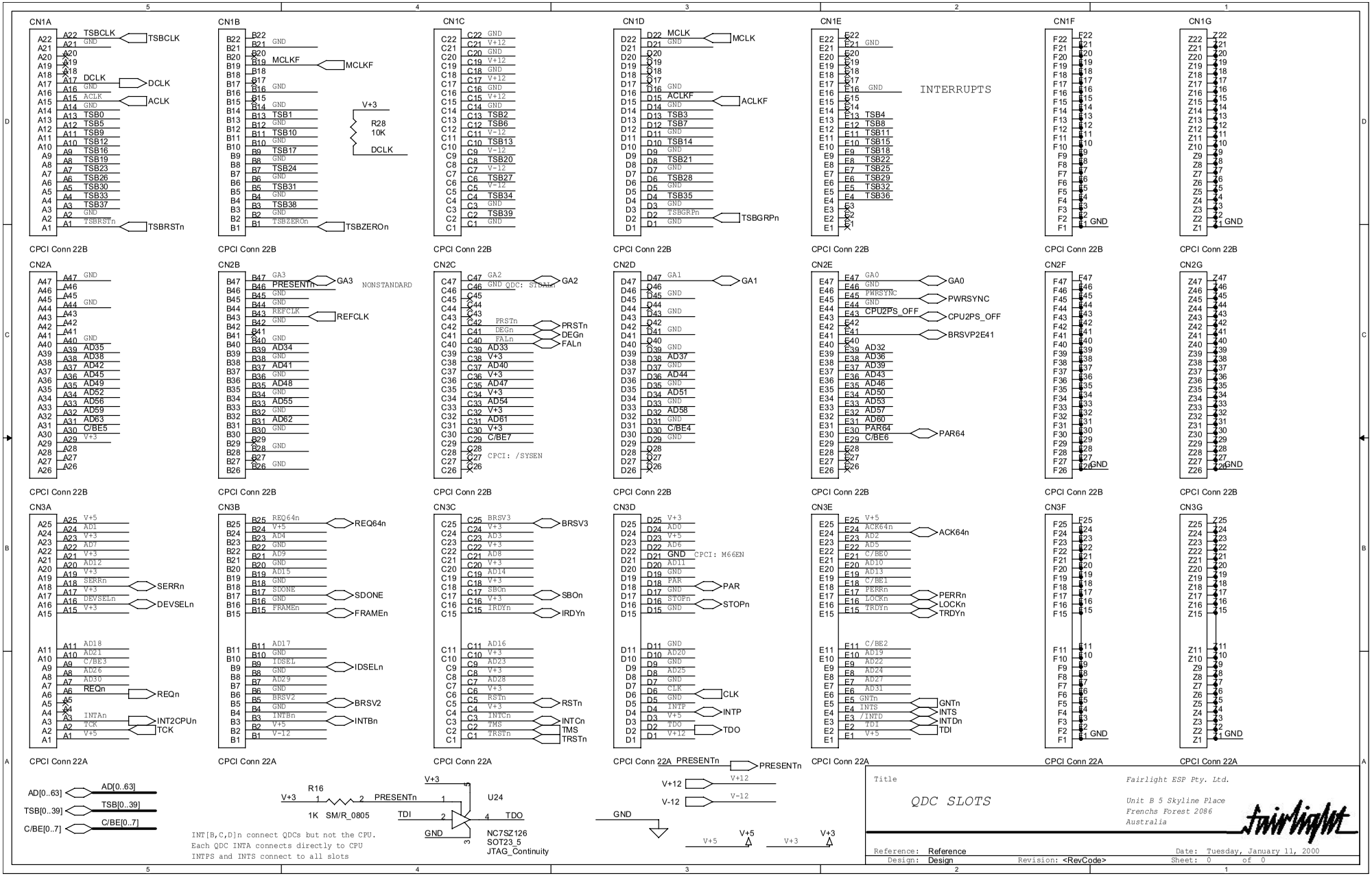
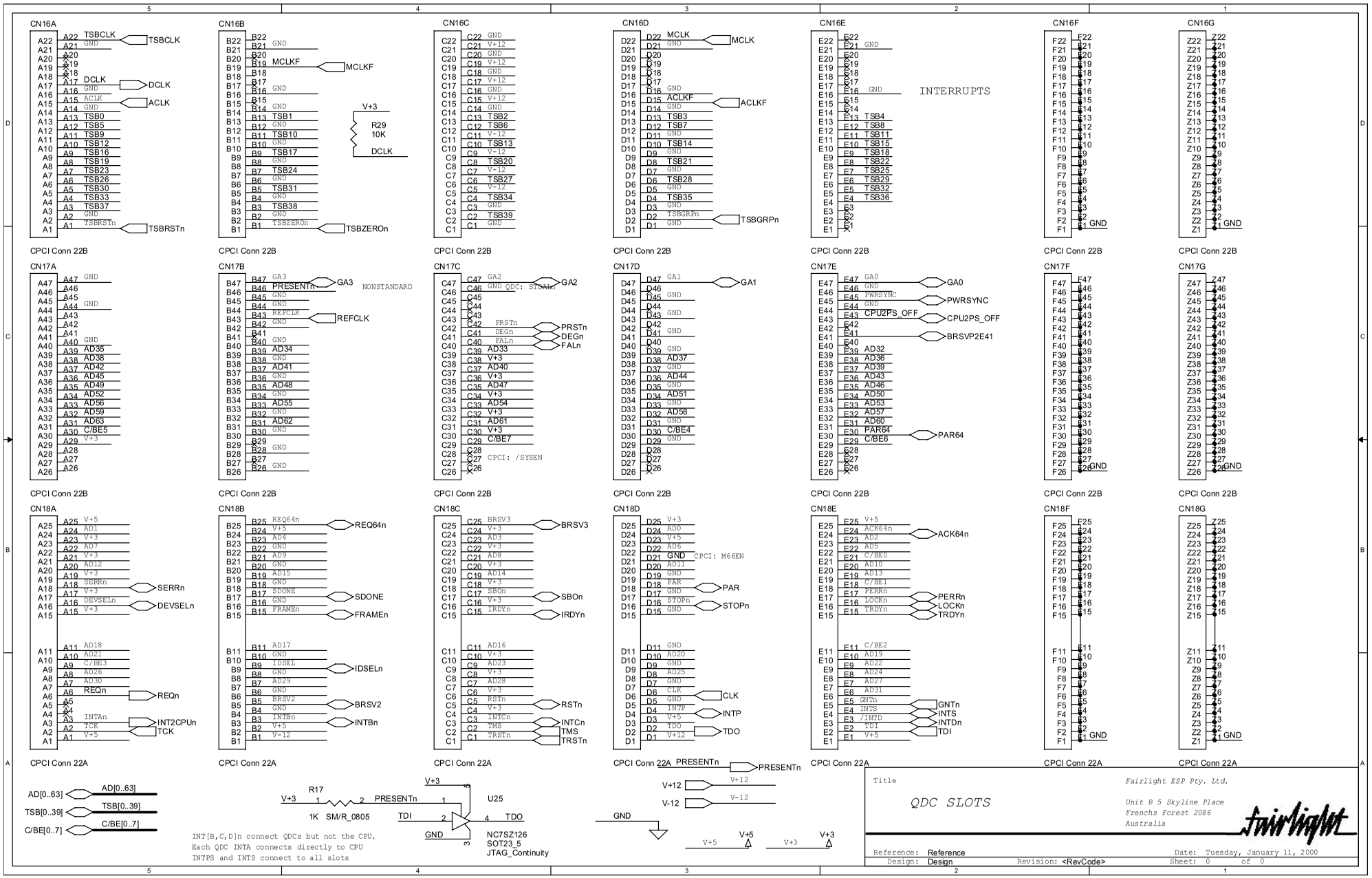

CN25A
CPCI Conn 22B
CN25B
CPCI Conn 22B
CN25C
CPCI Conn 22B
CN25D
CPCI Conn 22B
CN25E
CPCI Conn 22B
CN25F
CPCI Conn 22B
CN25G
CPCI Conn 22B
CN26A
CPCI Conn 22B
CN26B
CPCI Conn 22B
CN26C
CPCI Conn 22B
CN26D
CPCI Conn 22B
CN26E
CPCI Conn 22B
CN26F
CPCI Conn 22B
CN26G
CPCI Conn 22B
CN27A
A3: INTAn
CPCI Conn 22A
CN27B
B3: INTBn
CPCI Conn 22A
CN27C
C3: INTCn
CPCI Conn 22A
CN27D
CPCI Conn 22A
CN27E
E3: INTDn
CPCI Conn 22A
CN27F
CPCI Conn 22A
CN27G
CPCI Conn 22A
JP1
KEY
TDO_TAP
TDI
TMS_TAP
TCK_TAP
HEADER 5X2
PIN3 IS AN OUTPUT
BACKPLANE TAP
CONN RCPT 3
JP2
U22
DS2401Z
Power Switch
JP3
HDR2X2
JP4
CONN RCPT 3x2
JP7
CONN RCPT 3
JP8
HEADER 5
JP6
HEADER 5
PIN1 IS OPEN COLLECTOR
PIN2 IS ANODE
PIN3 IS CATHODE, PS GND
PIN4 IS CATHODE
PIN5 IS ANODE
JP5
HEADER 2
Reset Switch
P2INTSn[1..8]
AD[0..63]
TSB[0..39]
C/BE[0..7]
P2REQn[1..8]
DCLK[1..8]
TSBCLK[1..4]
P2CLK[1..4]
P2GNTn[1..8]
Title
CPU SLOT
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Monday, January 10, 2000
Sheet: 0 of 0


CN13A
CN13B
CN13C
CN13D
CN13E
CN13F
CN13G
INTERRUPTS
CPCI Conn 22B
CN14A
CN14B
CN14C
CN14D
CN14E
CN14F
CN14G
NONSTANDARD
CN15A
CN15B
CN15C
CN15D
CN15E
CN15F
CN15G
CPCI Conn 22A
R15
1K SM/R_0805
R27
10K
U23
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0


CN1A
CPCI Conn 22B
CN1B
CPCI Conn 22B
MCLKF
V+3
R28
10K
DCLK
CN1C
CPCI Conn 22B
CN1D
CPCI Conn 22B
MCLK
ACLKF
TSBGRPn
CN1E
CPCI Conn 22B
INTERRUPTS
CN1F
CPCI Conn 22B
CN1G
CPCI Conn 22B
CN2A
CPCI Conn 22B
CN2B
CPCI Conn 22B
GA3
NONSTANDARD
REFCLK
CN2C
CPCI Conn 22B
GA2
PRSTn
DEGn
FALn
CN2D
CPCI Conn 22B
GA1
CN2E
CPCI Conn 22B
GA0
PWRSYNC
CPU2PS_OFF
BRSVP2E41
PAR64
CN2F
CPCI Conn 22B
CN2G
CPCI Conn 22B
CN3A
CPCI Conn 22B
SERRn
DEVSELn
REQn
INT2CPUn
TCK
CN3B
CPCI Conn 22B
REQ64n
SDONE
FRAMEn
IDSELn
BRSV2
INTBn
CN3C
CPCI Conn 22B
BRSV3
SBOn
IRDYn
RSTn
INTCn
TMS
TRSTn
CN3D
CPCI Conn 22B
PAR
STOPn
CLK
INTP
TDO
CN3E
CPCI Conn 22B
ACK64n
PERRn
LOCKn
TRDYn
GNTn
INTS
INTDn
TDI
CN3F
CPCI Conn 22B
CN3G
CPCI Conn 22B
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
CPCI Conn 22A
R16
1K SM/R_0805
PRESENTn
TDI
TDO
GND
U24
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
CPCI Conn 22A
PRESENTn
V+12
V-12
GND
V+5
V+3
CPCI Conn 22A
CPCI Conn 22A
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0


CN16A
CPCI Conn 22B
TSBCLK
DCLK
ACLK
TSBRSTn
CN16B
CPCI Conn 22B
MCLKF
V+3
R29
10K
DCLK
TSBZEROn
CN16C
CPCI Conn 22B
CN16D
CPCI Conn 22B
MCLK
ACLKF
TSBGRPn
CN16E
CPCI Conn 22B
INTERRUPTS
CN16F
CPCI Conn 22B
CN16G
CPCI Conn 22B
CN17A
CPCI Conn 22B
CN17B
CPCI Conn 22B
GA3
NONSTANDARD
PRESENTn
REFCLK
CN17C
CPCI Conn 22B
GA2
PRSTn
DEGn
FALn
CPCI: /SYSEN
CN17D
CPCI Conn 22B
GA1
CN17E
CPCI Conn 22B
GA0
PWRSYNC
CPU2PS_OFF
CPU2PS_OFF
BRSVP2E41
PAR64
CN17F
CPCI Conn 22B
CN17G
CPCI Conn 22B
CN18A
CPCI Conn 22B
SERRn
DEVSELn
REQn
INT2CPUn
TCK
CN18B
CPCI Conn 22B
REQ64n
SDONE
IDSELn
FRAMEn
BRSV2
INTBn
CN18C
CPCI Conn 22B
BRSV3
SBOn
IRDYn
RSTn
INTCn
TMS
TRSTn
CN18D
CPCI Conn 22B
CPCI: M66EN
PAR
STOPn
CLK
INTP
TDO
CN18E
CPCI Conn 22B
ACK64n
PERRn
LOCKn
TRDYn
GNTn
INTS
INTDn
TDI
CN18F
CPCI Conn 22B
CN18G
CPCI Conn 22B
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
R17
1K SM/R_0805
PRESENTn
TDI
TDO
U25
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
V+12
V-12
GND
V+5
V+3
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0

SLOT1

V-12 C1 10UF/35V/1ohm, C2 10UF/35V/1ohm

V+12 C3 10UF/35V/1ohm, C4 10UF/35V/1ohm

V+3 C5 22UF/16V/1.1ohm, C6 22UF/16V/1.1ohm, C65 22UF/16V/1.1ohm

V+5 C7 22UF/16V/1.1ohm, C8 22UF/16V/1.1ohm, C66 22UF/16V/1.1ohm

SLOT2

V-12 C9 10UF/35V/1ohm, C10 10UF/35V/1ohm

V+12 C11 10UF/35V/1ohm, C12 10UF/35V/1ohm

V+3 C13 22UF/16V/1.1ohm, C14 22UF/16V/1.1ohm, C67 22UF/16V/1.1ohm

V+5 C15 22UF/16V/1.1ohm, C16 22UF/16V/1.1ohm, C68 22UF/16V/1.1ohm

SLOT3

V-12 C17 10UF/35V/1ohm, C18 10UF/35V/1ohm

V+12 C19 10UF/35V/1ohm, C20 10UF/35V/1ohm

V+3 C21 22UF/16V/1.1ohm, C22 22UF/16V/1.1ohm, C69 22UF/16V/1.1ohm

V+5 C23 22UF/16V/1.1ohm, C24 22UF/16V/1.1ohm, C80 22UF/16V/1.1ohm

SLOT4

V-12 C25 10UF/35V/1ohm, C26 10UF/35V/1ohm

V+12 C27 10UF/35V/1ohm, C28 10UF/35V/1ohm

V+3 C29 22UF/16V/1.1ohm, C30 22UF/16V/1.1ohm, C70 22UF/16V/1.1ohm

V+5 C31 22UF/16V/1.1ohm, C32 22UF/16V/1.1ohm, C71 22UF/16V/1.1ohm

SLOT5

V-12 C33 10UF/35V/1ohm

V+12 C36 10UF/35V/1ohm

V+3 C37 22UF/16V/1.1ohm, C38 22UF/16V/1.1ohm, C72 22UF/16V/1.1ohm

V+5 C39 22UF/16V/1.1ohm, C40 22UF/16V/1.1ohm, C73 22UF/16V/1.1ohm

U12 SN74S1053: TSB0 TSB1 TSB2 TSB3 TSB4 TSB6 TSB7 TSB8 TSB5 TSB9 TSB10 TSB11 TSB12 TSB13 TSB14 TSB15

U13 SN74S1053: TSB16 TSB17 TSB183 TSB19 TSB204 TSB21 TSB225 TSB23 TSB24 TSB25 TSB26 TSB27 TSB28 TSB29 TSB30 TSB32

U14 SN74S1053: TSB33 TSB31 TSB343 TSB35 TSB364 TSB37 TSB38 TSB396 TSBZERQn PRSTn DEGn TSBGRPn TSBRSTn REFCLK FALn

U15 SN74S1053: AD35 AD34 AD33 AD32 AD38 AD37 AD36 AD42 AD41 AD40 AD39 AD45 AD44 AD43 AD49 AD48

U16 SN74S1053: AD47 AD46 AD52 AD51 AD50 AD56 AD55 AD53 AD54 AD59 AD58 AD57 AD63 AD62 AD61 AD60

U17 SN74S1053: C/BE5 PAR64 C/BE4 C/BE6 C/BE7 REQ64n BRSV3 AD1 ACK64n AD0 AD3 AD2 AD6 AD7 AD5

U18 SN74S1053: AD8 AD9 C/BE0 AD11 AD12 AD15 AD14 AD10 AD13 SERRn PAR C/BE1 SDONE PERRn SBOn DEVSELn

U19 SN74S1053: STOPn LOCKn FRAMEn IRDYn TRDYn AD18 AD17 AD16 C/BE2 AD21 AD20 AD19 C/BE3 AD23 AD22 AD26

U20 SN74S1053: AD25 AD24 AD30 AD29 AD28 AD27 AD31 RSTn INTS INTP INTAn INTCn INTBn INTDn

R13 82R REFCLK R14 82R

R1 220R R3 220R R2 330R R4 330R TMS TCK

R5 82R R6 82R MCLK

R9 82R R10 82R ACLK

R7 82R R8 82R MCLKF

R11 82R R12 82R ACLKF

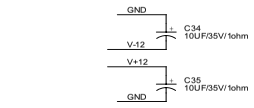
AD[0..63] TSB[0..39] C/BE[0..7]

INTERRUPTS

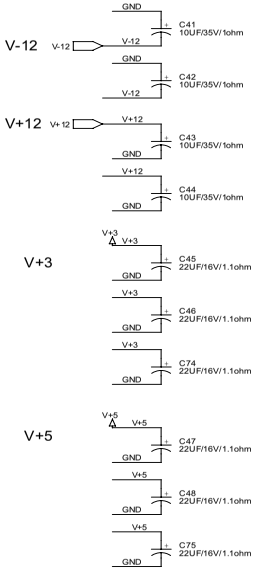
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots

ALL BYPASSES ARE AVX TANTALUM SM/CT_7343 (D CASE) PARTS, WITH 3X VOLTAGE RATINGS

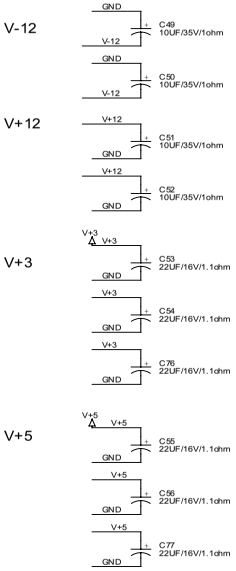
Title	QDC SLOTS
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place
	Frenchs Forest 2086
	Australia
Reference:	Reference
Design:	Design
Revision:	<RevCode>
Date:	Monday, October 11, 1999
Sheet:	0 of 0



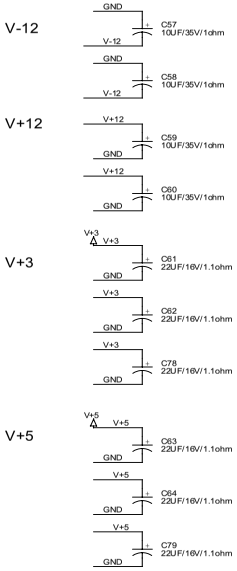
SLOT6

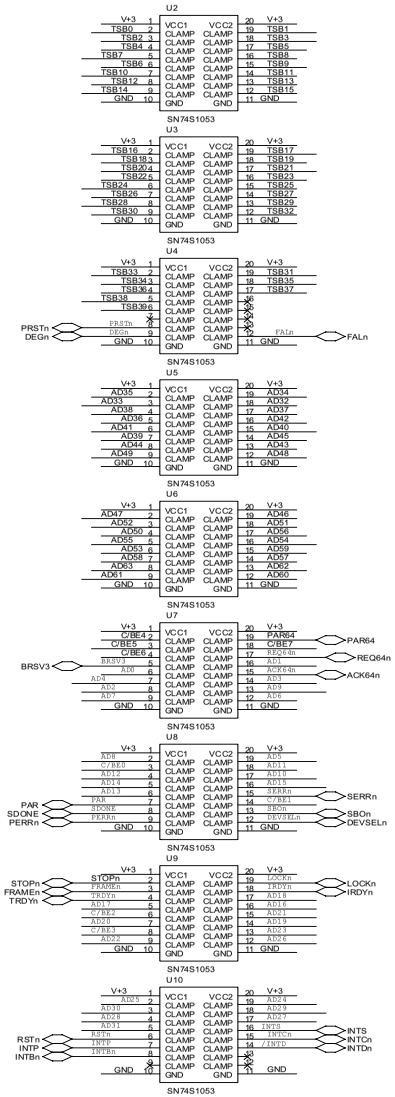


SLOT7



SLOT8



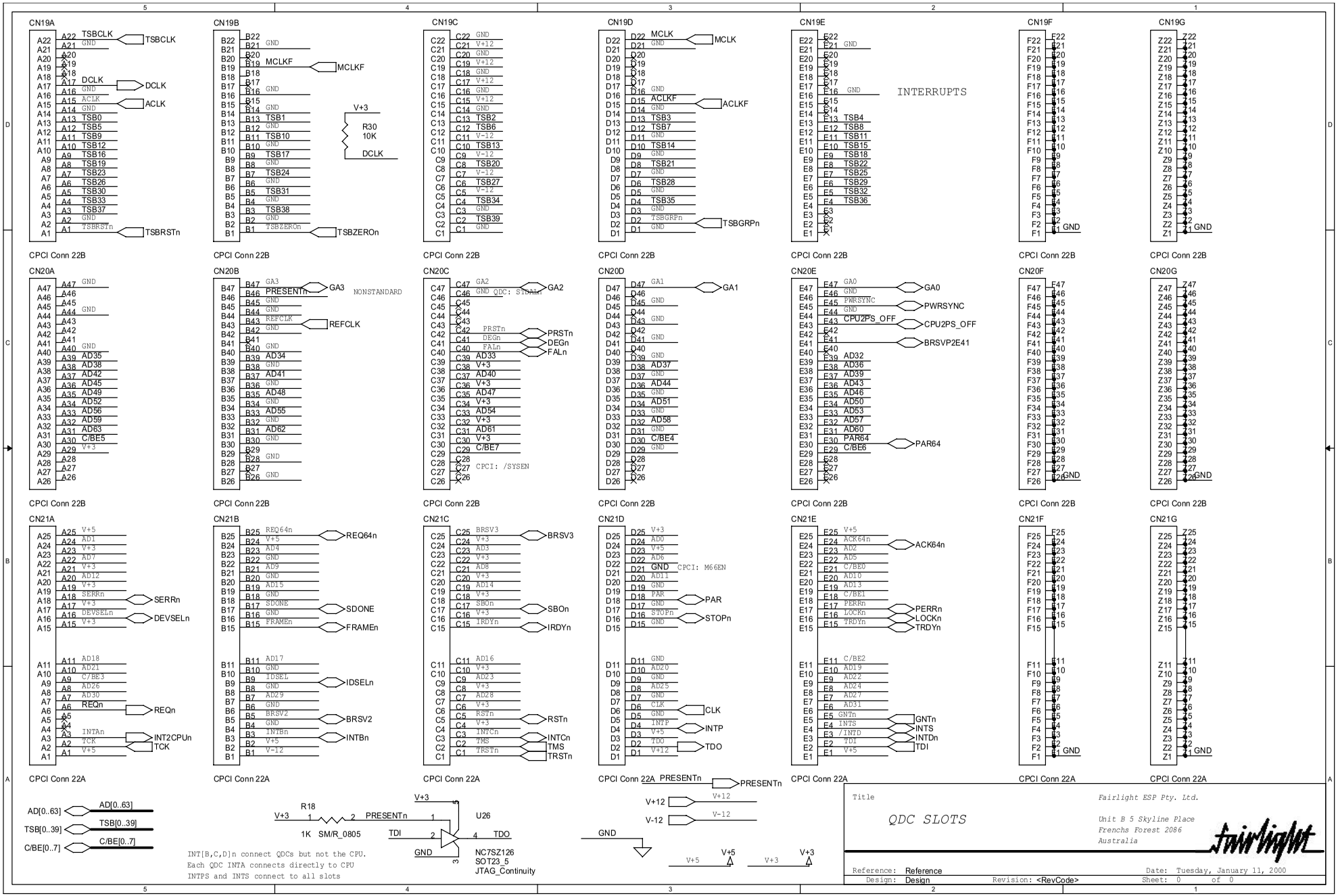


INTERRUPTS

INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots

Title	QDC SLOTS
	Fairlight ESP Pty. Ltd.
	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Reference:	Reference
Design:	Design
Revision:	<RevCode>
Date:	Monday, October 11, 1999
Sheet:	0 of 0


CN19A
CN19B
CN19C
CN19D
CN19E
CN19F
CN19G
INTERRUPTS
CPCI Conn 22B
CN20A
CN20B
CN20C
CN20D
CN20E
CN20F
CN20G
CN21A
CN21B
CN21C
CN21D
CN21E
CN21F
CN21G
CPCI Conn 22A
R18
1K SM/R_0805
R30
10K
U26
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0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INTERRUPTS
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CN21C
CN21D
CN21E
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1K SM/R_0805
R30
10K
U26
NC7SZ126
SOT23_5
JTAG_Continuity
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Fairlight ESP Pty. Ltd.
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Reference: Reference
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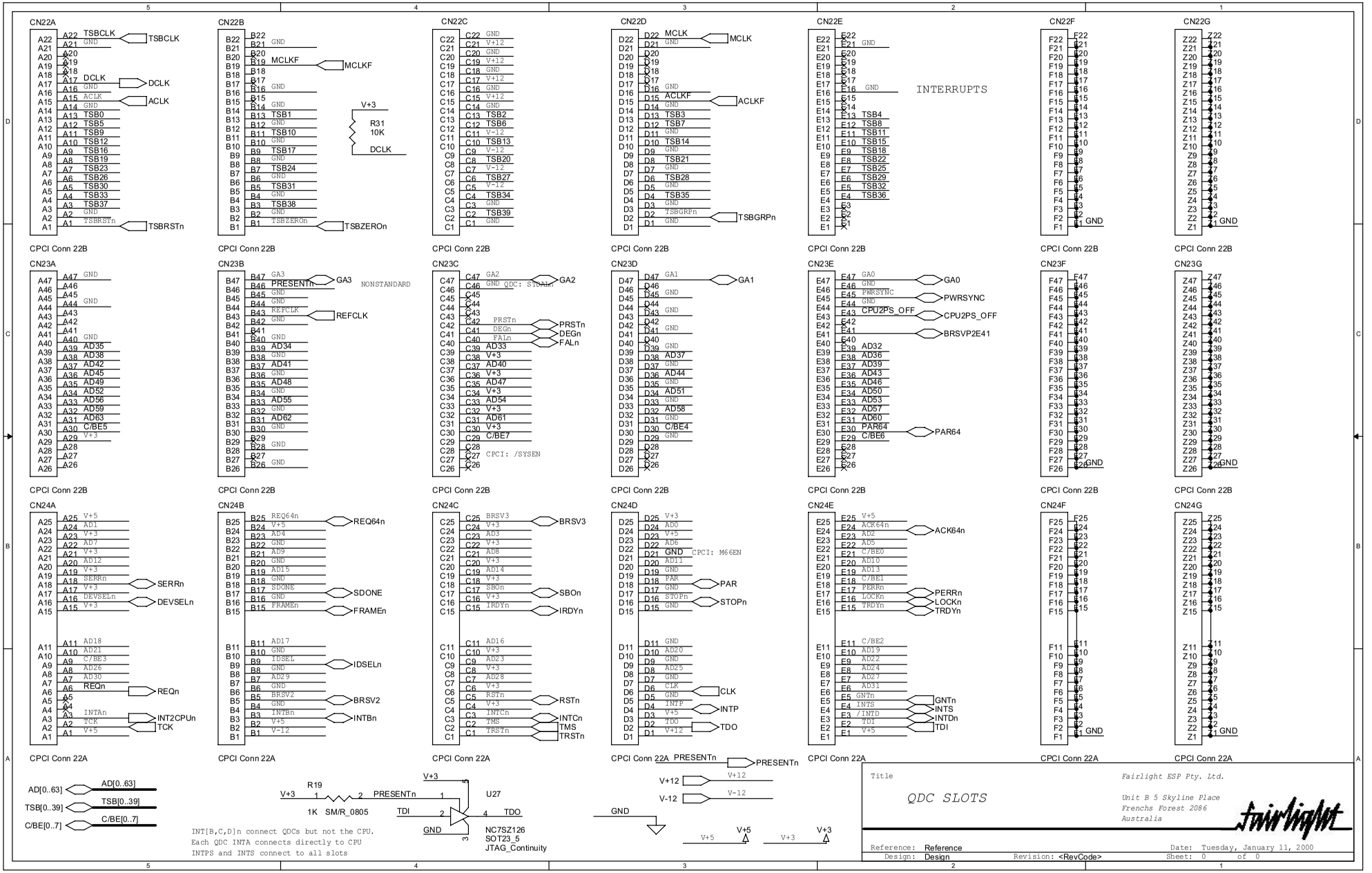
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0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CN22D
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CN22F
CN22G
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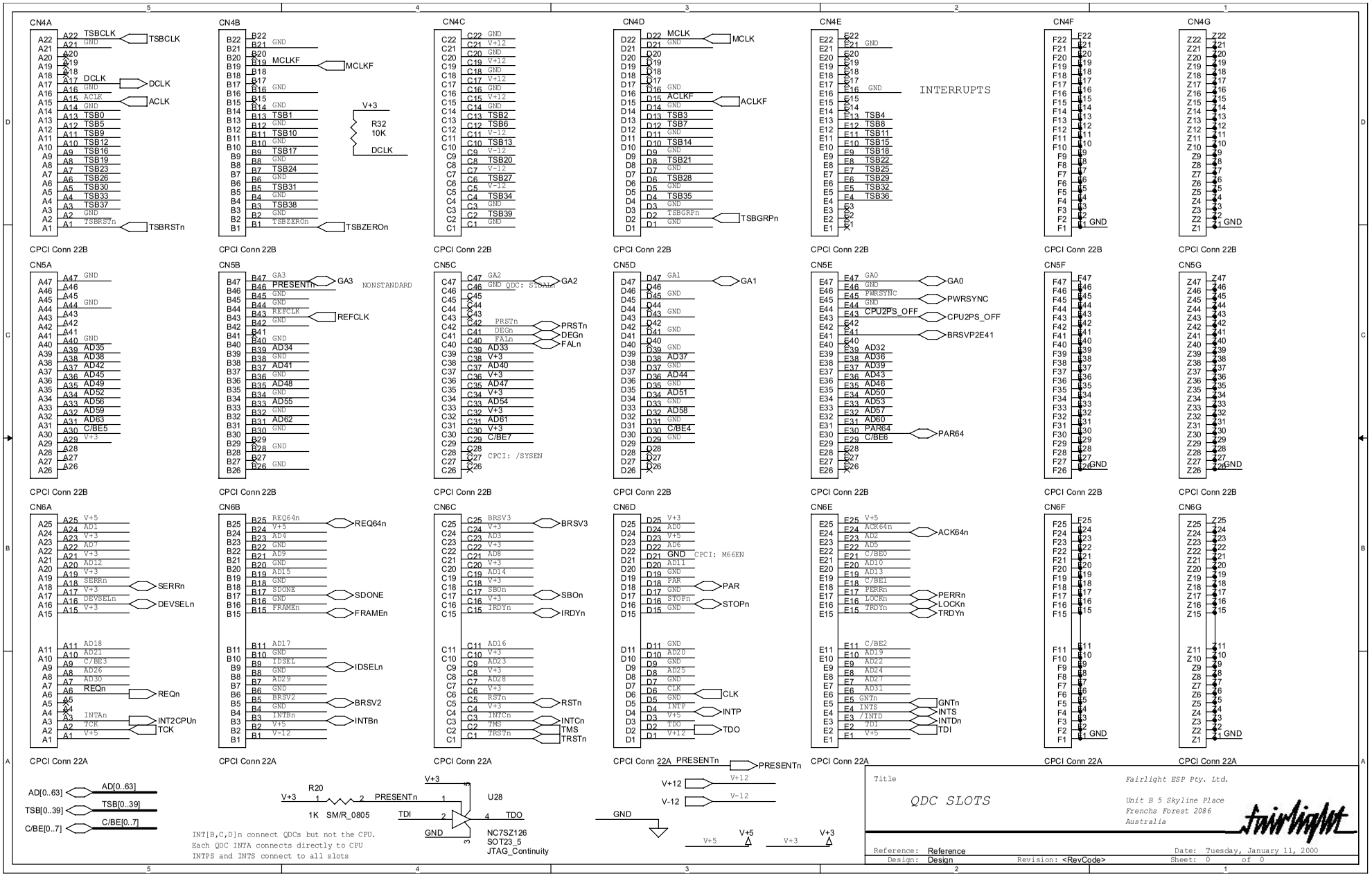
CN23B
CN23C
CN23D
CN23E
CN23F
CN23G
NONSTANDARD
CPCI: /SYSEN
CPCI Conn 22B
CN24A
CN24B
CN24C
CN24D
CN24E
CN24F
CN24G
CPCI: M66EN
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
R19
1K SM/R_0805
R31
10K
U27
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0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DCLK
ACLK
TSBRSTn
CN4B
MCLKF
V+3
R32
10K
DCLK
TSBZEROn
CN4C
CN4D
MCLK
ACLKF
TSBGRPn
CN4E
INTERRUPTS
CN4F
CN4G
CN5A
CN5B
GA3
NONSTANDARD
REFCLK
CN5C
GA2
PRSTn
DEGn
FALn
CPCI: /SYSEN
CN5D
GA1
CN5E
GA0
PWRSYNC
CPU2PS_OFF
BRSVP2E41
PAR64
CN5F
CN5G
CN6A
SERRn
DEVSELn
REQn
INT2CPUn
TCK
CN6B
REQ64n
SDONE
FRAMEn
IDSELn
BRSV2
INTBn
CN6C
BRSV3
SBOn
IRDYn
RSTn
INTCn
TMS
TRSTn
CN6D
CPCI: M66EN
PAR
STOPn
CLK
INTP
TDO
CN6E
ACK64n
PERRn
LOCKn
TRDYn
GNTn
INTS
INTDn
TDI
CN6F
CN6G
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
R20
1K SM/R_0805
PRESENTn
U28
TDI
TDO
GND
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
V+12
V-12
V+5
V+3
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
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Design: Design
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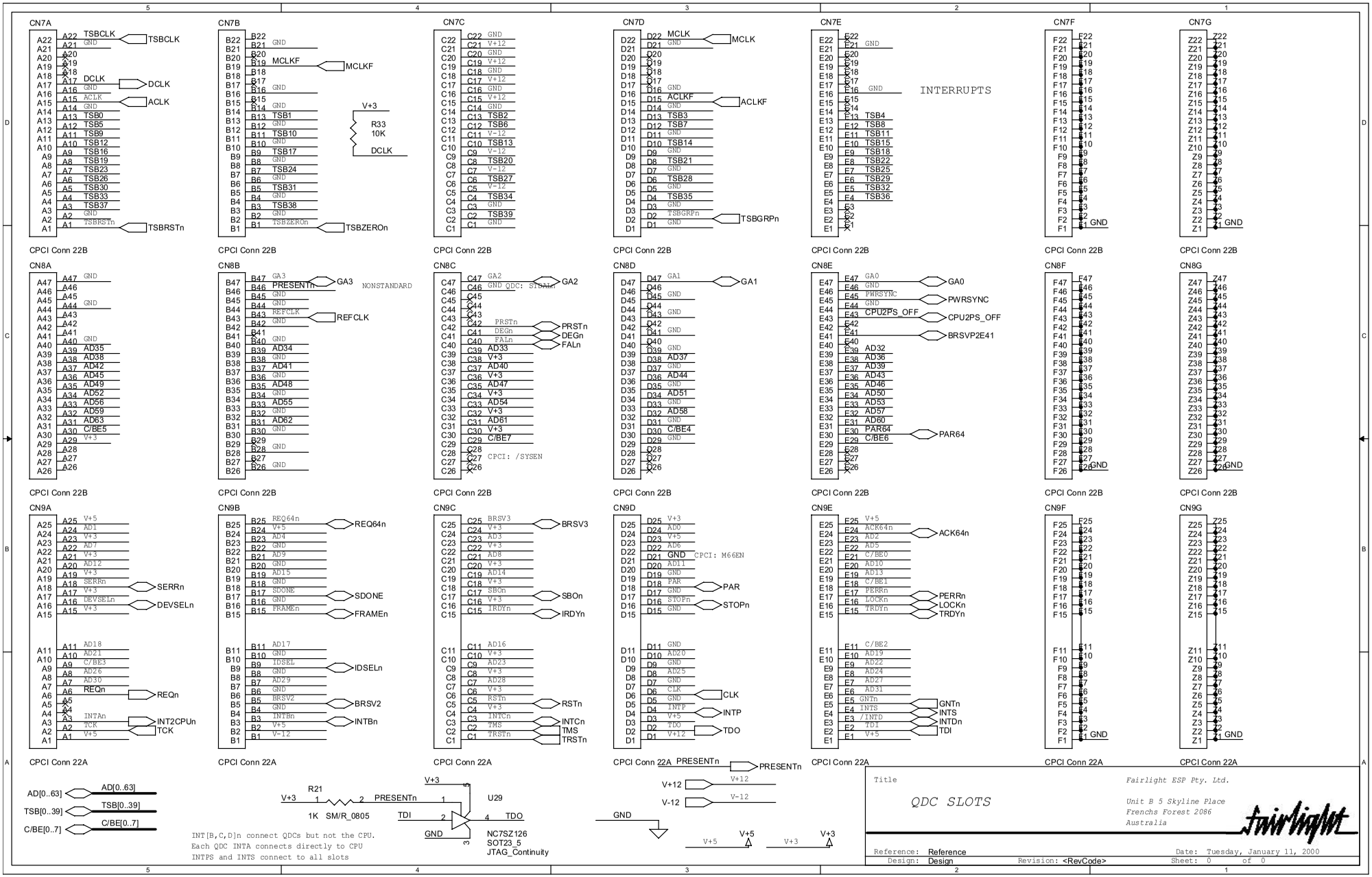
Date: Tuesday, January 11, 2000
Sheet: 0 of 0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CN7B
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CN7D
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CN7F
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INTERRUPTS
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CN8A
CN8B
CN8C
CN8D
CN8E
CN8F
CN8G
NONSTANDARD
CN9A
CN9B
CN9C
CN9D
CN9E
CN9F
CN9G
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
R21
1K SM/R_0805
U29
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
INTPS and INTS connect to all slots
Title
QDC SLOTS
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Reference: Reference
Design: Design
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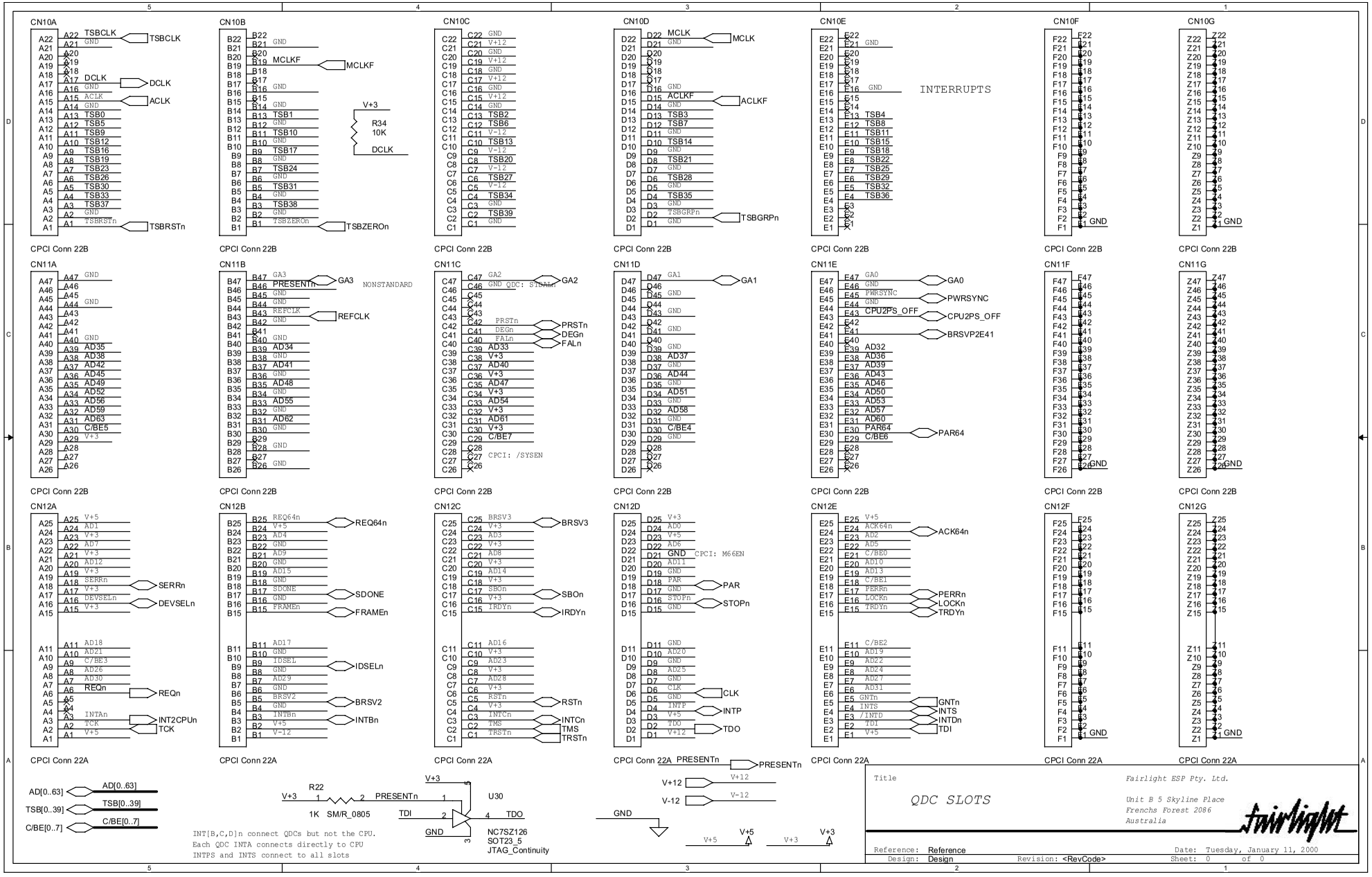
Date: Tuesday, January 11, 2000
Sheet: 0 of 0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CN10C
CN10D
CN10E
CN10F
CN10G
INTERRUPTS
CPCI Conn 22B
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CN11B
NONSTANDARD
CN11C
CPCI: /SYSEN
CN11D
CN11E
CN11F
CN11G
CN12A
CN12B
CN12C
CN12D
CPCI: M66EN
CN12E
CN12F
CN12G
CPCI Conn 22A
AD[0..63]
TSB[0..39]
C/BE[0..7]
R22
1K SM/R_0805
U30
NC7SZ126
SOT23_5
JTAG_Continuity
INT[B,C,D]n connect QDCs but not the CPU.
Each QDC INTA connects directly to CPU
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Title
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Unit B 5 Skyline Place
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Australia
Reference: Reference
Design: Design
Revision: <RevCode>
Date: Tuesday, January 11, 2000
Sheet: 0 of 0

25.0 MFX Console

25.1 MFX010 Conroller Card Description

The MFX keyboard is a console designed to facilitate the use of post-production software on the MFX.

The MFX keyboard contains two circuit boards. MFX010 is the controller board for the MFX console, containing the Microprocessor. The other board, MFK, is used to decode the switches and trigger keys.

25.1.1 68000 Master Processor

(refer schematic MFX010-CPU (page 2 of 8))

The 68000 is responsible for the processing tasks in the MFX as it handles every task including scanning the 24 trigger keys. It has ROM, RAM and non-volatile RAM to store and execute programs and data.

The peripherals of the 68000 are memory mapped in the usual way with the high bits of the address buss determining the active peripheral. Each peripheral capable of generating interrupts is assigned to a different interrupt level.

25.1.2 ROM's

(refer schematic MFX010-MEMORY (page 3 of 8))

Two 8 bit EPROM's are used in parallel to provide the 16-bit boot code required by the 68000. These EPROM's are 27256 varieties with access times of 170ns or better. When accessing these EPROM's, no wait states are required by the 68000 allowing full-speed operation.

On power-up or after a reset, the EPROM's are mapped at location 0, as this is where the 68000 loads its initial stack pointer and program counter. The EPROM's can also be accessed at location $100000H. By setting the signal OVLY low (U9 pin 17) the EPROM is mapped out of location 0 and replaced by static RAM. This allows the exception vector locations to be modified by software. The OVLY signal is set high by reset. Regardless of the state of OVLY, the EPROM's may be accessed starting at $100000H.

The first instruction of the EPROM is to set OVLY low. If this does not occur then the processor is probably not able to execute any instructions. If the processor does not even load the stack pointer and program counter then the problem is very fundamental, and is not simply problems with the address or data lines.

25.1.3 RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Four 8-bit static RAM's are used in parallel to provide the 16-bit wide memory space in which to execute code. Normally 256K-bit RAM's are installed giving 64K words of memory. The memory is mapped starting at location 0. This allows direct access to the 68000 exception vectors, which occupy the first $200H words.

On power-up or reset, the signal OVLY is high, mapping the EPROM's to location 0 and preventing access to the RAM's. Normally, the first instruction executed is sets OVLY low,

mapping the RAM to location 0. OVLY should remain low until power is removed or the processor is reset.

The MFX keyboard has been designed to allow downloading of software from the Series III CMI, eliminating the need for costly EPROM updates. The task of the boot code in the EPROM's is to move the application code from the non-volatile memory to the RAM for execution.

25.1.4 Non-volatile RAM

(refer schematic MFX010-MEMORY (page 3 of 8))

Three 8K by 8-bit static RAM with battery-backup is provided to store programs configuration setups and data. This RAM is protected by a DS1234 non-volatile controller (U38), which controls write-protection and battery usage. The memory may be configured to be read-only or read-write and volatile or non-volatile. Normally the memory is kept as ready-only non- volatile memory, and changed to- read-write memory only when the data is being changed.

As this memory space is only 8 bits wide, it is not possible to execute programs directly from this RAM. At a temperature of 25'C, the BR2325 battery should provide a life of 8 years. Care should be taken to avoid exposing the MFX to extremes of temperature for long periods of time, as elevated temperature decreases the battery life rapidly.

At the time of writing this document, 100% CMOS RAM's are only made by Toshiba and are proving difficult to obtain. However they offer such low stand-by currents that they would offer non-volatility for the shelf life of the battery (> 10 years).

There is a jumper block provided which allows selection of a variable number of wait states for the non-volatile RAM - either 0, 2, 4 or 6 wait states. This may be necessary as the DS1234 shortens the access times of- the RAM by around 30ns. The actual setting used depends on the speed of the installed static RAM.

25.1.5 Address Decoding

(refer schematic MFX010-CPU (page 2 of 8))

The address decoding is performed by two 74ACT138 demultiplexers (U21 and U26) and half of a 74HCT138 demultiplexer (U27). The 16 megabyte memory space of the 68000 is divided up into sixteen 1 megabyte areas by the two 74ACT138, with each register or peripheral given ifs own area. All the peripherals decoded by U26 are no wait-state devices, whilst those decoded by U21 must supply an open collector /DTACK signal.

The second last address space is supplied to the 74HCT138, which subdivides this space into four areas for use by peripherals which require synchronization to the 1MHz E clock of the 68000. The /CS6800 signal tells the 68000 to synchronise to the E clock by, asserting VPA low whenever this address range is selected. The highest 1 megabyte address space should be left vacant, as this space is selected whenever an interrupt acknowledge cycle is commenced.

/DTACK is generated by all four DUARTs (U7, U8, U9 and U10) and by the 74HC175 (U33). Whenever the demultiplexer U26 is selected, U33 is reset causing /DTACK to be asserted low. Whenever the non-volatile RAM is selected, the select signal is shifted through the flip-flops of U33 on the rising edge of PCLK (10MHz) until is appears at the link block (W4) causing / DTACK to be asserted low.

25.1.6 LED Circuitry

(refer schematic MFX010-DISPLAY (page 6 of 8))

The LED's controlled by the MFX are arranged into rows and columns, and lit using a multiplexed scheme. Under this scheme each LED is pulsed on for 1ms with a high current, and then turned off for 7ms. By pulsing the LED its efficiency is improved and the drive circuitry is simplified.

The 16 columns are controlled by two 74HC273 latches (U37and U38). If a bit is set to high, then the corresponding column is active. The columns are driven by two UDN2981A high-current source drivers (U29 and U30) and the current set by the 100R 1W resistors. The outputs of the source drivers are either VLED (+12V) if they are driven or floating if they are off.

The 8 rows are controlled by a 74HC164 shift-register (U19). This register is arranged as a circulating buffer with one bit high (the active row) and the other bits low. Every time an access is made to the column register, the active row is incremented. Two ULN2803A Darlington drivers (U15 and U12) drive the rows in parallel. The outputs of the drivers are either around 1 volt if driven or floating if they are off.

The circuitry has been designed to work optimally if the LED column register is accessed every 1ms. This speed ensures that the blinking of the LED's (125Hz) is faster than the human eye. If a Led were to be driven by this circuitry continuously then it would burnout because the driving currents are greater than the maximum allowable average current through the LED's. To prevent this undesirable event, protection circuitry has been installed to turn off the LED's if the column register is not accessed for 3ms. This protection circuitry consists of a 74HC123 dual monostables (U44 and U50) and a flip-flop (U31B). If a fault condition is detected then U37, U38 and U19 are reset, and the signal START goes high. When the LED register is next accessed, START supplies the initial conditions to drive output QH of U19 high. If the next row to become active will be ROWO then the signal CHECK will be high. This signal is available at ACIA2 (U10), input port signal IP4 (pin 43). The software should check this signal to determine if it agrees with what software expects. If a disagreement is detected, the software should immediately write a 0 to the LED column register and wait 10ms. If the signal CHECK is now high, the LED scanning may resume; otherwise the software should disable LED scanning and inform the user.

25.1.7 Clocks

(refer schematic MFX010-CPU (page 2 of 8))

A 10MHz oscillator (OSC1) supplies the main system clock, PCLK. The 68000 divides this signal by 10 to give the 1MHz E clock (6:4 duty cycle) used by slow synchronous peripherals (displays). The E clock is divided by a flip-flop (U31) to give a 1/2 MHz square wave. The 1/2 MHz clock is used by DUART U7 as the 16 x MIDI clock. A 3.6864MHz clock is generated by DUART U8 for use in generating RS232 baud rates. See the section on the DUARTS for more information.

25.1.8 Watchdog

(refer schematic *MFX010-CPU (page 2 of 8))*

A DS1232 watchdog (U45) is used to supervise the operation of the MFX keyboard. It

drives the open collector /RESET and /HALT signals low whenever the +5V power supply is out of range (4.76V to 5.25V), if the optional reset button has been pressed (connector J11), or if, the watchdog has not been accessed by the 68000 for 100ms. The 68000 requires both /RESET and /HALT to cause it to reset. If the 68000 does a double buss fault (e.g. loading an odd address pointer during an exception vector fetch) then it will drive /HALT low. If the 68000 executes a reset instruction, then it will drive /RESET only low. Both /RESET and /HALT also drive low-current red LED's (LD6 and LD8). If both LED's light simultaneously, then it is likely that the watchdog is driving these lines. However if the /HALT LED lights marginally before the /RESET LED then it is likely that the 68000 has had a double buss fault. This would occur if the ROM's were corrupt or if there was a serious problem with the address or data buss. If the green LED (LD7) remains lit, then the 68000 is executing code and keeping the watchdog at bay. If the green and red LED's light alternately, then the 68000 is not executing correct code.

25.1.9 Displays

(refer schematic MFX010-DISPLAY (page 6 of 8))

The MFX keyboard supports the attachment of two LM402B01 displays. These displays each offer 40 columns by 2 rows with up to 8 custom characters. The display is backlit by yellow LED's, which shine through the characters (clear characters on a black background). The data buss, address buss and R/W are buffered (74HCT245 at U36 and elsewhere) before driving the display signal cables (J8 and J9). The backlight is driven from 12V, as very little other use is made of the negative supply capacity of the MFX. A contrast adjustment pot is accessible from the top right hand corner of the MFX keyboard. Before concluding that a display is faulty because nothing is visible, you should check the contrast adjustment.

25.1.10 DUARTs

(refer schematic MFX010-DUARTS & DRIVERS (page 4&5 of 8))

The MFX supports serial communications with the following devices:

1. MIDI to MIDI D on the MFX
2. MIDI from MIDI D on the MFX
3. Midi from the Fairlight music keyboard
4. RS422 to and from a LYNX synchroniser or other synchroniser supporting the ES Bus
5. RS232 to and from an MFX expansion device
6. RS232 to the MFX keyboard input
7. RS232 from printer port 2 on the MFX (this port is no longer an external connector)
8. RS232 from the music keyboard
9. RS232 to and from a mouse

Four 68C681 DUARTs (U7, U8, U9 and U10) support these communication channels.

U8 drives a 3.6864Mhz crystal, which when buffered by a 74HC240 (U6H) is supplied to the other DUARTs. This clock is divided by the 68C681s to give the RS232 baud rates. A 1/2MHz

clock is used as the MIDI 16 times clocks.

The 68C681 DUART has two transmit channels, and two receive channels. All channels have independent baud rates. An internal, 16-bit counter can be programmed in a variety of ways to act as a timer, counter or frequency generator. An 8-bit output port is provided, with some of the bits being able to provide status information. A 6 bit input port can be read directly, or programmed to generate interrupts on either or both edges of a signal.

The 68C681 implements the full 68000 interrupt vectoring scheme, by providing the contents of an interrupt vector register to the 68OOO during the interrupt acknowledge cycle.

25.1.11 AC1A1

(refer schematic MFX010-DUARTS (page 4 of 8))

AClA1 (U7) handles MIDI communications. MIDI to and from the MFX (port D) is handled by the “A” side, whilst MIDI from the music keyboard is received by side “B”. The 1/2MHz clock is supplied to input pins IP2 to IP5, and the software configures these inputs to be the 16 times clock inputs. This DUART can generate level 5 interrupts, enabling quick response to MIDI data.

25.1.12 ACIA2

(refer schematic MFX010-DRIVERS (page 5 of 8))

AClA2 (U10) handles RS422 communications at 38k4 baud to Lynx synchronisers, or other synchronisers supporting the ES-buss. The Lynx Synchroniser generates a square Wave synchronised to the field edges of a video signal (SYSC on pin3 of U10), which can be programmed to cause an interrupt in the MFX. It also handles the RS232 bi-directional channel available on the MFX expansion port. This DUART can generate level 4 interrupts.

25.1.13 ACIA3

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA3 (U8) handles RS232 communication to and from the MFX. Side “A” transmit drives the alphanumeric keyboard input signal on the MFX. The RS232 keyboard output from the MFX appears at the receive input, side “B”. This DUART can generate level 2 interrupts.

25.1.14 ACIA4

(refer schematic MFX010-DUARTS (page 4 of 8))

ACIA4 (U9) handles RS232 communications to and from a mouse using side “A”. This mouse should be a serial mouse with a DB9 connector for attachment to the serial port of an IBM PC-AT. There are numerous software protocols possible. Side “B” is unused, This DUART can generate level 2 interrupts.

Interface drivers

(refer schematic MFX010-DRIVERS (page 5 of 8))

MIDI is received using PC900 opto-couplers (U1, U2). This circuit is the circuit

recommended by the MIDI specifications. The MlDI transmitter is a BC549 transistor (Q7), which makes this circuit more rugged than the usual 7407 open-collector transmitter circuit. The tape synchroniser is interfaced using a DS8921 RS422 transmit receiver pair (U3), The driver has a source impedance of 110ohm and a low-pass filter. The receiver has termination impedance of 110ohm at high frequency, increasing to high impedance at DC. Pull-up resistors cause the +ve input to see a higher voltage than the -ve input if the inputs are not being driven. RS232 is driven by a 14C88-driver (U4), with all outputs filtered and output impedance's of 110 ohm. The voltage swing is +11V to -11V typically. A 14C89-receiver (U5) has termination impedances of 120 ohm at high frequency, increasing to high-impedance at DC.

25.1.15 Speaker

(refer schematic MFX010-DRIVERS (page 5 of 8))

Five of the output pins of AClA2 (U10) are used to produce tones through the speaker of the MFX. Each output is connected to a different resistor and summed at a common node. The signal is then AC-coupled and low-pass filtered before reaching the non-inverting input of a power op-amp (U14). By turning a pot accessible from the top right hand corner of the MFX, the gain of the op-amp may be varied. The op-amp directly drives an 8ohm speaker. Each output can produce an independent tone, with a volume level that depends upon the Output Used. The Signal SL1 produced by OP3 (pin 15 of ACIA2 (U10)) can be programmed to be a free running square-wave derived from the internal counter. The other four outputs require that the processor toggle each bit directly.

25.1.16 Key scanning

(refer schematic MFX010.004 and 009)

The switches are arranged into banks, with each bank containing 8 switches. The bank address is written to the output register of ACIA1 (U7), and the state of the 8 switches can then be read from the 74HC244 buffer (U11). A 1 in a switches bit position indicates that the switch is open (up), whilst a 0 indicates that the switch is closed (depressed). The bank address consists of a 4-bit diode network number, and a 4-bit circuit board selection number.

7		unused (future expansion)
6		unused (future expansion)
5	ENPANEL	0 panel key (MFK panel keys) enabled 1 panel key disabled
4	ENQWERTY	0- qwerty key (MFK qwerty keys) enabled 1= qwerty key disabled
3	SWI3	number of the active
2	SWI2	diode-network on
1	SWI1	each circuit board
0	SWI0	(MFX030 and MFX040)

Fig 1. Switch bank address register (output port of U7)

25.1.17 Jogger wheel

(refer schematic MFX010-DRIVERS (page 5 of 8))

The MFX supports the decoding of an optical shaft encoder. The quadrature output of the encoder is pulled up and low-pass filtered before being buffered by a 74HC132-schmitt-trigger (U18). The outputs of the Schmidt trigger are fed to ACIA2 (U10), input port bits IPO and lP1. The DUART can be configured to cause an interrupt on the edge of the quadrature signal.

25.1.18 MFK Qwerty board.

(Refer schematic MFK)

The MFK board supports and decodes the QWERTY keyboard, the function keys and the panel trigger keys. It receives power from MFX010 through a 10-way Molex connector, and communicates with, MFX010 through a 50-way lDC connector. The panel trigger keys and all other switches are scanned by the 68000 processor.

25.1.19 Qwerty, Panel trigger switches and function keys.

(refer schematic MFK-MFX console key panel)

The QWERTY, function and panel keys are decoded using a diode matrix, with an active row/column scheme. This allows infinite key roll-over to be implemented. The diodes are contained in 25 common cathode diode networks (DN1 through DN25).

25.1.20 Qwerty

(refer schematic MFK-qwerty keys 1 to 4)

The QWERTY keys are arranged into 4 banks (qwerty1, qwerty2, qwerty3, and qwerty4). The address of the active QWERTY key is set up by the 12-bit code SWQ0 through SWQ12. SWQ0-3 selects qwerty1, SWQ4-7 selects qwerty2, SWQ8-11 selects qwerty3, and SWQ12 selects qwerty4.

The anodes of the QWERTY diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U3 and U4). If the signal ENQWERTY is low, then the signals SWI0 through SWI3 set which of the 12 (plus 4 unused) outputs SWQ0 through SWQ15 will be low.

25.1.21Panel

(refer schematic MFK-panel keys 1 to 4)

The PANEL keys are arranged into 4 banks (panel1, panel2, panel3, and panel4). The address of the active PANEL key is set up by the 14-bit code SWP0 through SWP13. SWP0-3 selects panel1, SWP4-7 selects panel2, SWP8-11 selects panel3, and SWP12-13 selects panel4.

The anodes of the PANEL diode networks are connected to the outputs of two 74HC138 8-channel multiplexors (U2 and U1). If the signal ENPANEL is low, then the signals SWI0 through SWI3 set which of the 14 (plus 2 unused) outputs SWP0 through SWP15 will be low.

The signals SWOO0 through SWO7 are pulled up to +5V by resistors on MFX010. Thus only one diode network will have its cathode near GND, allowing its diodes to conduct if the attached switches are closed.

25.2 MFX CONSOLE DIAGNOSTICS

1. To reset the non-volatile RAM in the MFX console switch OFF power and hold down numeric keypad keys 1:2:3. Switch on power while keys are depressed. Go to the shell from MFX project screen by typing “SHIFT” $ <ret>. At the # type “mfxload” ret>. The system will load the non-volatile RAM. When operation is complete depress “ESC” key.

2. To enter diagnostics on the MFX console hold down numeric keypad keys 4:5:6. Switch on power while keys are depressed. Release keys when you are ready to enter diagnostics. Depress Fl:F3:F5:F7 to exit test.

TEST NUMBER	TEST DESCRIPTION
0	LCD, 68000 RAM, LED circuits
1	Raw Keyboard Test
2	ASCII keyboard Test, depress ‘keys and Check LCD display
3	Jogger and mouse X axis / Y axis
4	N/A
5	N/A
6	NIA
7	Speaker level test. Adjustment on top right corner of console
8	RS422 / N/A
9	Return MFX console to MFX operation

To set LCD contrast, adjust preset on top right corner of console.

3. Depressing keys -:+:BLUE will set console for software up load. This does not reset the non-volatile RAM as in point 1.

CABG8529 - MFX Plus Cable Assembly

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	5/8/96	L.Stewart	RELEASE		
1.1	16/1/97	L.Stewart	Cable spec and connections		
1.2	7/12/98	N.Plummer	Rotated drawing to match connection drawing. Corrected title name.		

NOTE :

1. Cable to be to the following specification;
   12 Pair + Drain Twisted Pair
   7/0.02mm Stranded Cores
   RS422 Hi Speed Data (50pF/m)
   Low Impedance & Braided Screen
   e.g. MCP-12S/BS (supplier A.G.Garland)
2. Refer to Dwg # CABC8529.DW2 for connections
3. Refer to supplied documentation for additional information regarding termination of cable screens
4. Ferrites to be FairRite P/N 2643626402 Fairlight P/N FERB0110)
5. Cover ferrites with heatshrink

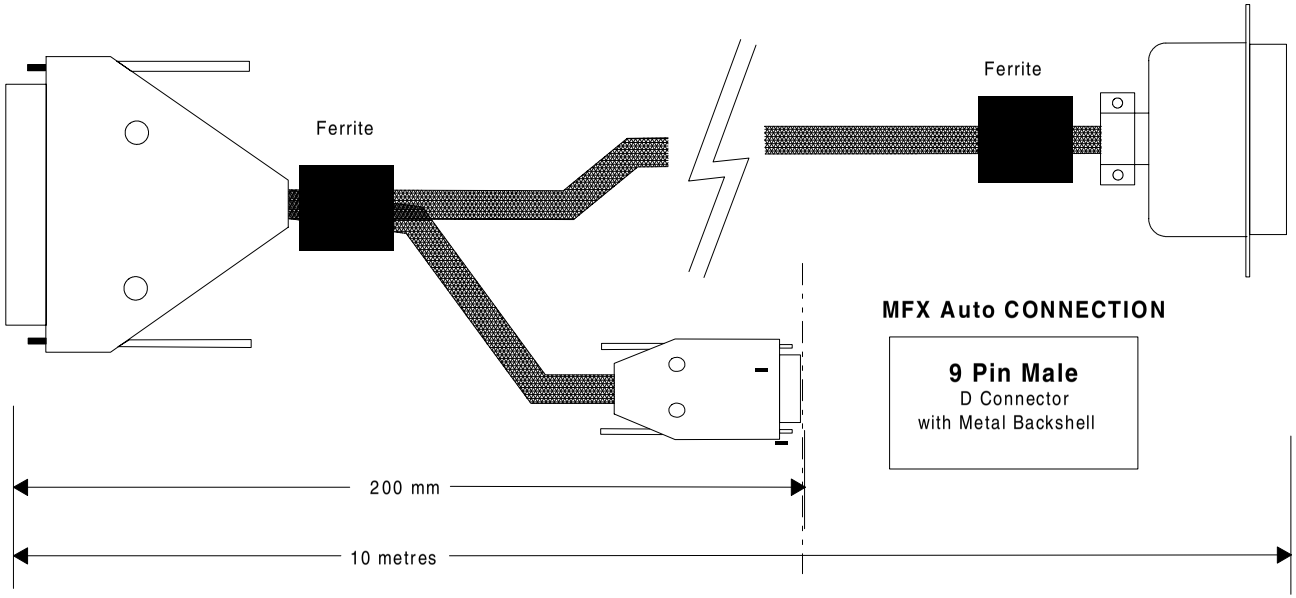
See also related connection drawing
Cabg8529 MFXP 1 of 2 Connect rev 1-3.dc

MAINFRAME CONNECTION

24 Pin Male
Centronics Connector
with Metal Backshell

CONSOLE CONNECTION

37 Pin Male
D Connector
with Metal Backshell



MFX Auto CONNECTION

9 Pin Male
D Connector
with Metal Backshell

DIMENSION UNITS: mm	DESIGNED BY ENGINEERING L.Stewart	TITLE CABG8529 - MFX Plus Cable Assembly	REV. 1.2
TOLERENCE: ± 3%	APPROVED BY ENGINEERING	FILE NAME: Cabg8529 MFXP 1 of 2 Assy rev 1-2.dc	
FILE NAME: CABG8529.DW2	APPROVED BY PRODUCTION	SCALE N.T.S. / SHEET 1 OF 1	COMPANY CONFIDENTIAL
	APPROVED BY QUALITY CONTROL		

CABG8529 - MFX Plus Cable Connection Diagram

REV.	DATE	DESIGNED BY	DESCRIPTION	PCO	ZONE
1.0	16/12/96	L.Stewart	RELEASE		
1.1	16/1/96	L.Stewart	Cable Spec & Connections		
1.2	27/8/98	M.Paolino	Signal names corrected (Midin / out)		
1.3	7/12/98	N.Plummer	Previous change reversed. Signal names changed to PCB name at each end. Corrected part number in title.		

NOTES :

** Assumes this signal when appropriate jumper is in place

1. Cable is to be to the following specification;
   14 Pair + Drain Twisted Pair
   7/0.02 Stranded cores
   RS422 HI SPEED Data (50pF/m)
   LOW IMPEDANCE
   Braided screen
   e.g. MCP-12S/BS (Supplier: A.G. Garland)

See also related assembly drawing
Cabg8529 MFXP 2 of 2 Assy rev 1-2.dc

Console Connection

37 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to J2 on MFX010)

Signal Name (MFX010 PCB)	Connector Pin No.	Colour	Mandatory	Connector Pin No.	Signal Name (ESP-MIDI PCB)	
FS+	13	Brown	Yes	5	X422+	Pair
FS-	31	Brown/White	Yes	17	X422-	
TS+	12	Grey	Yes	6	R422+	Pair
TS-	30	Grey/White	Yes	18	R422-	
MO1+	8	Green		10	Mid+	Pair
MO1-	26	Green/White		22	Mid-	
MI1+	9	Blue		9	MOut+	Pair
MI1-	27	Blue/White		21	MOut-	
MI2+	11	Orange		7	n/c	Pair
MI2-	29	Orange/White		19	n/c	
RSI1	6	Brown	Yes	12	Data2	Pair
Gnd	21	Brown/Black	Yes	14	Gnd **	
RSI2	7	Grey		11	Data1 **	Pair
Gnd	20	Grey/Black	Yes	13	Gnd **	
RSO2 **	25	Green		23	KEYBDOUT**	Pair
n/c	16	Green/Black		15	n/c	
Gnd	10	Green	Yes	8	*MFXPresent	Pair
SYSC	28	Green/Yellow		20	n/c	
RSO1	24	Orange	Yes	24	Datain	Pair
Gnd	23	Orange/Black	Yes	16	Gnd **	
n/c	2	Grey		2	n/c	Pair
n/c	4	Grey/Red		3	n/c	
Gnd	1	Green	Yes	1	Gnd **	Pair
n/c	14	Green/Red		4	n/c	
MRXD	36	(any)	Yes	2	(MRXD)	
MTXD	37	(any)	Yes	3	(MTXD)	
Gnd	33	(any)	Yes	5	Gnd	

Mainframe Connection

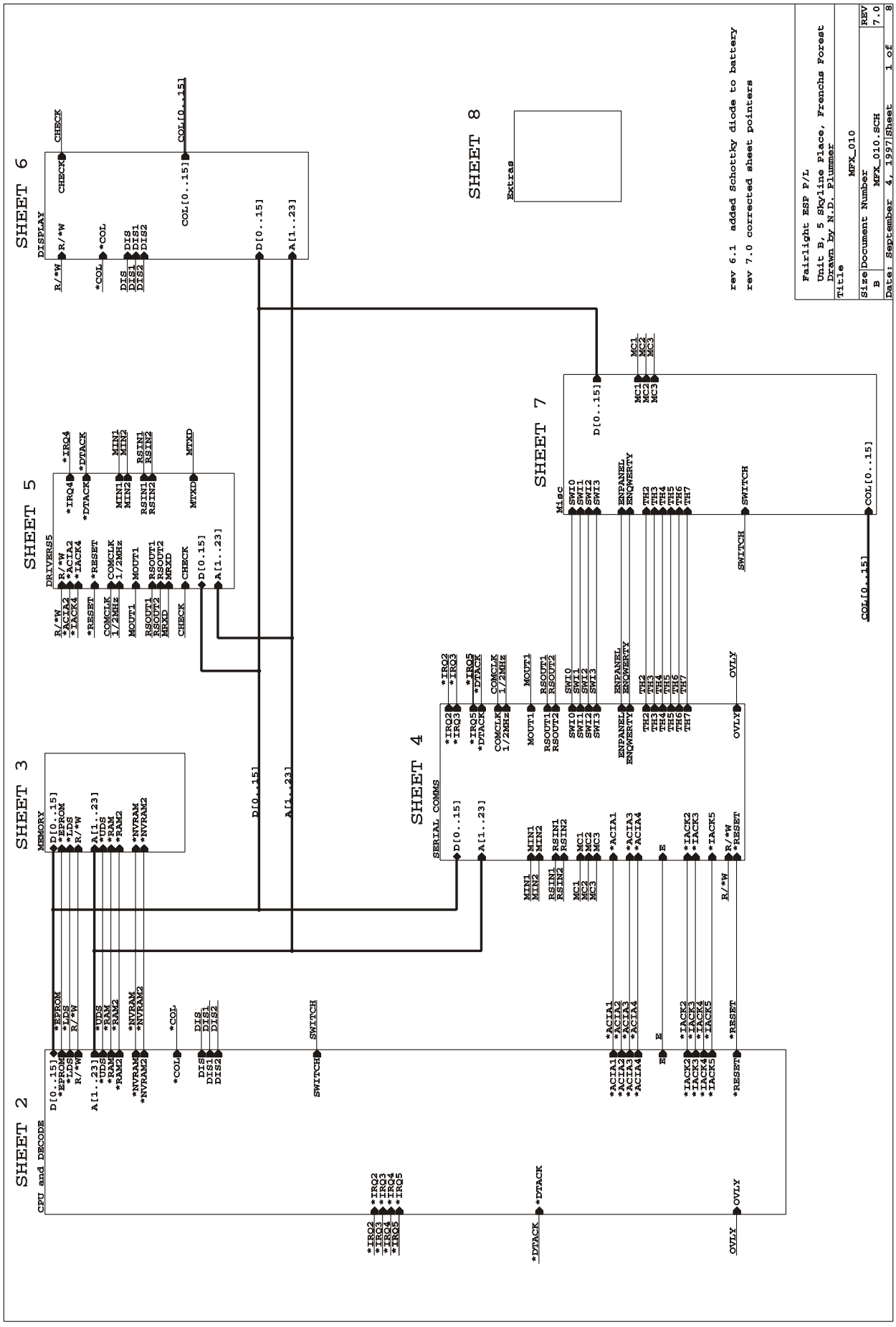
24 Pin Male
Centronics Connector
with Metal Backshell
UL Recognised
(Connects to P5 on ESP-MIDI)

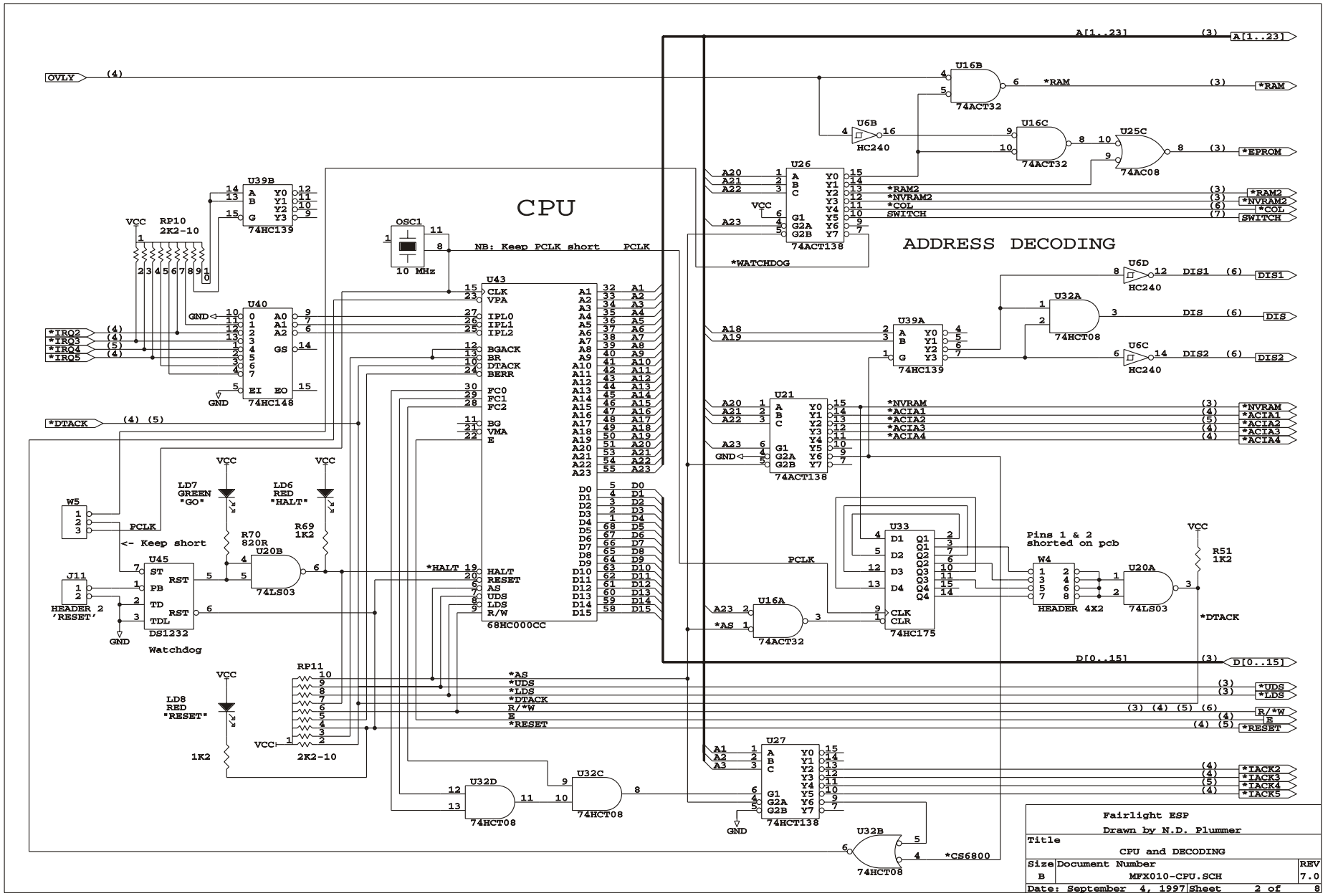
MFX Auto Connection

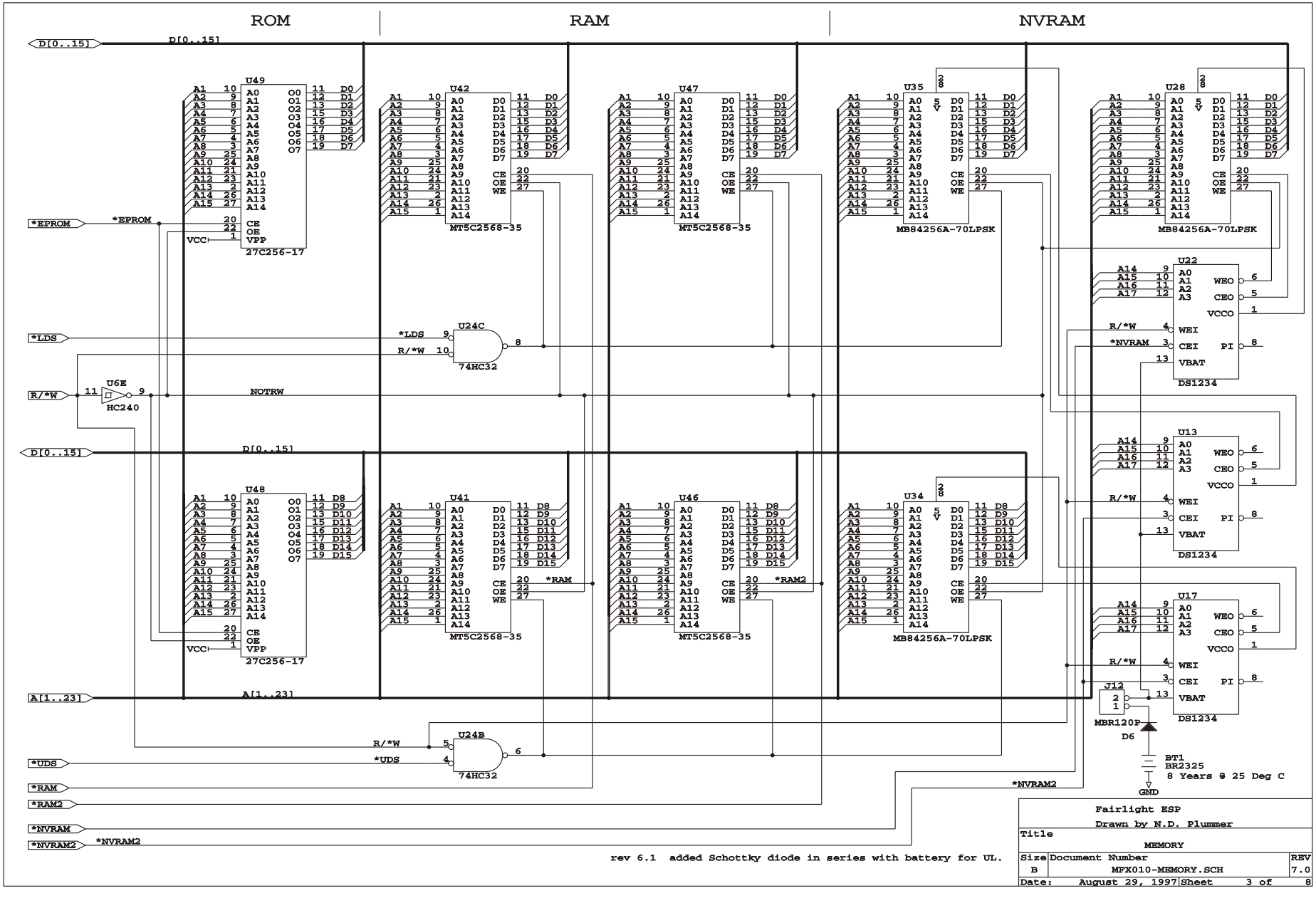
9 Pin Male
D Connector
with Metal Backshell
UL Recognised
(Connects to Serial Port on PC)

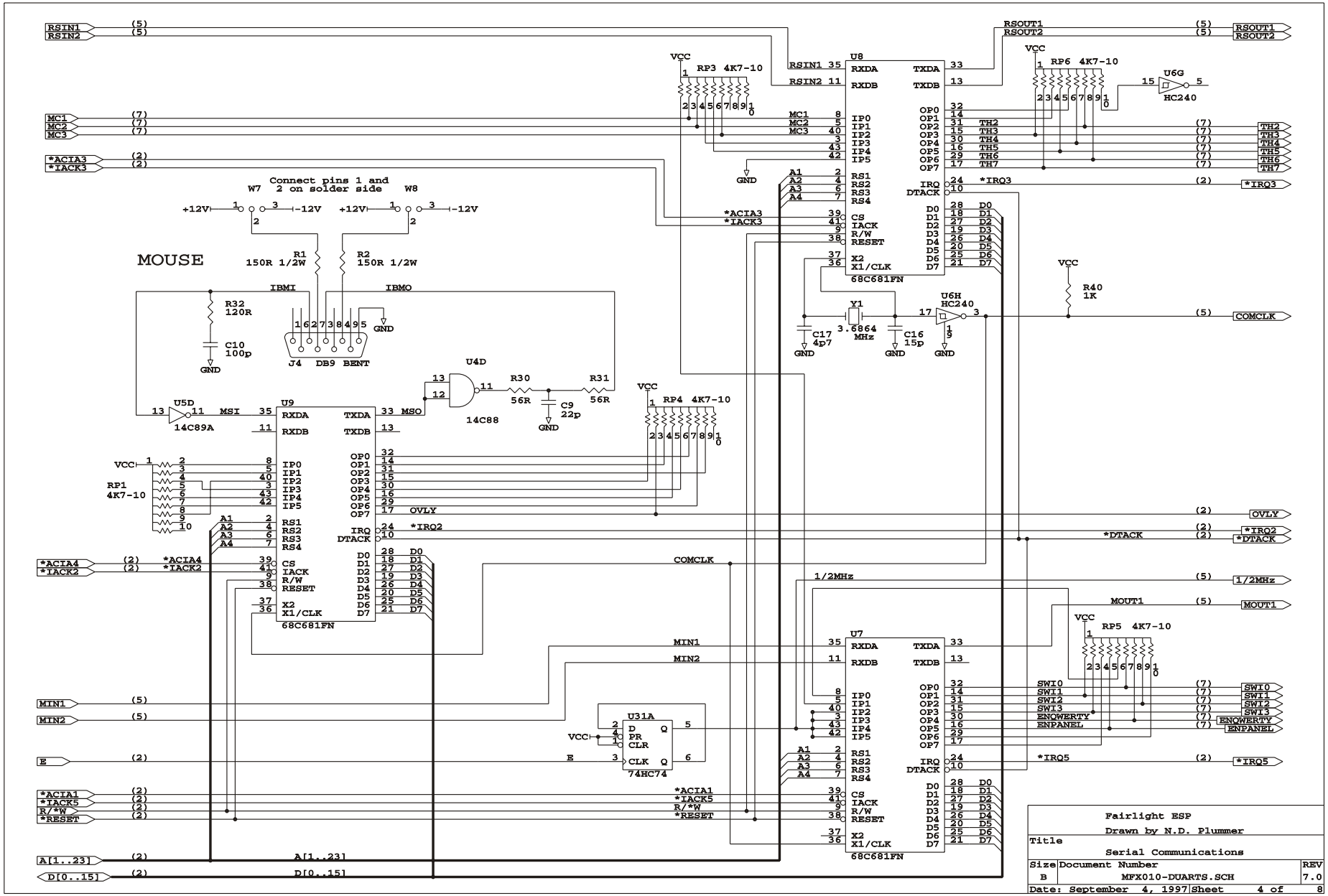
DIMENSION UNITS: mm	DESIGNED BY ENGINEERING: L.Stewart	TITLE: CABG8529 - MFXP Cable Connection Diagram	REV. 1.3
TOLERENCE: ± 3%	APPROVED BY ENGINEERING	FILE NAME: Cabg8529 MFXP 2 of 2 Connect rev 1-3.dc	
FILE NAME: CABC8529.DW2	APPROVED BY PRODUCTION	SCALE N.T.S. / SHEET 1 OF 1	COMPANY CONFIDENTIAL
	APPROVED BY QUALITY CONTROL		

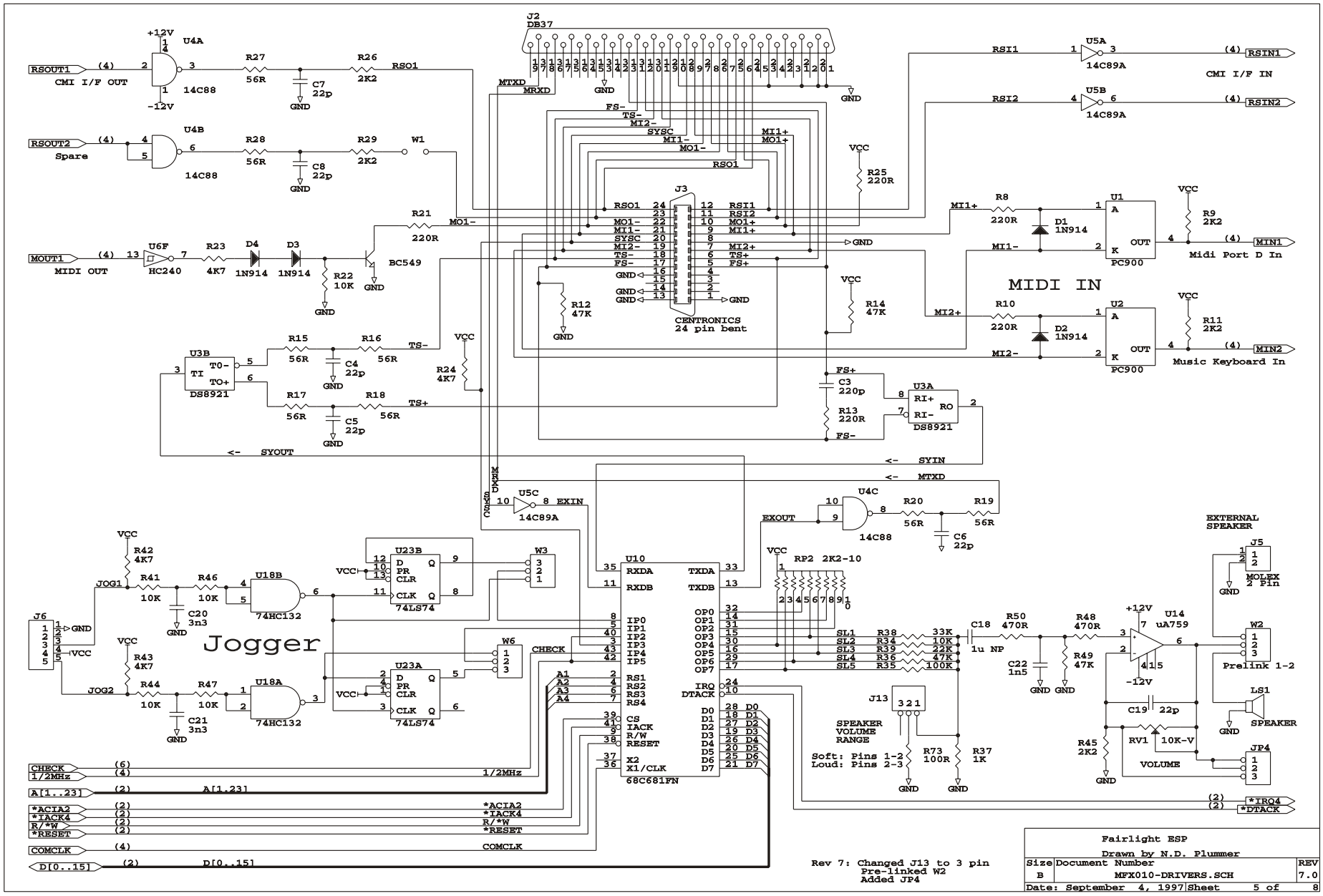
25.4 MFX010 Controller Card Schematics

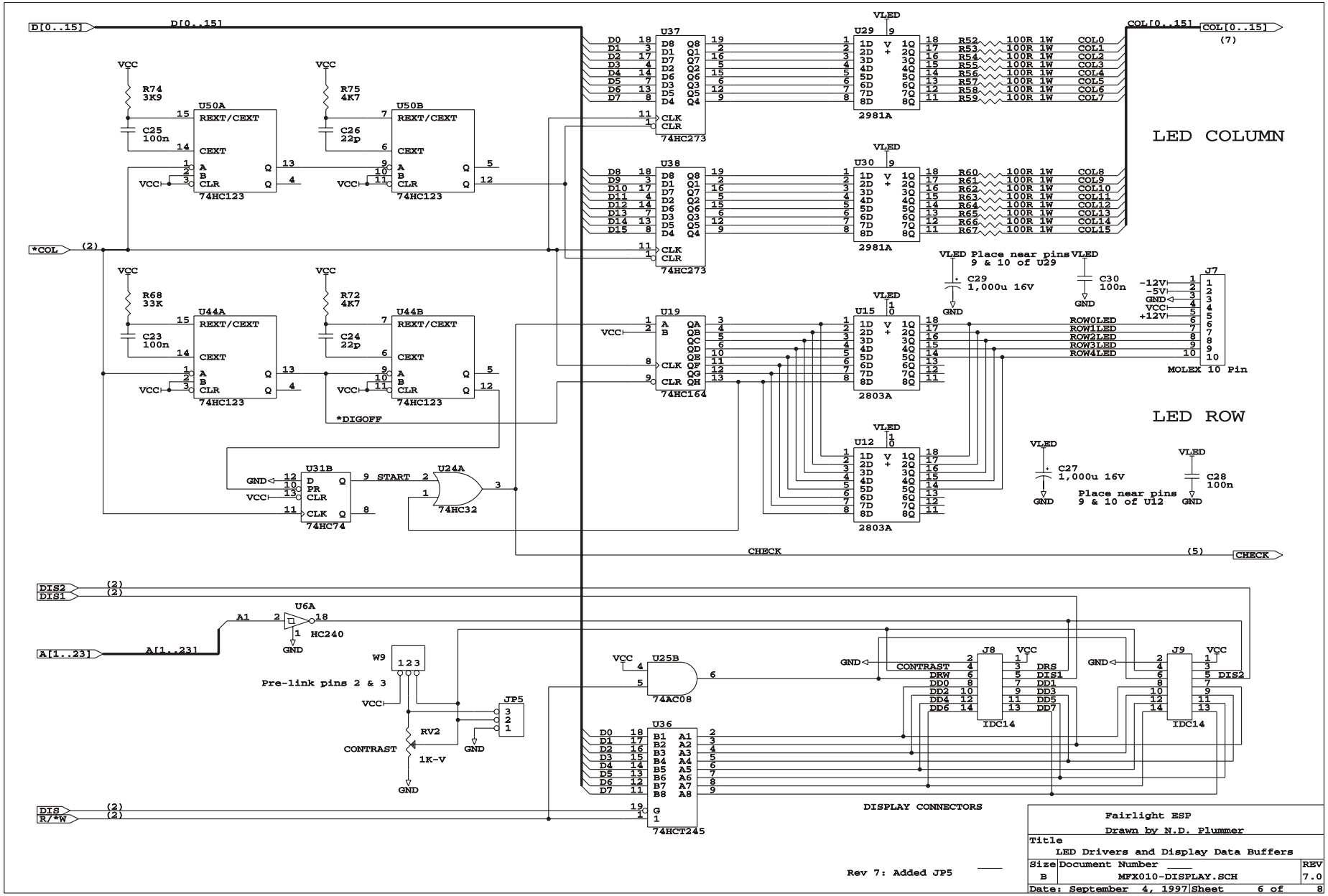


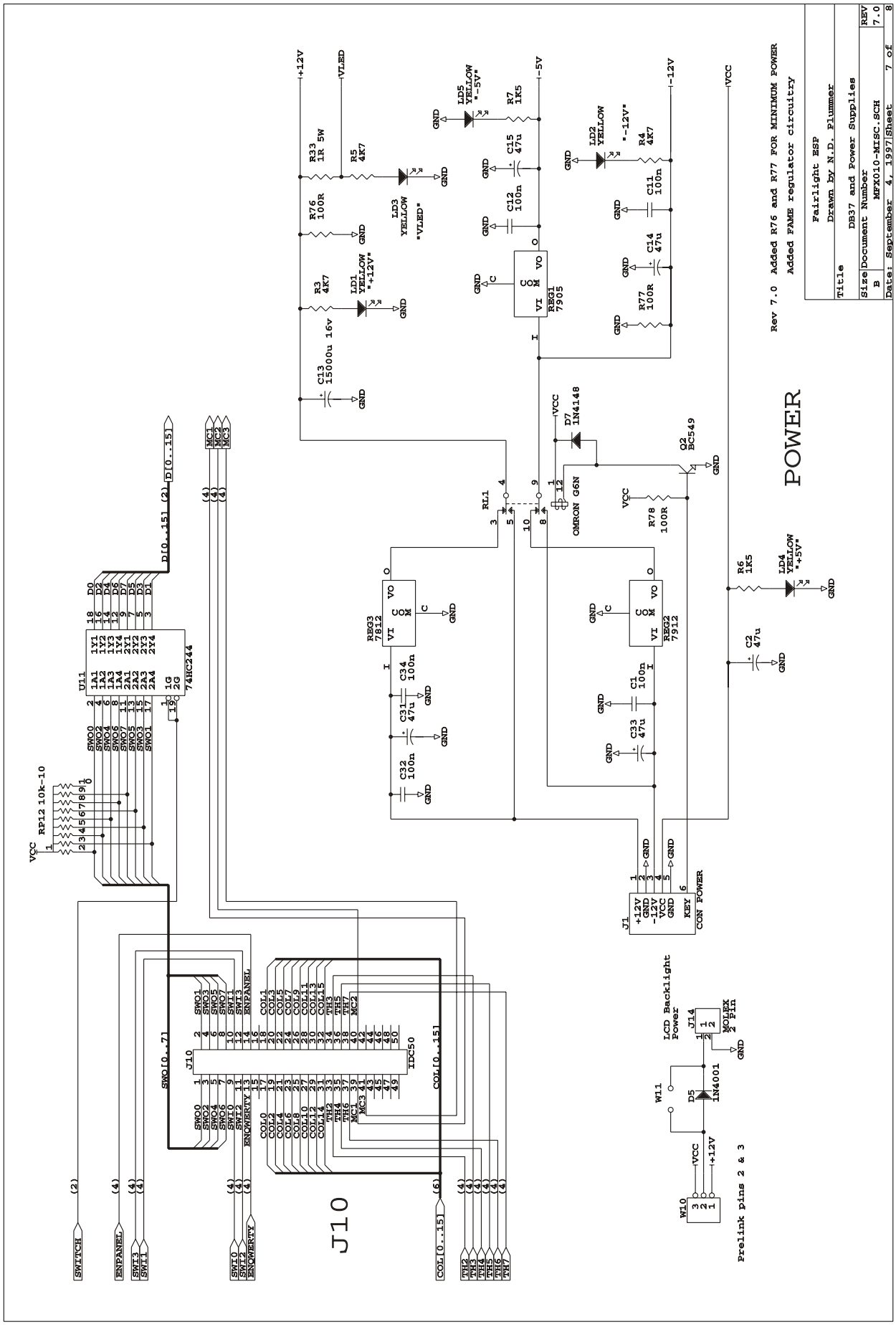

CPU
ADDRESS DECODING
NB: Keep PCLK short
<- Keep short
Pins 1 & 2
shorted on pcb
Watchdog
Fairlight ESP
Drawn by N.D. Plummer
Title
CPU and DECODING
Size B
Document Number MFX010-CPU.SCH
REV 7.0
Date: September 4, 1997 Sheet 2 of 8

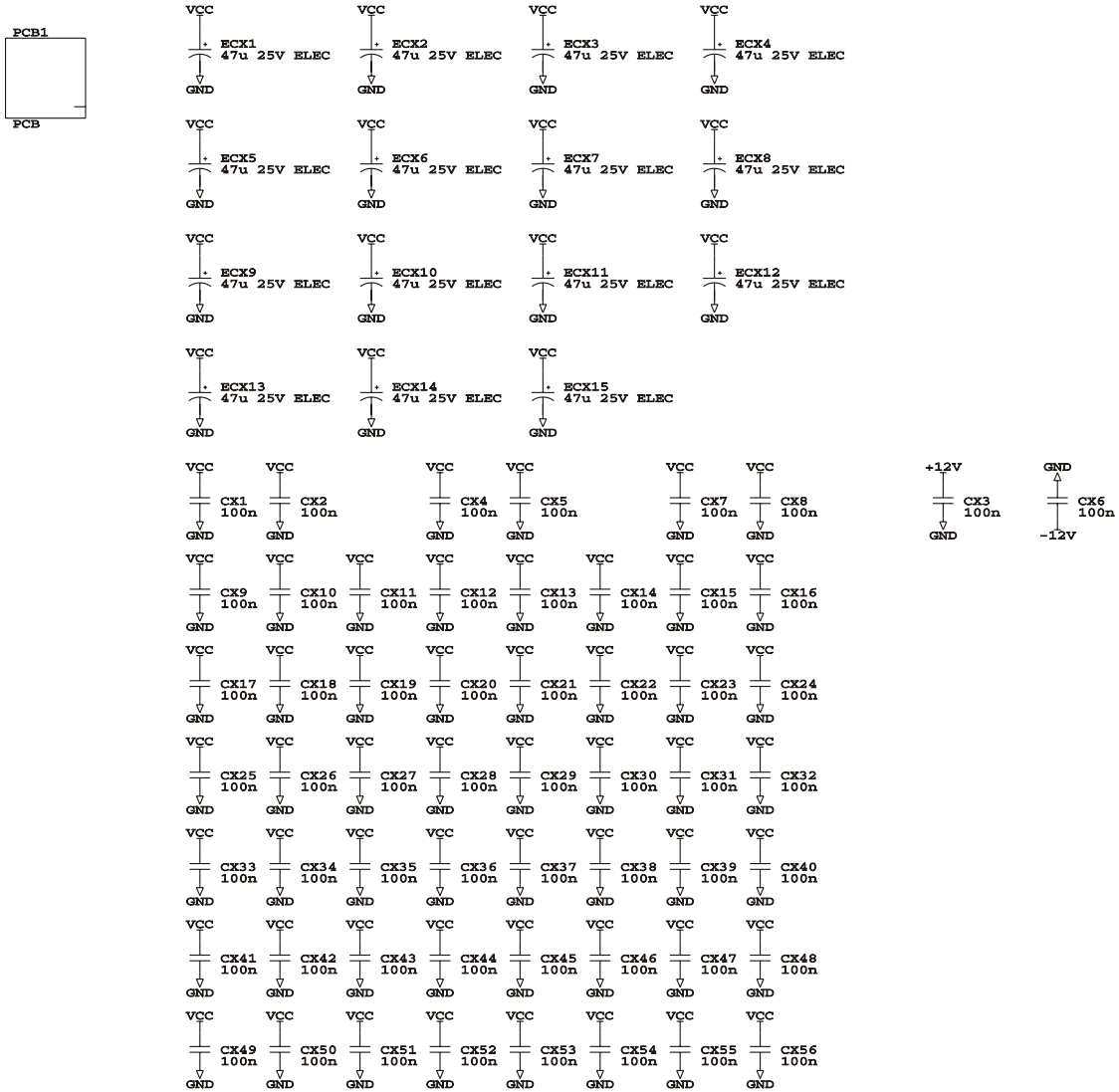

ROM
RAM
NVRAM
D[0..15]
U49
27C256-17
U42
MT5C2568-35
U47
MT5C2568-35
U35
MB84256A-70LPSK
U28
MB84256A-70LPSK
*EPROM
*LDS
R/*W
U6E
HC240
NOTRW
U24C
74HC32
U22
DS1234
U13
DS1234
U17
DS1234
U48
27C256-17
U41
MT5C2568-35
U46
MT5C2568-35
U34
MB84256A-70LPSK
A[1..23]
U24B
74HC32
*UDS
*RAM
*RAM2
*NVRAM
*NVRAM2
J12
MBR120P
D6
BT1
BR2325
8 Years @ 25 Deg C
GND
rev 6.1 added Schottky diode in series with battery for UL.
Fairlight ESP
Drawn by N.D. Plummer
Title
MEMORY
Size B
Document Number MFX010-MEMORY.SCH
REV 7.0
Date: August 29, 1997
Sheet 3 of 8


RSIN1
RSIN2
MC1
MC2
MC3
*ACIA3
*IACK3
MOUSE
Connect pins 1 and 2 on solder side
W7
W8
+12V
-12V
R1 150R 1/2W
R2 150R 1/2W
IBMI
IBMO
R32 120R
C10 100p
J4 DB9 BENT
U4D
14C88
R30 56R
R31 56R
C9 22p
U5D
14C89A
MSI
MSO
U9
68C681FN
RP1 4K7-10
RP3 4K7-10
RP4 4K7-10
U8
RSOUT1
RSOUT2
RP6 4K7-10
U6G
HC240
TH2
TH3
TH4
TH5
TH6
TH7
*IRQ3
R40 1K
Y1
3.6864 MHz
U6H
C17 4p7
C16 15p
COMCLK
OVLY
*IRQ2
*DTACK
*ACIA4
*IACK2
1/2MHz
MOUT1
RP5 4K7-10
MIN1
MIN2
U31A
74HC74
SWI0
SWI1
SWI2
SWI3
ENQWERTY
ENPANEL
*IRQ5
*ACIA1
*IACK5
R/*W
*RESET
A[1..23]
D[0..15]
Fairlight ESP
Drawn by N.D. Plummer
Title
Serial Communications
Size
Document Number
MFX010-DUARTS.SCH
REV
7.0
Date: September 4, 1997
Sheet 4 of 8

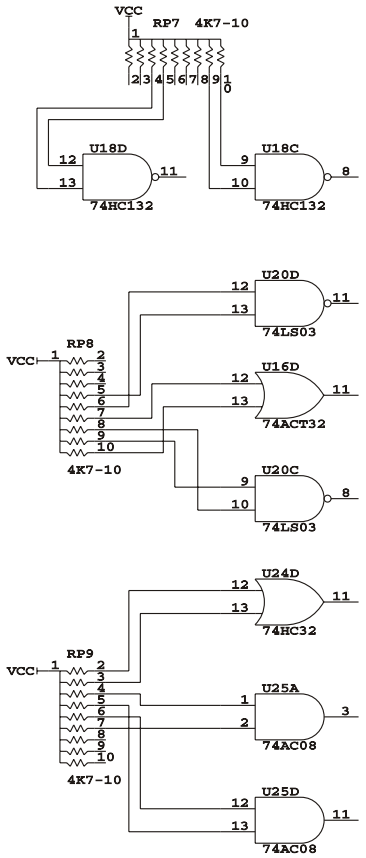

Jogger
MIDI IN
CMI I/F OUT
CMI I/F IN
Spare
MIDI OUT
Midi Port D In
Music Keyboard In
CENTRONICS
24 pin bent
SPEAKER
VOLUME
RANGE
Soft: Pins 1-2
Loud: Pins 2-3
EXTERNAL
SPEAKER
Prelink 1-2
VOLUME
Fairlight ESP
Drawn by N.D. Plummer
Size B
Document Number MFX010-DRIVERS.SCH
REV 7.0
Date: September 4, 1997
Sheet 5 of 8
Rev 7: Changed J13 to 3 pin
Pre-linked W2
Added JP4


LED COLUMN
LED ROW
DISPLAY CONNECTORS
MOLEX 10 Pin
74HC123
74HC273
2981A
74HC164
2803A
74HC74
74HC32
74AC08
74HCT245
HC240
IDC14
Pre-link pins 2 & 3
VLED Place near pins 9 & 10 of U29
Place near pins 9 & 10 of U12
C29 1,000u 16V
C30 100n
C27 1,000u 16V
C28 100n
R74 3K9
R75 4K7
R68 33K
R72 4K7
C25 100n
C26 22p
C23 100n
C24 22p
RV2
1K-V
CONTRAST
*COL
*DIGOFF
START
CHECK
DIS
R/*W
Fairlight ESP
Drawn by N.D. Plummer
Title
LED Drivers and Display Data Buffers
Size B
Document Number MFX010-DISPLAY.SCH
REV 7.0
Date: September 4, 1997
Sheet 6 of 8
Rev 7: Added JP5


POWER
J10
Rev 7.0 Added R76 and R77 FOR MINIMUM POWER
Added FAMS regulator circuitry
Fairlight ESP
Drawn by N.D. Plummer
DB37 and Power Supplies
MPX010-MISC.SCH
Prelink pins 2 & 3
LCD Backlight Power
CON POWER
74HC244
IDC50
REG1 7905
REG2 7912
REG3 7812
OMRON G6N
1N4001
1N4148
BC549
SWITCH
ENPANEL
SWI3
SWI1
SWI0
SWI2
ENQWERTY
COL[0..15]
SWO[0..7]
D[0..15]
VCC
GND
+12V
-12V
-5V
VLED

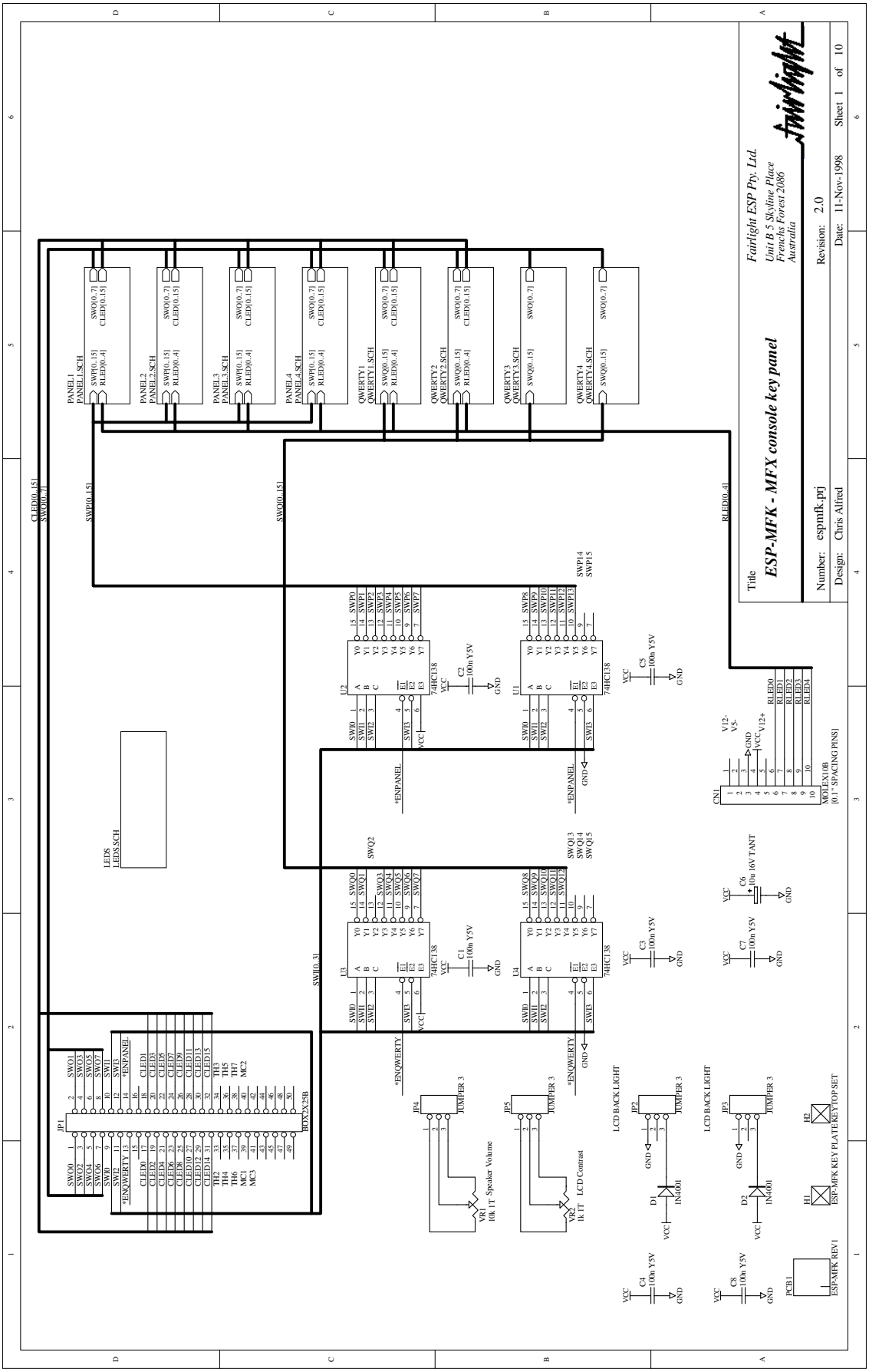


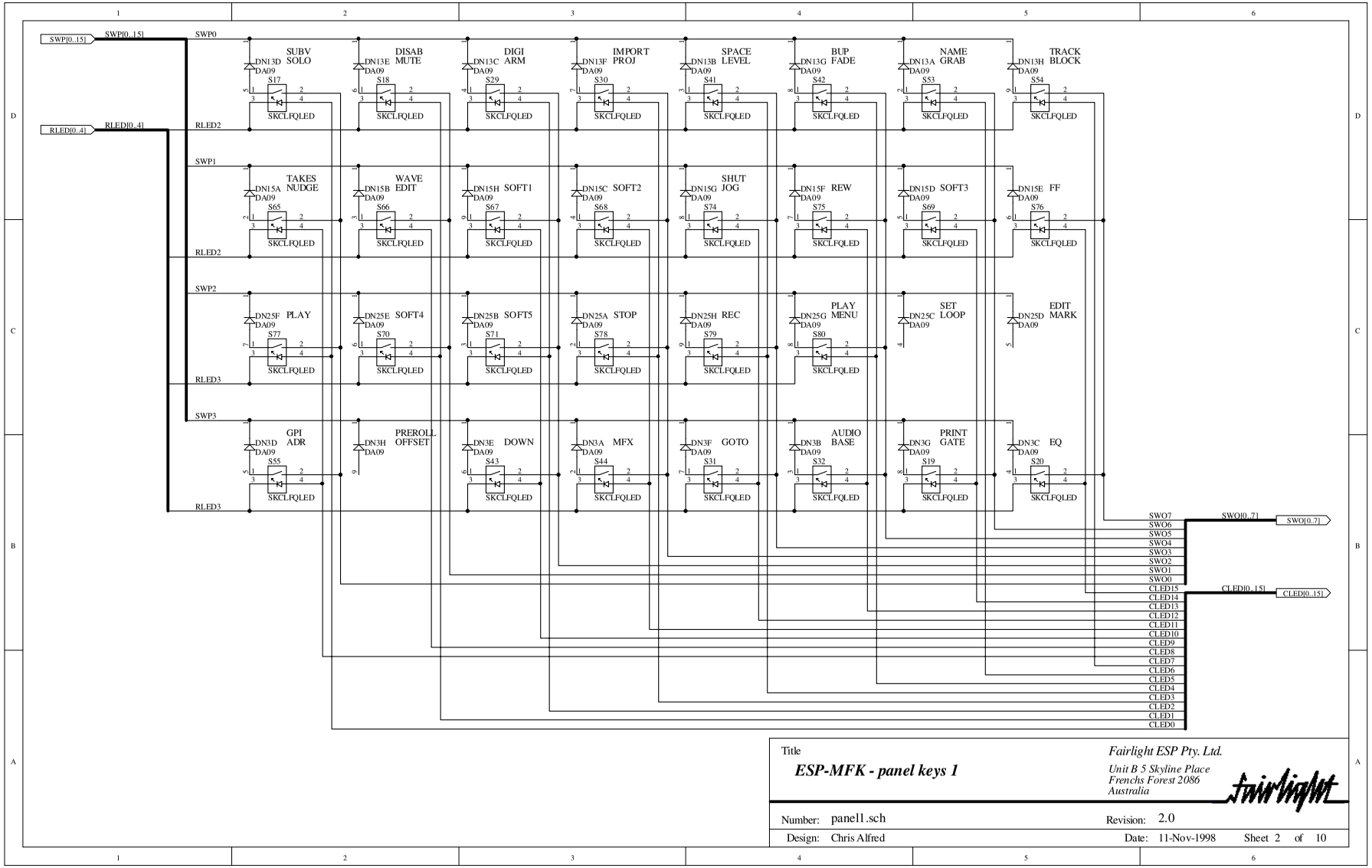
SPARES

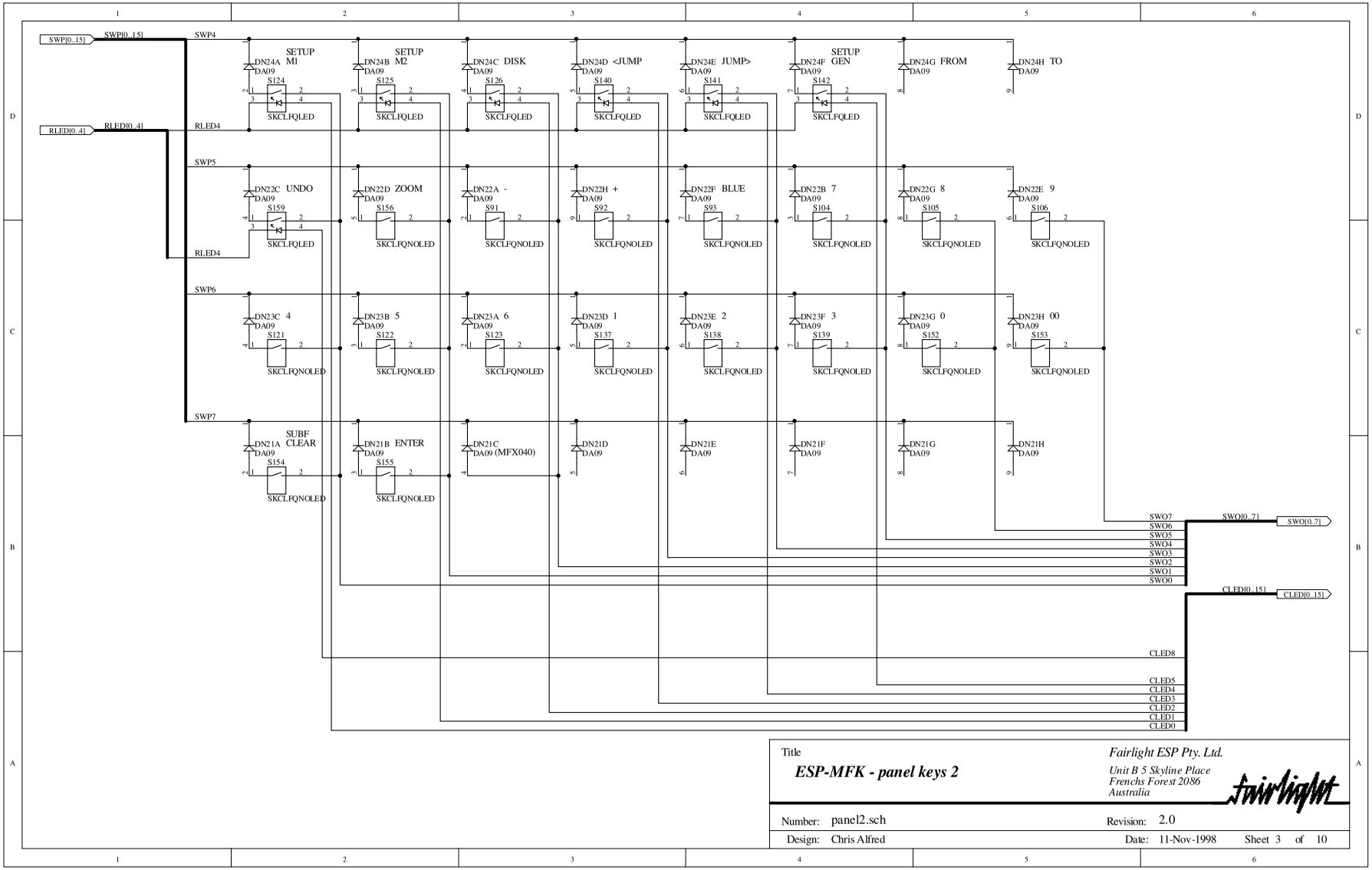


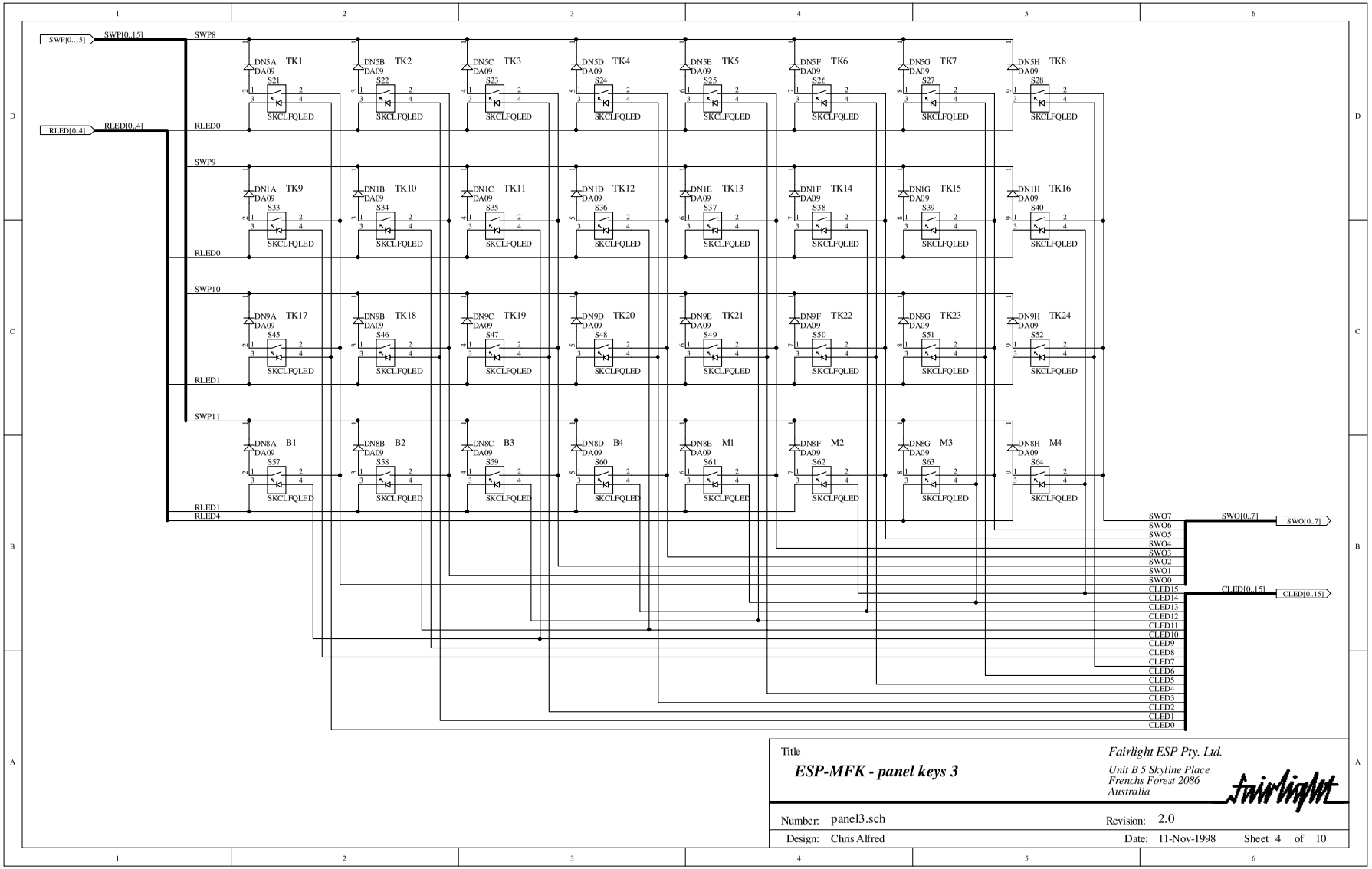
Fairlight ESP		
Title: MFX010 - EXTRAS		
Size: B	Document Number: EXTRAS.SCH	REV: 7.0
Date: August 27, 1997	Sheet 8 of 8	

25.5 MFK Schematics

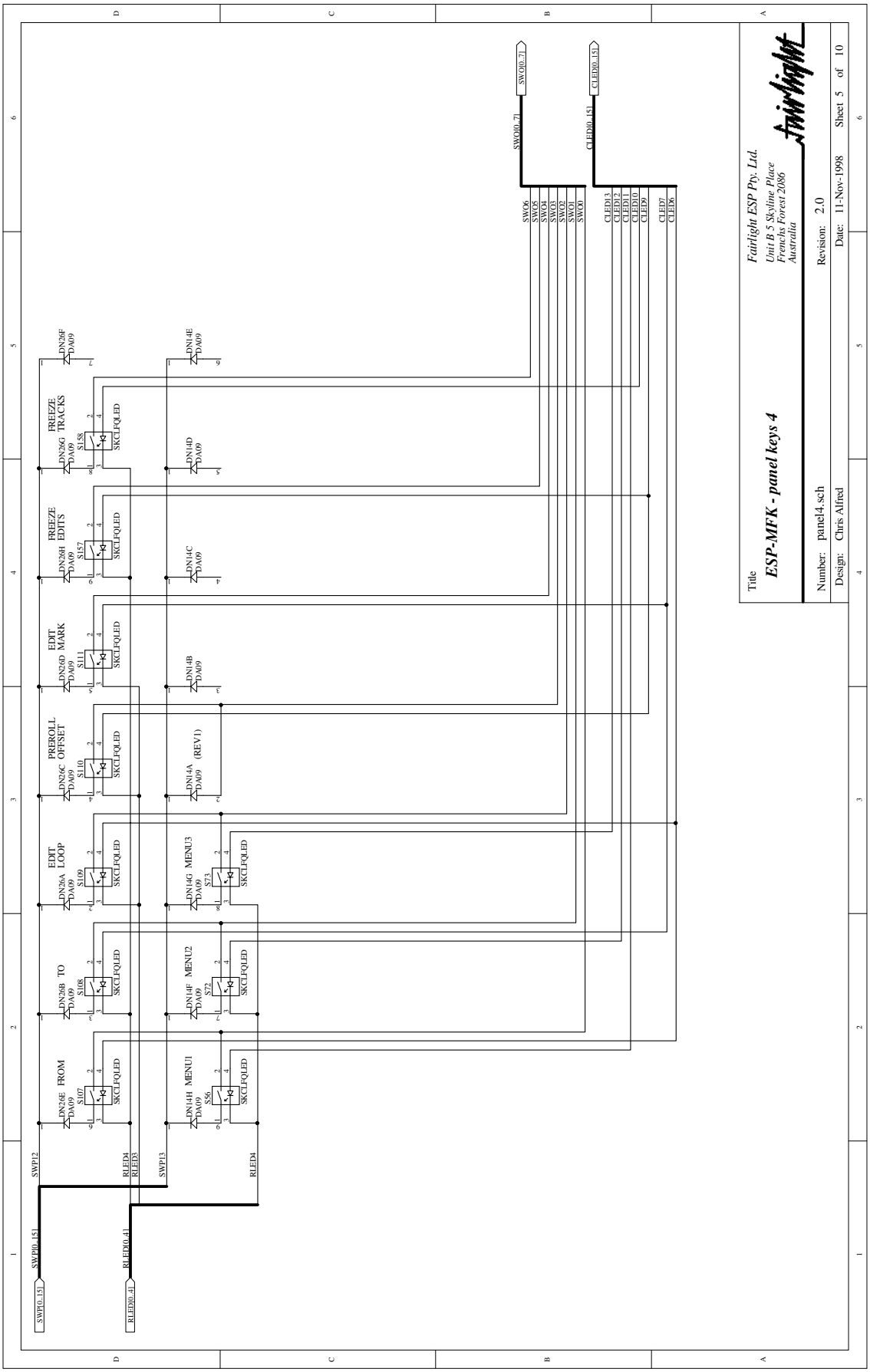


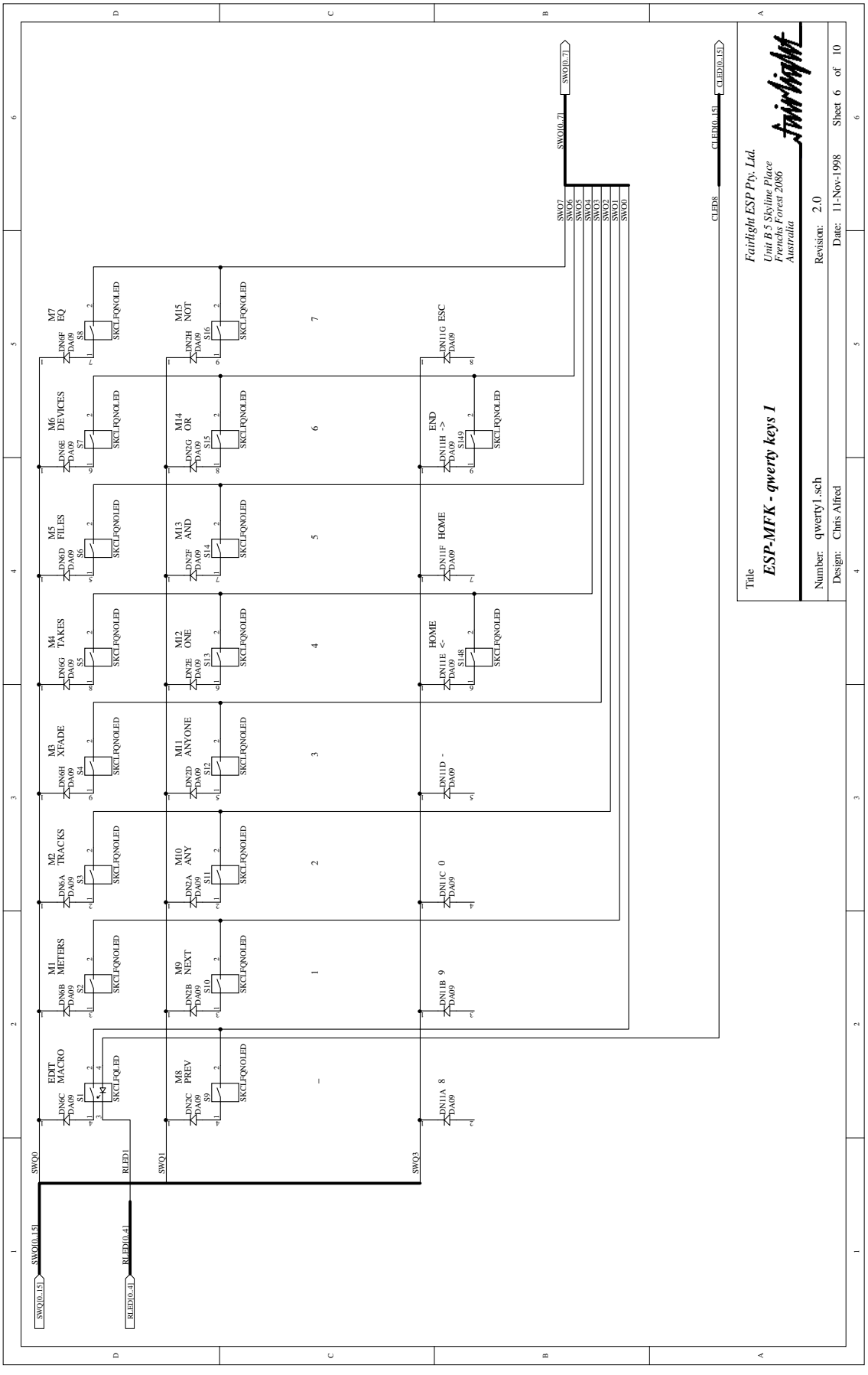

SWP[0..15]
RLED[0..4]
SUBV SOLO
DISAB MUTE
DIGI ARM
IMPORT PROJ
SPACE LEVEL
BUP FADE
NAME GRAB
TRACK BLOCK
TAKES NUDGE
WAVE EDIT
SOFT1
SOFT2
SHUT JOG
REW
SOFT3
FF
PLAY
SOFT4
SOFT5
STOP
REC
PLAY MENU
SET LOOP
EDIT MARK
GPI ADR
PREROLL OFFSET
DOWN
MFX
GOTO
AUDIO BASE
PRINT GATE
EQ
SKCLFQLED
SWO[0..7]
CLED[0..15]
Title
ESP-MFK - panel keys 1
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: panel1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 2 of 10

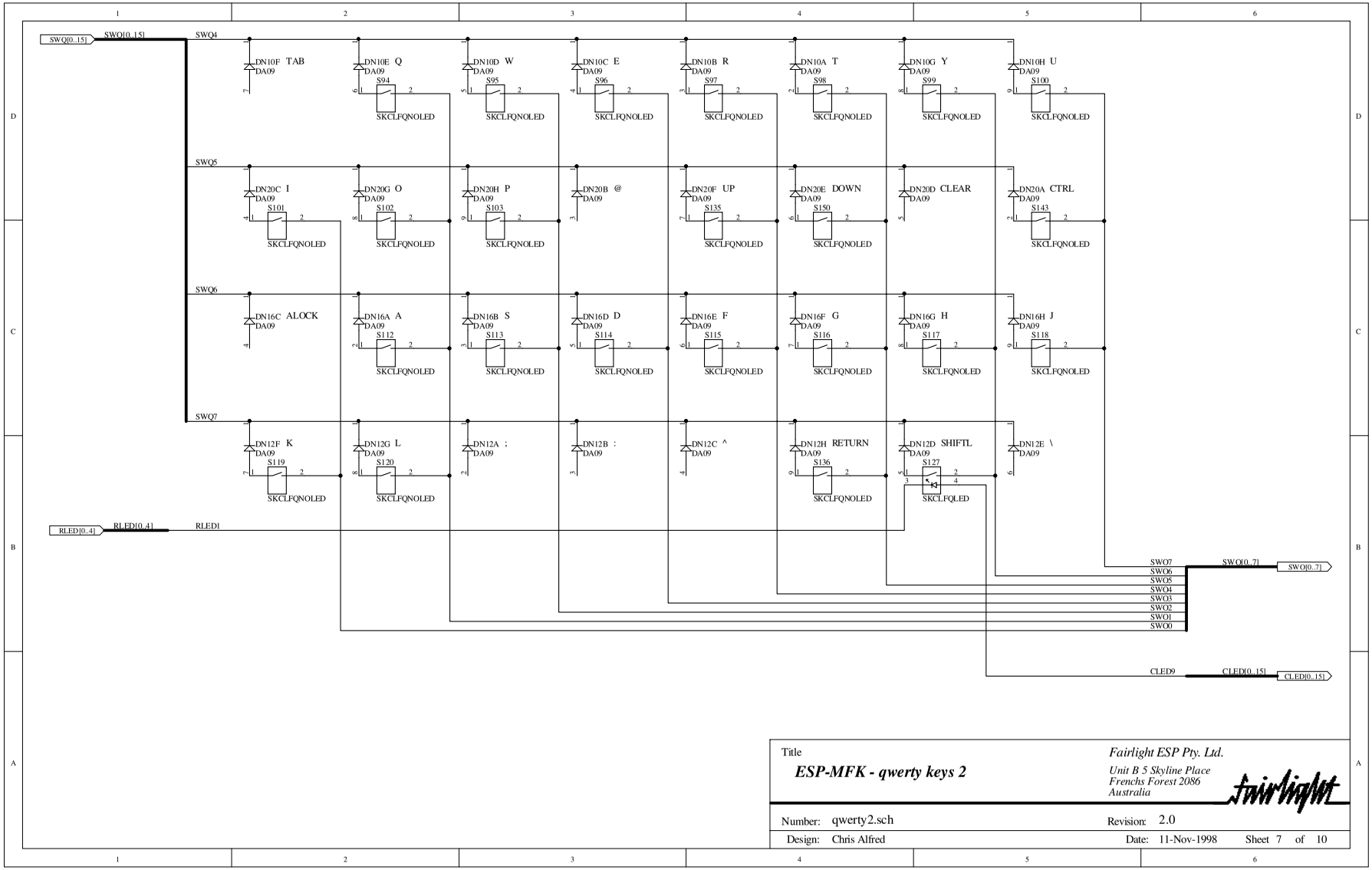

SWP[0..15]
RLED[0..4]
SWP4
RLED4
SWP5
RLED4
SWP6
SWP7
SETUP M1
SETUP M2
DN24C DISK
DN24D <JUMP
DN24E JUMP>
SETUP GEN
DN24G FROM
DN24H TO
DN22C UNDO
DN22D ZOOM
DN22A -
DN22H +
DN22F BLUE
DN22B 7
DN22G 8
DN22E 9
DN23C 4
DN23B 5
DN23A 6
DN23D 1
DN23E 2
DN23F 3
DN23G 0
DN23H 00
SUBF CLEAR
DN21B ENTER
DN21C
DN21D
DN21E
DN21F
DN21G
DN21H
DA09
DA09 (MFX040)
SKCLFQLED
SKCLFQNOLED
SWO7
SWO6
SWO5
SWO4
SWO3
SWO2
SWO1
SWO0
SWO[0..7]
CLED[0..15]
CLED8
CLED5
CLED4
CLED3
CLED2
CLED1
CLED0
Title
ESP-MFK - panel keys 2
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: panel2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 3 of 10

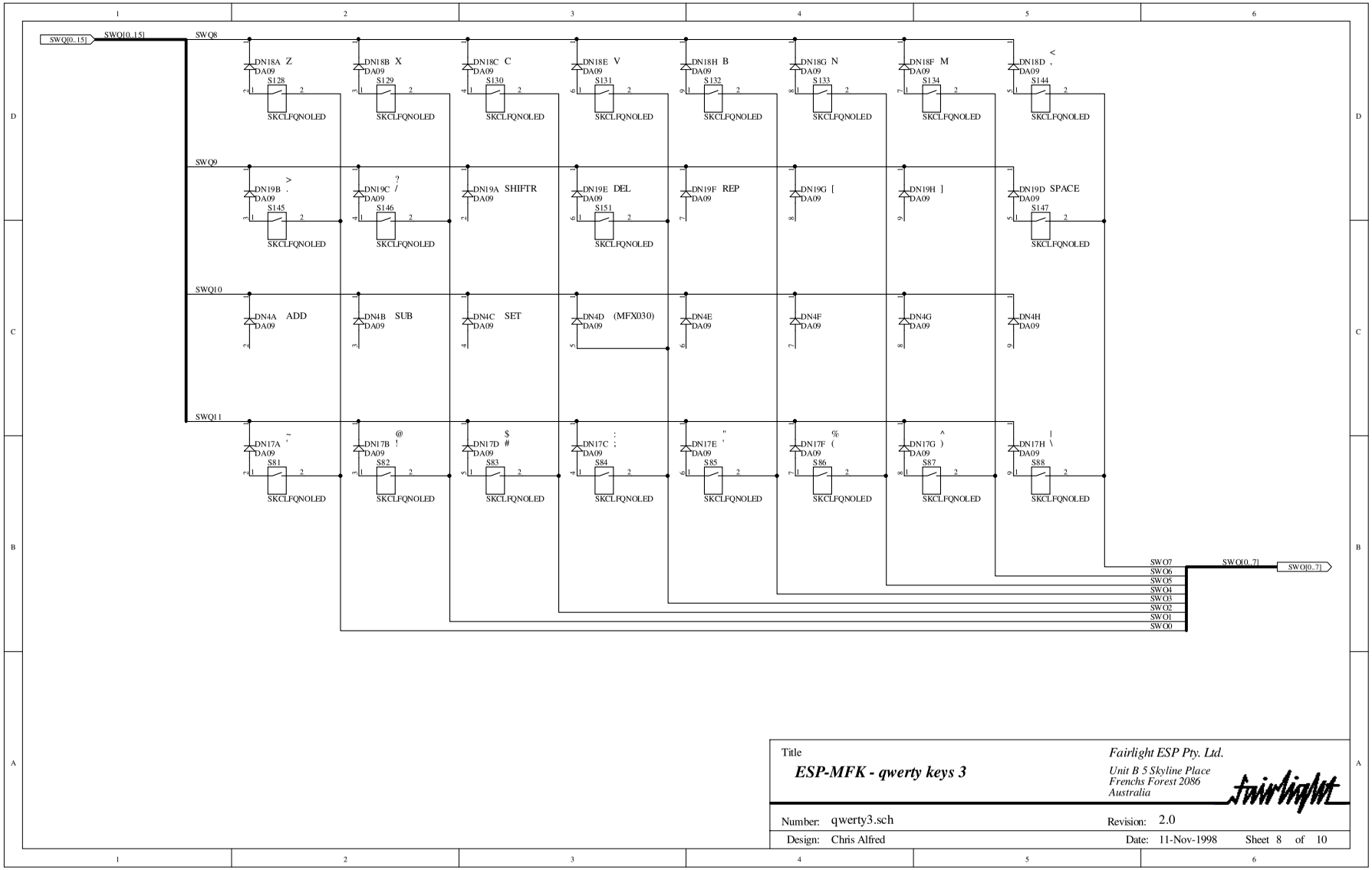


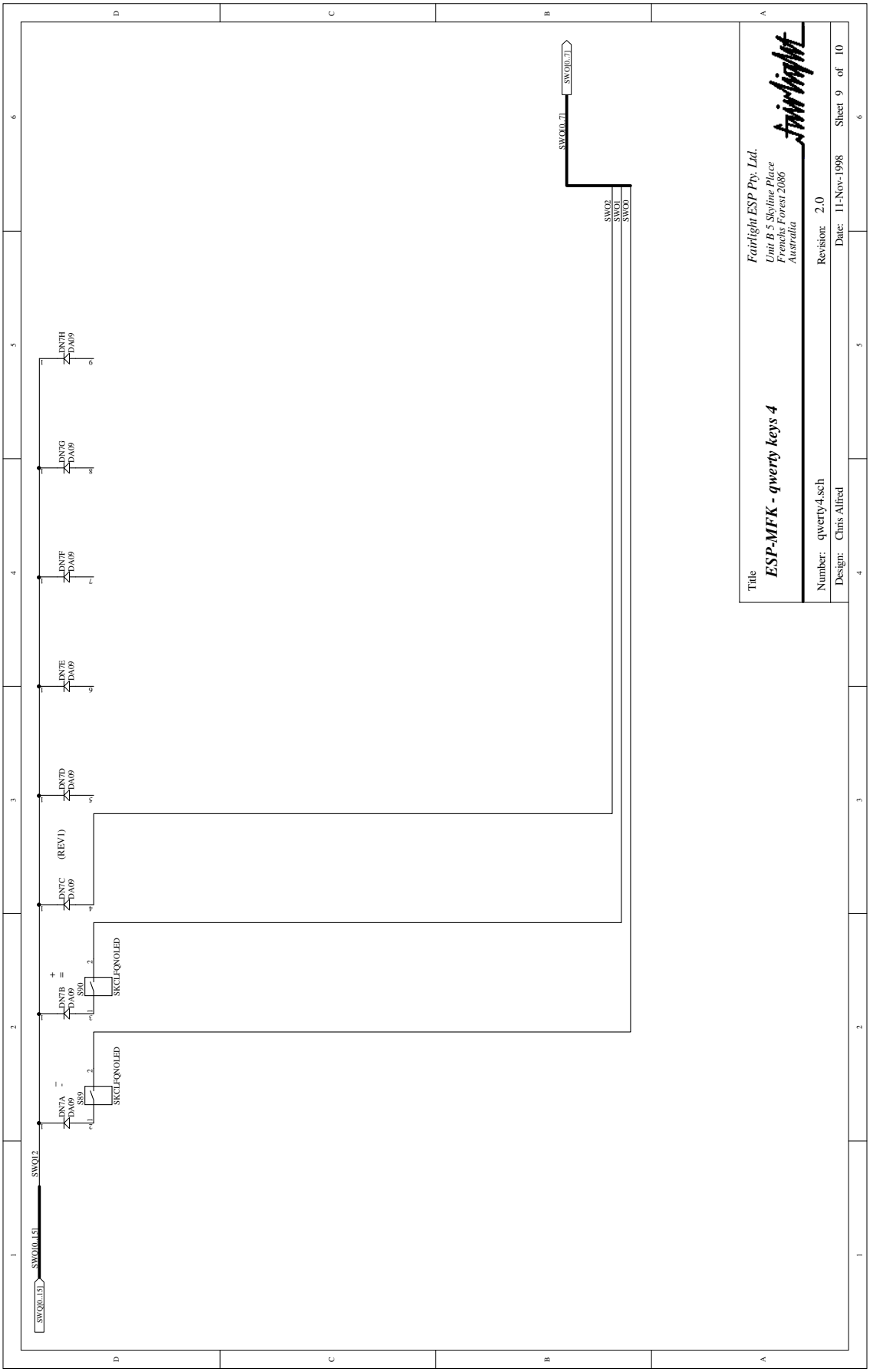
Title	*ESP-MFK - panel keys 3*	*Fairlight ESP Pty. Ltd.*	
		Unit B 5 Skyline Place	
		Frenchs Forest 2086	
		Australia	
Number:	panel3.sch	Revision:	2.0
Design:	Chris Alfred	Date: 11-Nov-1998	Sheet 4 of 10

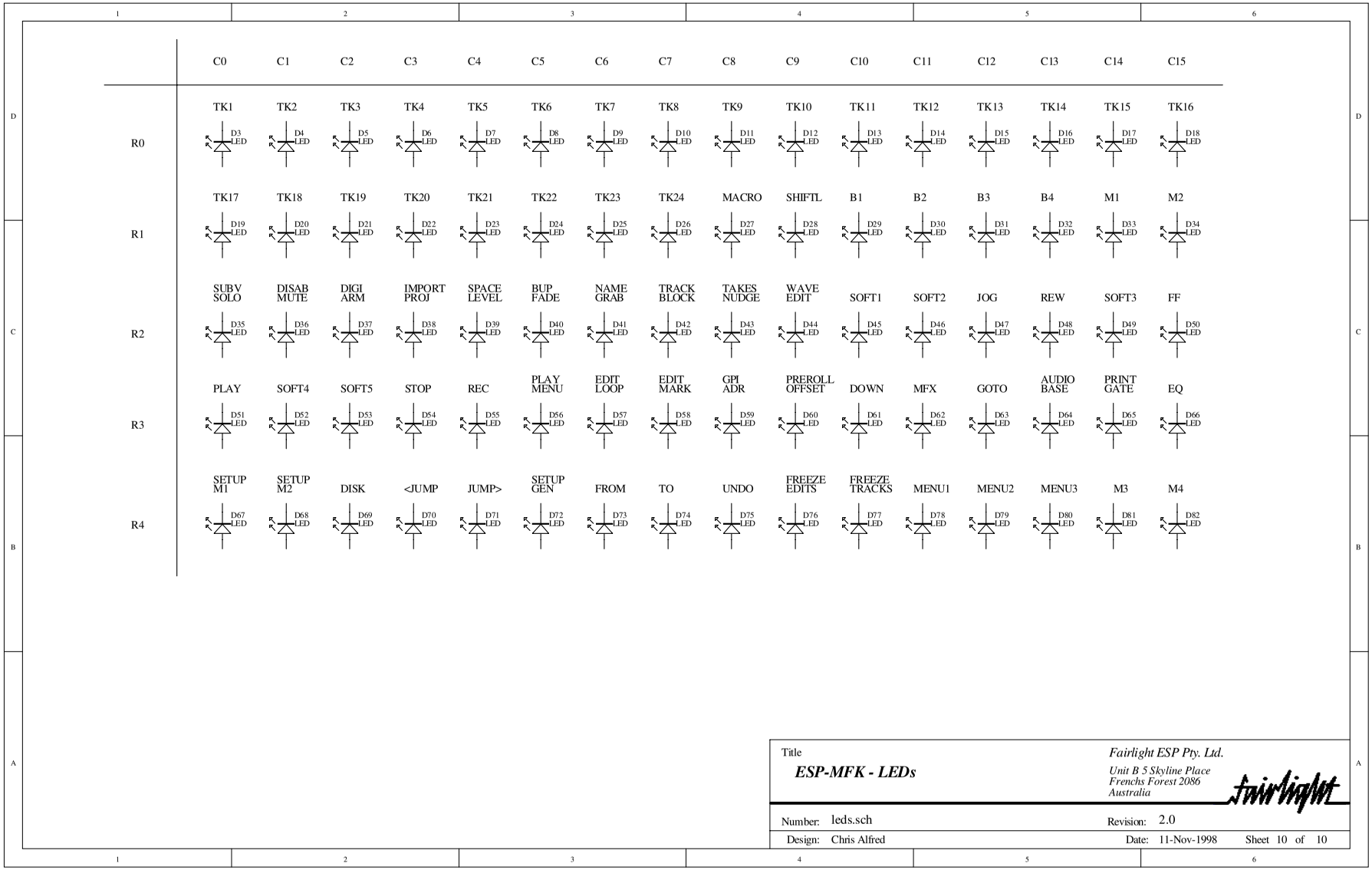

Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Title
ESP-MFK - panel keys 4
Number: panel4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 5 of 10
SWP[0..15]
RLED[0..4]
SW0[0..7]
CLED[0..15]
FROM
TO
EDIT LOOP
PREROLL OFFSET
EDIT MARK
FREEZE EDITS
FREEZE TRACKS
MENU1
MENU2
MENU3
(REV1)
SKCLFQLED


Title
ESP-MFK - qwerty keys 1
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
French's Forest 2086
Australia
Number: qwerty1.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 6 of 10
SWQ[0..15]
RLED[0..4]
CLED[0..15]
SWO[0..7]
EDIT MACRO
M1 METERS
M2 TRACKS
M3 XFADE
M4 TAKES
M5 FILES
M6 DEVICES
M7 EQ
M8 PREV
M9 NEXT
M10 ANY
M11 ANYONE
M12 ONE
M13 AND
M14 OR
M15 NOT
HOME <<
END ->
SKCLFQOLED
SKCLFQNOLED


SWQ[0..15]
SWQ[0..15]
SWQ4
SWQ5
SWQ6
SWQ7
DN10F TAB
DN10E Q
DN10D W
DN10C E
DN10B R
DN10A T
DN10G Y
DN10H U
DN20C I
DN20G O
DN20H P
DN20B @
DN20F UP
DN20E DOWN
DN20D CLEAR
DN20A CTRL
DN16C ALOCK
DN16A A
DN16B S
DN16D D
DN16E F
DN16F G
DN16G H
DN16H J
DN12F K
DN12G L
DN12A ;
DN12B :
DN12C ^
DN12H RETURN
DN12D SHIFTL
DN12E \
DA09
S94
S95
S96
S97
S98
S99
S100
S101
S102
S103
S135
S150
S143
S112
S113
S114
S115
S116
S117
S118
S119
S120
S136
S127
SKCLFQNOLED
SKCLFQLED
RLED[0..4]
RLED[0..4]
RLED1
SWO7
SWO6
SWO5
SWO4
SWO3
SWO2
SWO1
SWO0
SWO[0..7]
SWO[0..7]
CLED9
CLED[0..15]
CLED[0..15]
Title
ESP-MFK - qwerty keys 2
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: qwerty2.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 7 of 10


SWQ[0..15]
SWQ[0..15]
SWQ8
SWQ9
SWQ10
SWQ11
DN18A Z
DN18B X
DN18C C
DN18E V
DN18H B
DN18G N
DN18F M
DN18D <
,
DN19B >
.
DN19C ?
/
DN19A SHIFTR
DN19E DEL
DN19F REP
DN19G [
DN19H]
DN19D SPACE
DN4A ADD
DN4B SUB
DN4C SET
DN4D (MFX030)
DN4E
DN4F
DN4G
DN4H
DN17A ~
`
DN17B @
!
DN17D $
#
DN17C :
;
DN17E "
'
DN17F %
(
DN17G ^
)
DN17H |
\
DA09
S128
S129
S130
S131
S132
S133
S134
S144
S145
S146
S151
S147
S81
S82
S83
S84
S85
S86
S87
S88
SKCLFQNOLED
SWO7
SWO6
SWO5
SWO4
SWO3
SWO2
SWO1
SWO0
SWO[0..7]
SWO[0..7]
Title
ESP-MFK - qwerty keys 3
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: qwerty3.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 8 of 10


SWQ0..15
SWQ0..15
SWQ12
DN7A DA09
S89
SKCLFQNOLED
DN7B DA09
S90
SKCLFQNOLED
DN7C DA09
(REV1)
DN7D DA09
DN7E DA09
DN7F DA09
DN7G DA09
DN7H DA09
SWO0..7
SWO0..7
SWO2
SWO1
SWO0
Title
ESP-MFK - qwerty keys 4
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: qwerty4.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 9 of 10


C0 C1 C2 C3 C4 C5 C6 C7 C8 C9 C10 C11 C12 C13 C14 C15
R0
TK1 TK2 TK3 TK4 TK5 TK6 TK7 TK8 TK9 TK10 TK11 TK12 TK13 TK14 TK15 TK16
D3 LED D4 LED D5 LED D6 LED D7 LED D8 LED D9 LED D10 LED D11 LED D12 LED D13 LED D14 LED D15 LED D16 LED D17 LED D18 LED
R1
TK17 TK18 TK19 TK20 TK21 TK22 TK23 TK24 MACRO SHIFTL B1 B2 B3 B4 M1 M2
D19 LED D20 LED D21 LED D22 LED D23 LED D24 LED D25 LED D26 LED D27 LED D28 LED D29 LED D30 LED D31 LED D32 LED D33 LED D34 LED
R2
SUBV SOLO DISAB MUTE DIGI ARM IMPORT PROJ SPACE LEVEL BUP FADE NAME GRAB TRACK BLOCK TAKES NUDGE WAVE EDIT SOFT1 SOFT2 JOG REW SOFT3 FF
D35 LED D36 LED D37 LED D38 LED D39 LED D40 LED D41 LED D42 LED D43 LED D44 LED D45 LED D46 LED D47 LED D48 LED D49 LED D50 LED
R3
PLAY SOFT4 SOFT5 STOP REC PLAY MENU EDIT LOOP EDIT MARK GPI ADR PREROLL OFFSET DOWN MFX GOTO AUDIO BASE PRINT GATE EQ
D51 LED D52 LED D53 LED D54 LED D55 LED D56 LED D57 LED D58 LED D59 LED D60 LED D61 LED D62 LED D63 LED D64 LED D65 LED D66 LED
R4
SETUP M1 SETUP M2 DISK <JUMP JUMP> SETUP GEN FROM TO UNDO FREEZE EDITS FREEZE TRACKS MENU1 MENU2 MENU3 M3 M4
D67 LED D68 LED D69 LED D70 LED D71 LED D72 LED D73 LED D74 LED D75 LED D76 LED D77 LED D78 LED D79 LED D80 LED D81 LED D82 LED
Title
ESP-MFK - LEDs
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: leds.sch
Revision: 2.0
Design: Chris Alfred
Date: 11-Nov-1998
Sheet 10 of 10

9MW4RK1 - Merlin Console Keyboard Card

Merlin Console Test ROM

Entering Diagnostics

Hold down keys 4, 5, 6 on the console while turning the power on. This should cause the console to enter the diagnostics mode. To enter each test press one of the numeric keys. Some tests exit automatically, and some tests need to be completed by pressing "clear" key on the Merlin surface or "ESC" on the AT Keyboard.
Tests Number and Description

0 LED SRAM TEST
This test writes four data values (00000000, FFFFFFFF, aa55aa55, 55aa55aa) to the SRAM that stores the LED data. The LCD displays the results from the test, and will show the address where an error has occurred.

1 PANEL KEYBOARD TEST
Shows the output from the panel keys on the Merlin Console. To return from the test, press the "clear" key. The screen should be in the following format.

00 00 00 00 00 00 00 00 00 00 00 00
00 00 00 00 00 00 00 00 00 00 0000 00

The first line shows the hexadecimal output from the 96 track keys. Each pair of digits shows one key row consisting of the output for 8 keys. For example, an output of 40h (01000000) indicates that one key on that row is held down. Therefore D6 on the data bus is active.

The next line shows the hexadecimal output from the 72 remaining keys in the first 9 byte outputs. The remaining part of the display (00 0000 00) is the jogger output (00), the decoded value of the last character (0000) and the number of buttons being held down (00).

2 AT KEYBOARD OUTPUT
Displays the value of the latest ASCII character received from the AT Keyboard. To return from the test, press the ESC key on the keyboard.

3 EMC TEST FUNCTION
Flashes LEDs, scrolls text on the LCD and sends characters on the RS232 line. To return from the test, press the "clear" key.

4 TURN ALL 'A' LEDS ON
Each key switch has either one or two LEDs to indicate the state of the key. This test turns on what is defined as the 'A' LED for each key.

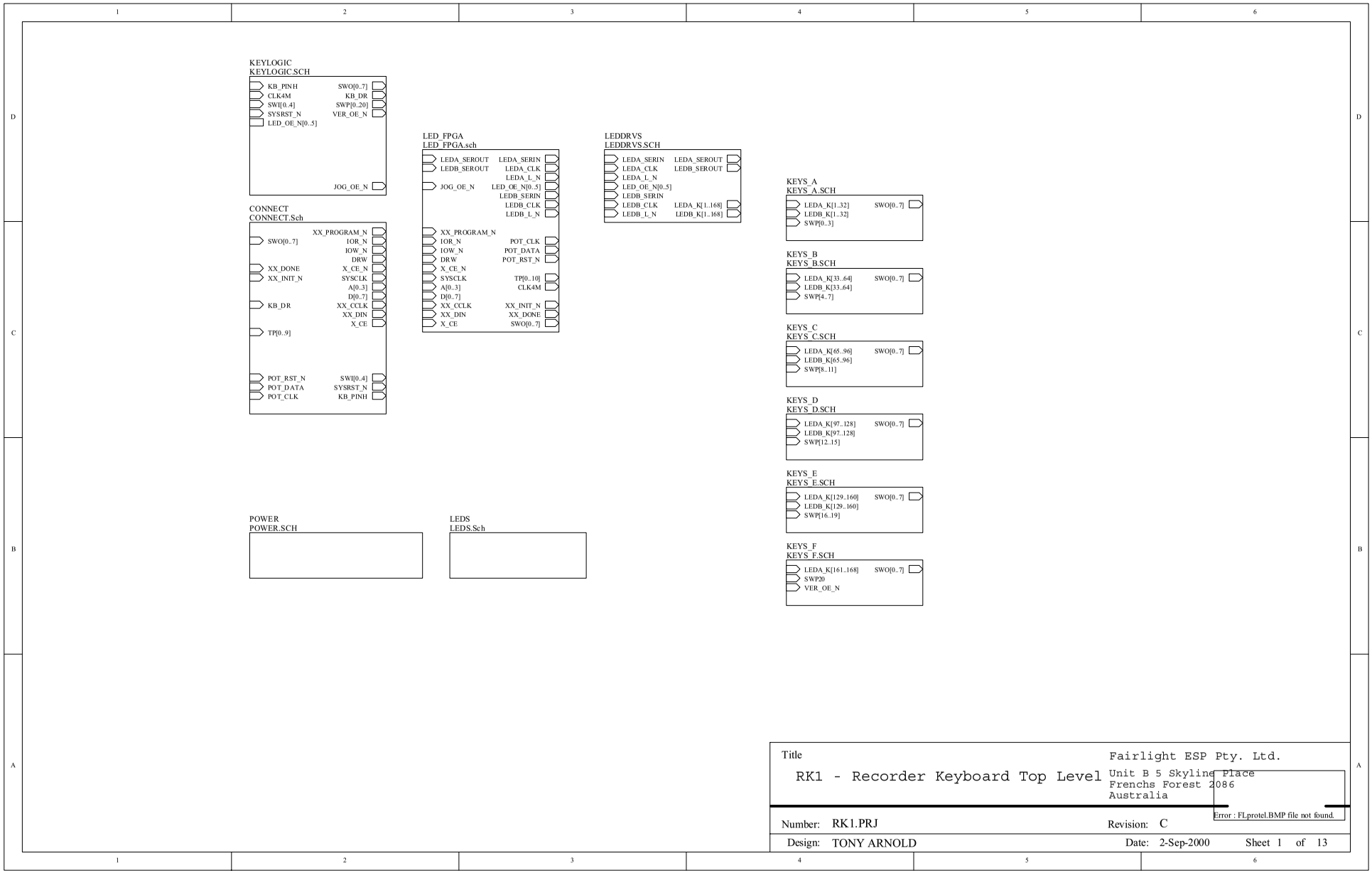
5 TURN ALL 'B' LEDS ON
This test turns on what is defined as the 'B' LED for each key.

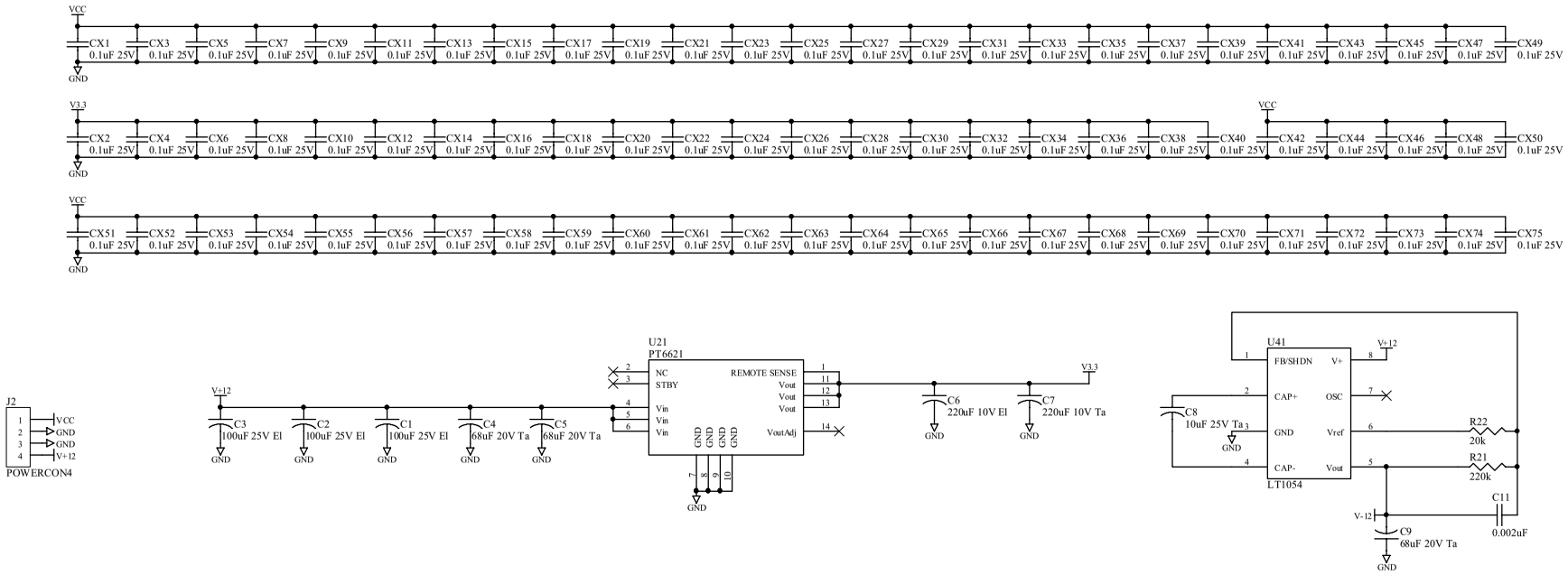
6 TURN OFF ALL LEDS

7 SPEAKER TEST

8 UNDEFINED TEST

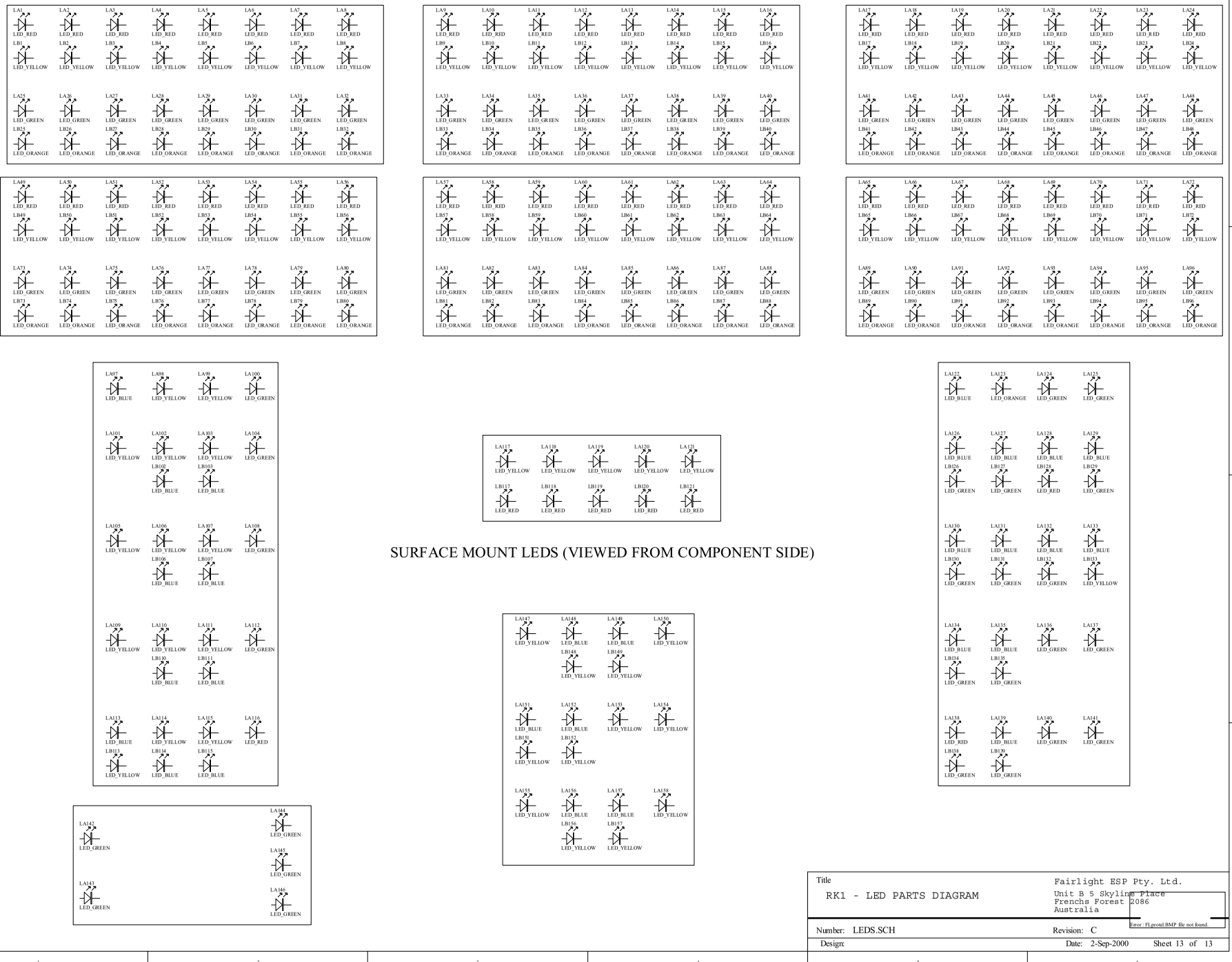
9 RESET CONSOLE

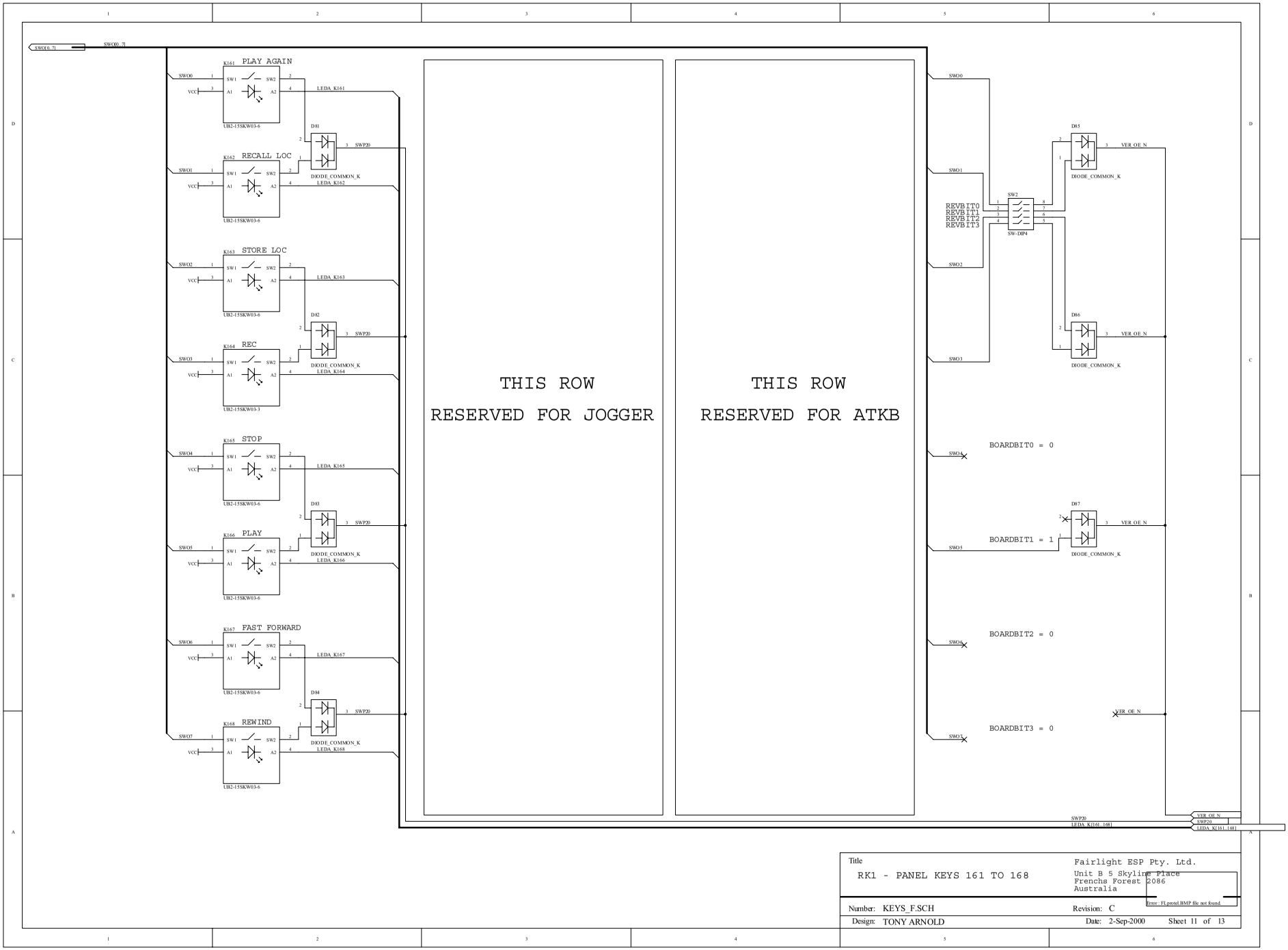

KEYLOGIC
KEYLOGIC.SCH
KB_PINH
CLK4M
SWI[0..4]
SYSRST_N
LED_OE_N[0..5]
SWO[0..7]
KB_DR
SWP[0..20]
VER_OE_N
JOG_OE_N
CONNECT
CONNECT.Sch
SWO[0..7]
XX_DONE
XX_INIT_N
KB_DR
TP[0..9]
POT_RST_N
POT_DATA
POT_CLK
XX_PROGRAM_N
IOR_N
IOW_N
DRW
X_CE_N
SYSCLK
A[0..3]
D[0..7]
XX_CCLK
XX_DIN
X_CE
SWI[0.4]
SYSRST_N
KB_PINH
LED_FPGA
LED_FPGA.sch
LEDA_SEROUT
LEDB_SEROUT
JOG_OE_N
XX_PROGRAM_N
IOR_N
IOW_N
DRW
X_CE_N
SYSCLK
A[0..3]
D[0..7]
XX_CCLK
XX_DIN
X_CE
LEDA_SERIN
LEDA_CLK
LEDA_L_N
LED_OE_N[0..5]
LEDB_SERIN
LEDB_CLK
LEDB_L_N
POT_CLK
POT_DATA
POT_RST_N
TP[0..10]
CLK4M
XX_INIT_N
XX_DONE
SWO[0..7]
LEDDRVS
LEDDRVS.SCH
LEDA_SERIN
LEDA_CLK
LEDA_L_N
LED_OE_N[0..5]
LEDB_SERIN
LEDB_CLK
LEDB_L_N
LEDA_SEROUT
LEDB_SEROUT
LEDA_K[1..168]
LEDB_K[1..168]
KEYS_A
KEYS_A.SCH
LEDA_K[1..32]
LEDB_K[1..32]
SWP[0..3]
SWO[0..7]
KEYS_B
KEYS_B.SCH
LEDA_K[33..64]
LEDB_K[33..64]
SWP[4..7]
SWO[0..7]
KEYS_C
KEYS_C.SCH
LEDA_K[65..96]
LEDB_K[65..96]
SWP[8..11]
SWO[0..7]
KEYS_D
KEYS_D.SCH
LEDA_K[97..128]
LEDB_K[97..128]
SWP[12..15]
SWO[0..7]
KEYS_E
KEYS_E.SCH
LEDA_K[129..160]
LEDB_K[129..160]
SWP[16..19]
SWO[0..7]
KEYS_F
KEYS_F.SCH
LEDA_K[161..168]
SWP20
VER_OE_N
SWO[0..7]
POWER
POWER.SCH
LEDS
LEDS.Sch
Title
RK1 - Recorder Keyboard Top Level
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Error : FLprotel.BMP file not found.
Number: RK1.PRJ
Revision: C
Design: TONY ARNOLD
Date: 2-Sep-2000
Sheet 1 of 13



Title	RK1 - POWER SUPPLY	Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number:	POWER.SCH	Revision:	C
Design:	TONY ARNOLD	Date: 2-Sep-2000	Sheet 12 of 13

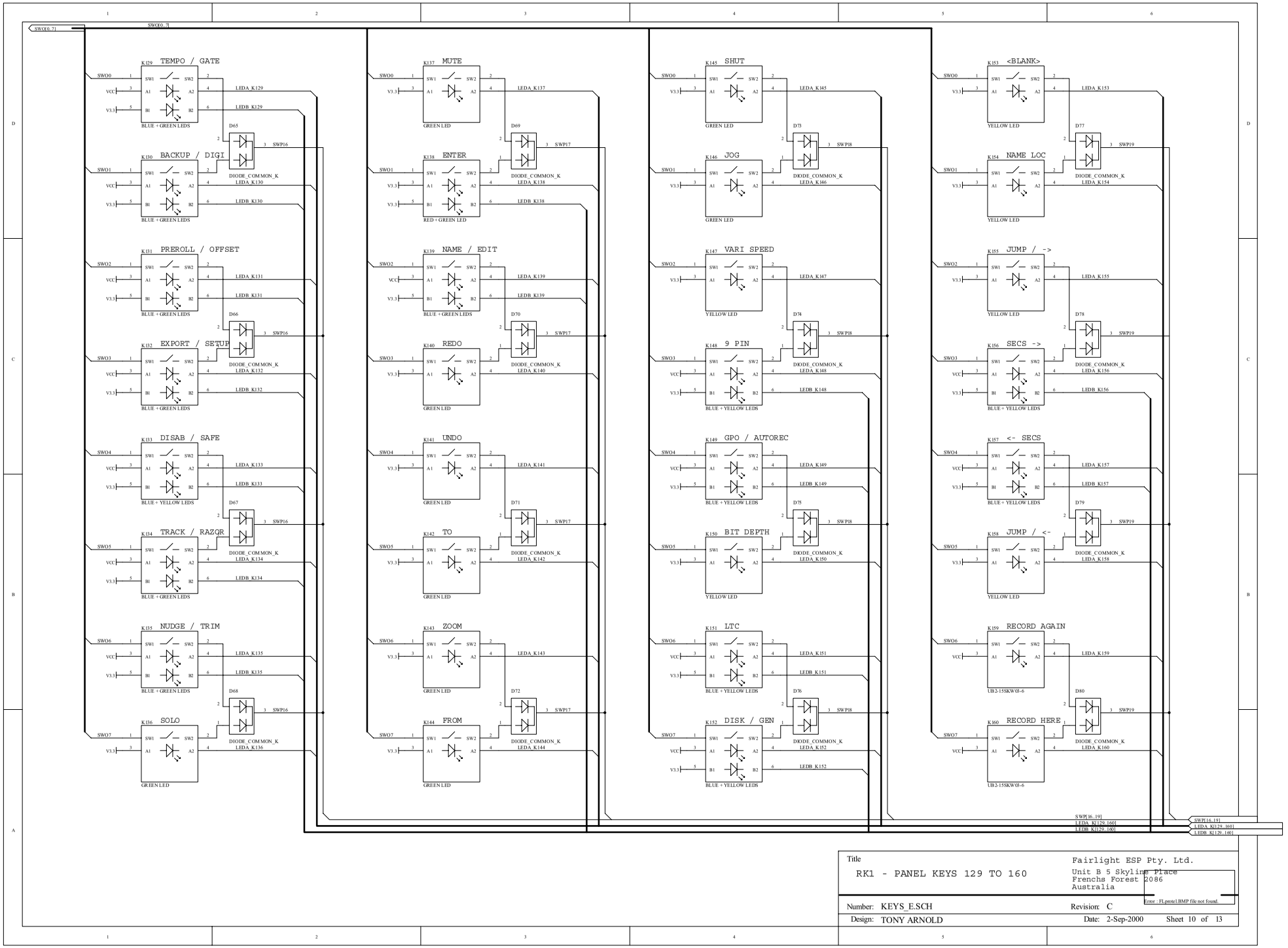
Error : FLprotel.BMP file not found.


SURFACE MOUNT LEDS (VIEWED FROM COMPONENT SIDE)
Title
RK1 - LED PARTS DIAGRAM
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Error : FL.protel.BMP file not found.
Number: LEDS.SCH
Revision: C
Design:
Date: 2-Sep-2000
Sheet 13 of 13



Title: RK1 - PANEL KEYS 161 TO 168	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: KEYS_F.SCH	Revision: C
Design: TONY ARNOLD	Date: 2-Sep-2000 Sheet 11 of 13

Error : FLpostel.BMP file not found.



Title	RK1 - PANEL KEYS 129 TO 160
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: KEYS_E.SCH	Revision: C
Design: TONY ARNOLD	Date: 2-Sep-2000 Sheet 10 of 13

Error : FLpnote.UBMP file not found.

DRAFT

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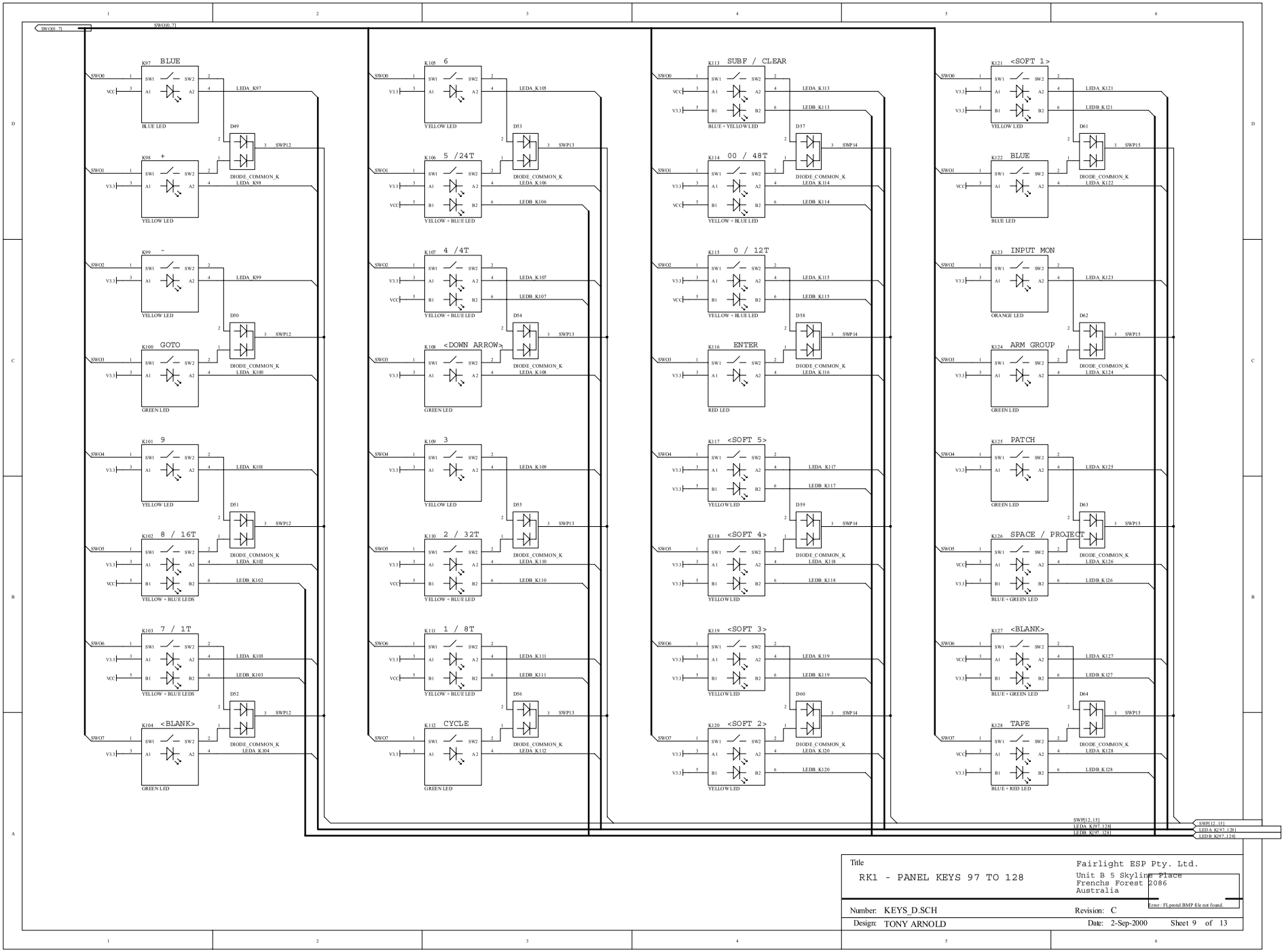
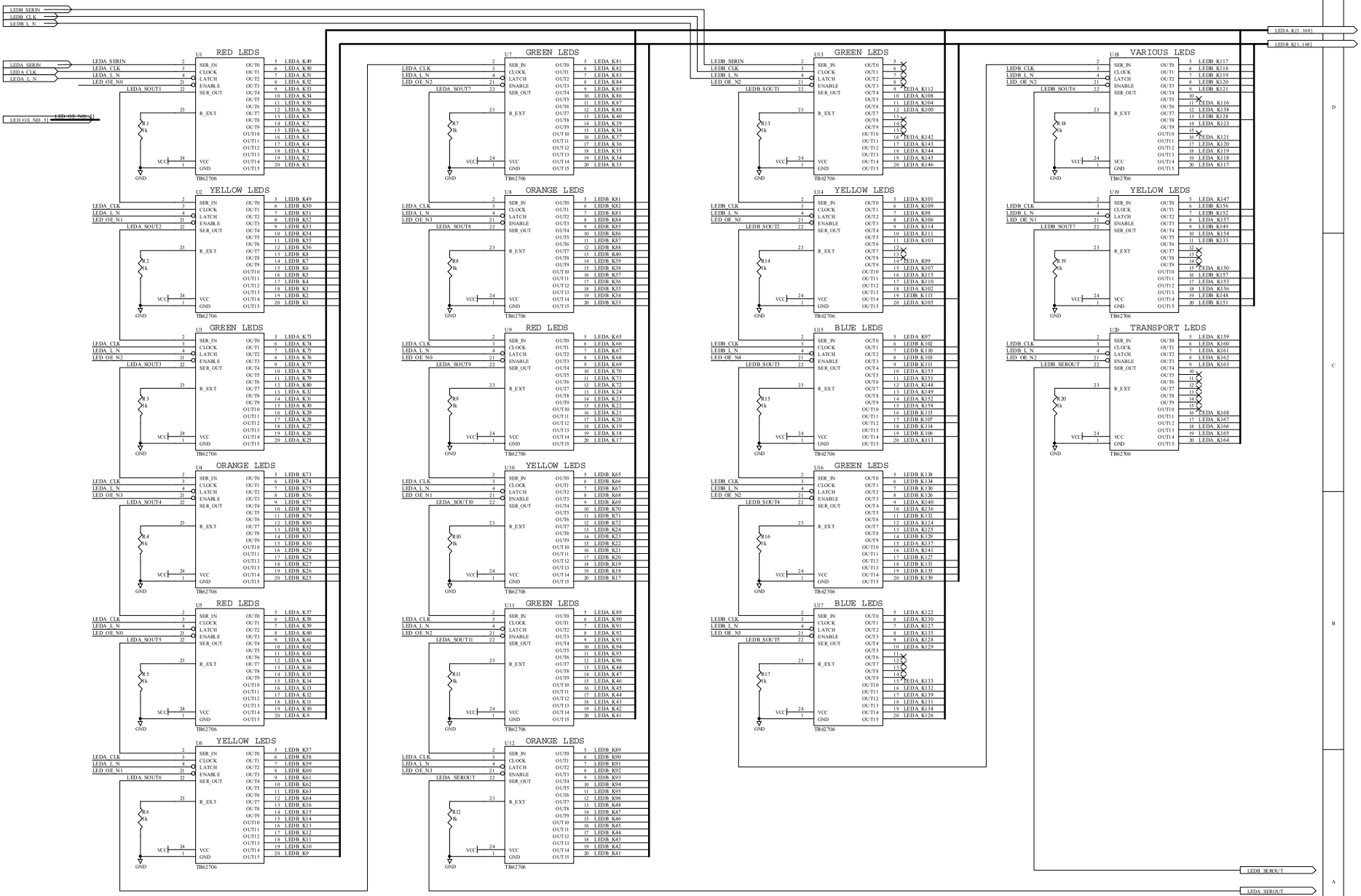


Title	RK1 - PANEL KEYS 97 TO 128	Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place, Frenchs Forest 2086, Australia
Number:	KEYS_D.SCH	Revision:	C
Design:	TONY ARNOLD	Date:	2-Sep-2000
		Sheet	9 of 13

Error : FLpsotel.BMP file not found.



Title	RK1 - CONSTANT CURRENT LED DRIVERS
	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
	Error : FL:posted.BMP file not found.
Number:	LEDDRVS.SCH
Revision:	C
Design:	TONY ARNOLD
Date:	2-Sep-2000
Sheet	5 of 13

DRAFT

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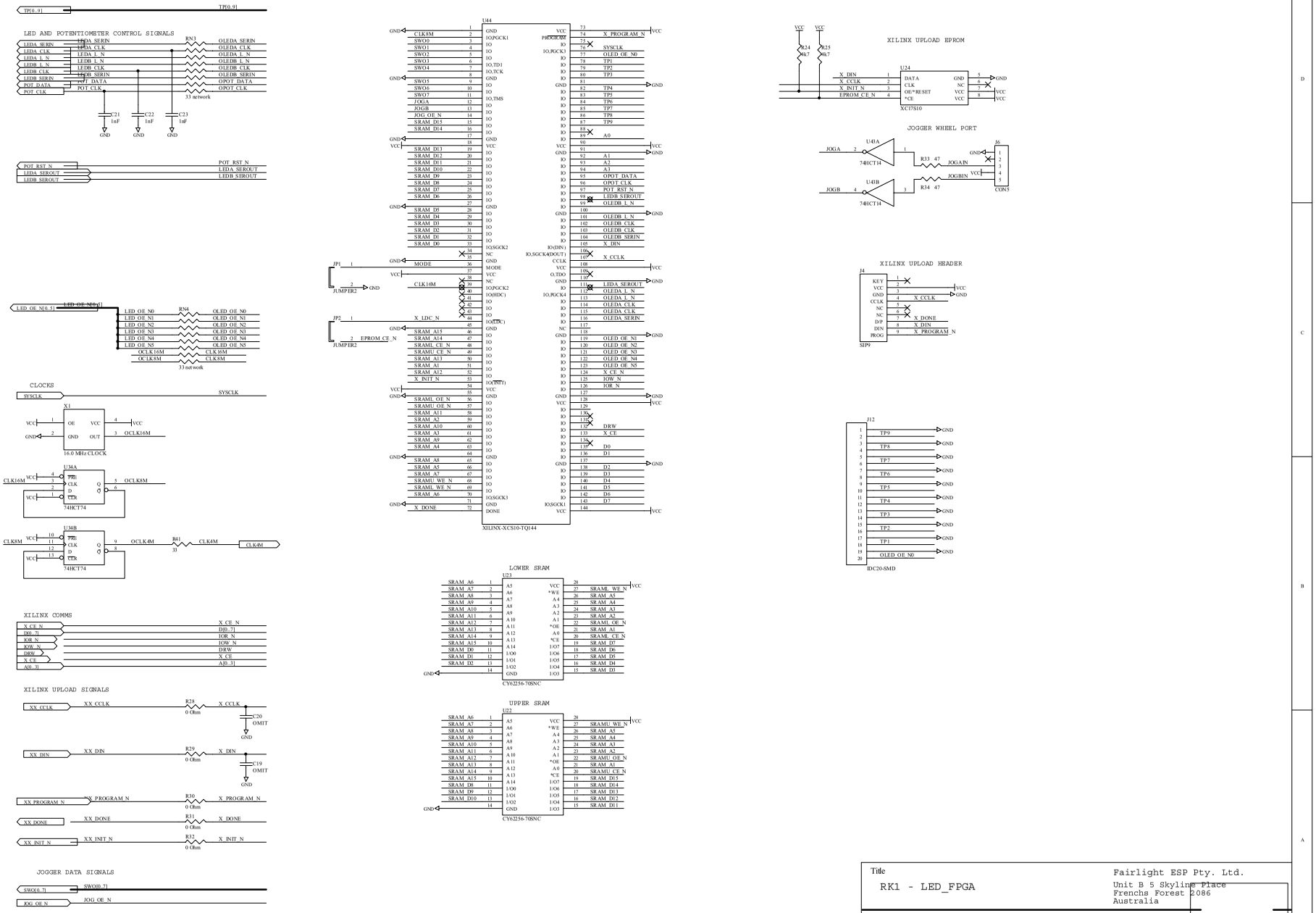
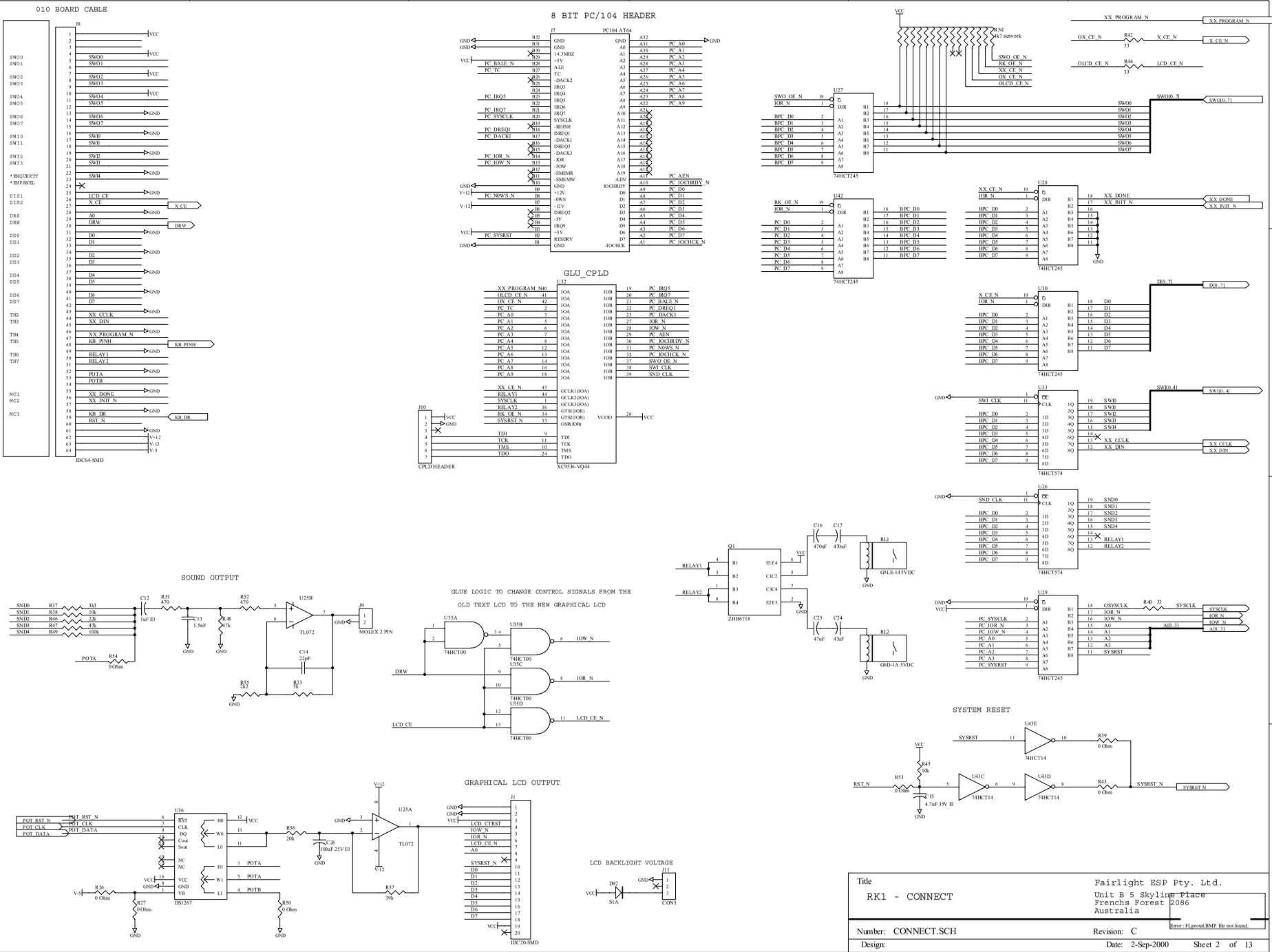


TONY ARNOLD

Title: RK1 - LED_FPGA	Fairlight ESP Pty. Ltd. Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: LED_FPGA.SCH	Revision: C
Design:	Date: 2-Sep-2000 Sheet 3 of 13

Error : F1proto1.BMP file not found.


010 BOARD CABLE
8 BIT PC/104 HEADER
GLU_CPLD
SOUND OUTPUT
GLUE LOGIC TO CHANGE CONTROL SIGNALS FROM THE
OLD TEXT LCD TO THE NEW GRAPHICAL LCD
SYSTEM RESET
GRAPHICAL LCD OUTPUT
LCD BACKLIGHT VOLTAGE
IDC64-SMD
CPLD HEADER
XC9536-VQ44
MOLEX 2 PIN
1DC20-SMD
Title
RK1 - CONNECT
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: CONNECT.SCH
Revision: C
Design:
Date: 2-Sep-2000
Sheet 2 of 13

DRAFT

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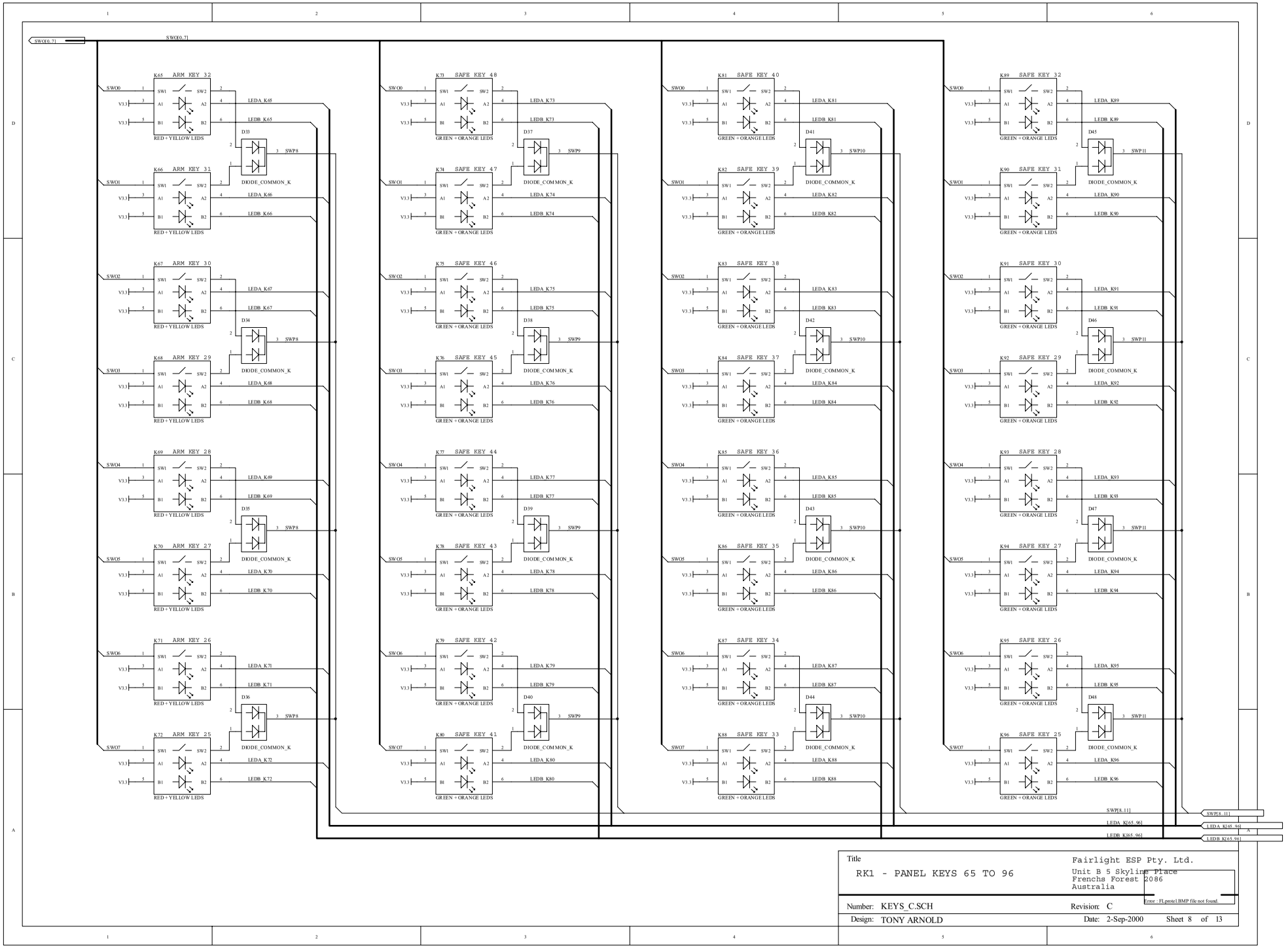
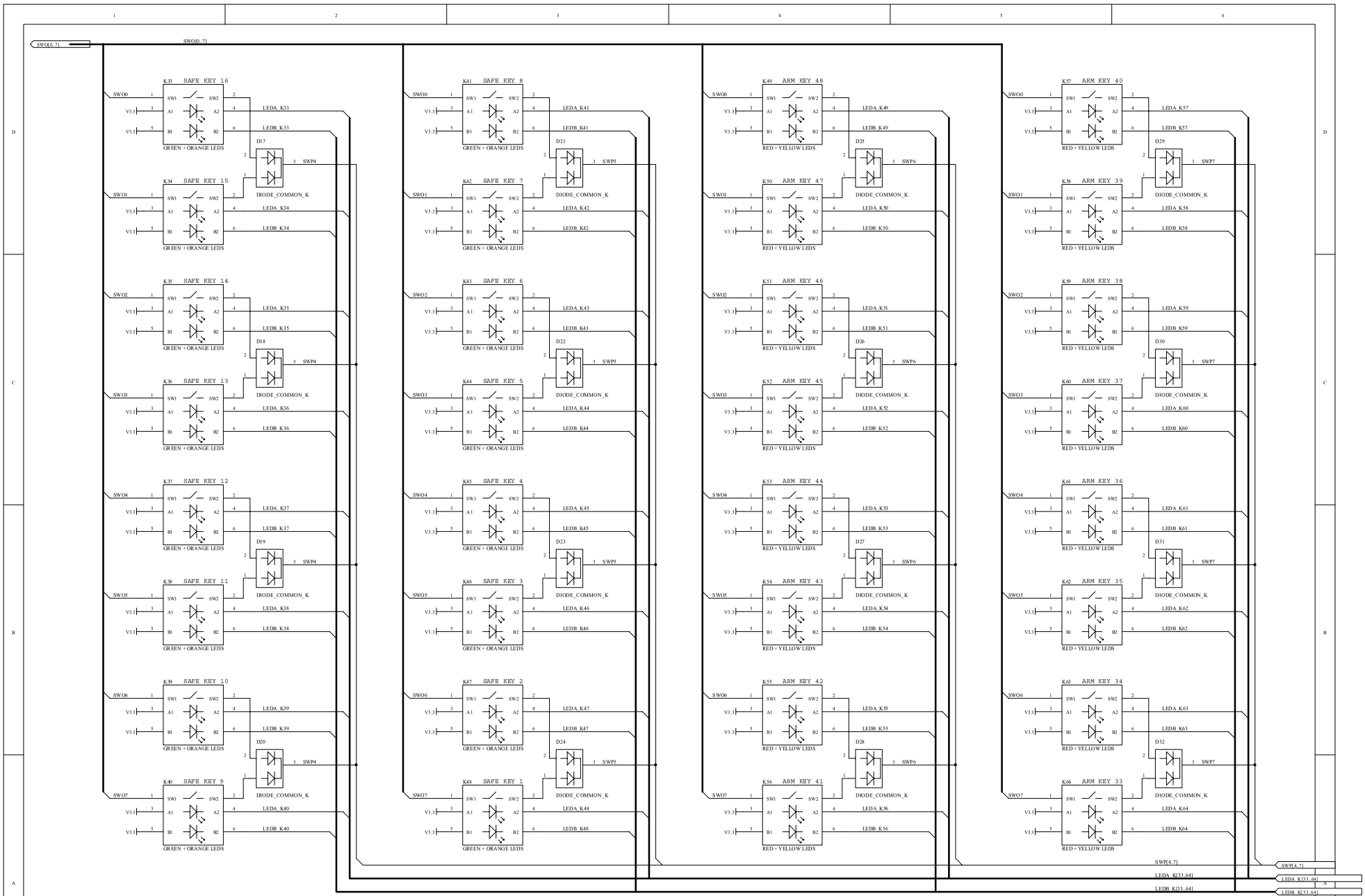


Title	RK1 - PANEL KEYS 65 TO 96
Fairlight ESP Pty. Ltd.	Unit B 5 Skylins Place Frenchs Forest 2086 Australia
Number: KEYS_C.SCH	Revision: C
Design: TONY ARNOLD	Date: 2-Sep-2000 Sheet 8 of 13

Error : FLpntoLIBMP file not found.



Title	RK1 - PANEL KEYS 33 TO 64
Fairlight ESP Pty. Ltd.	Unit B 5 Skyline Place Frenchs Forest 2086 Australia
Number: KEYS_B.SCH	Revision: C
Design: TONY ARNOLD	Date: 2-Sep-2000 Sheet 7 of 13

Error: FLprotoLIBMP file not found.

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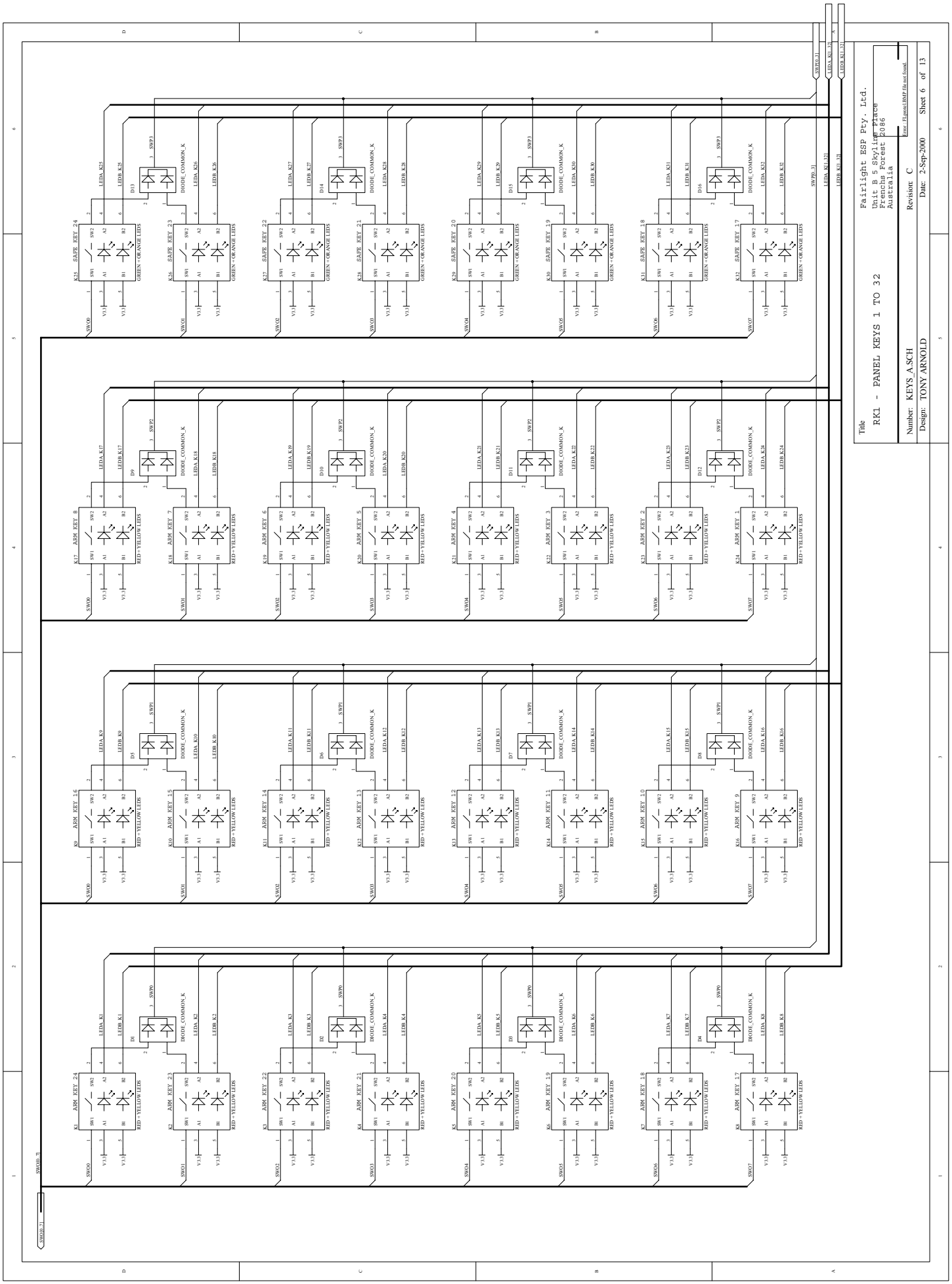
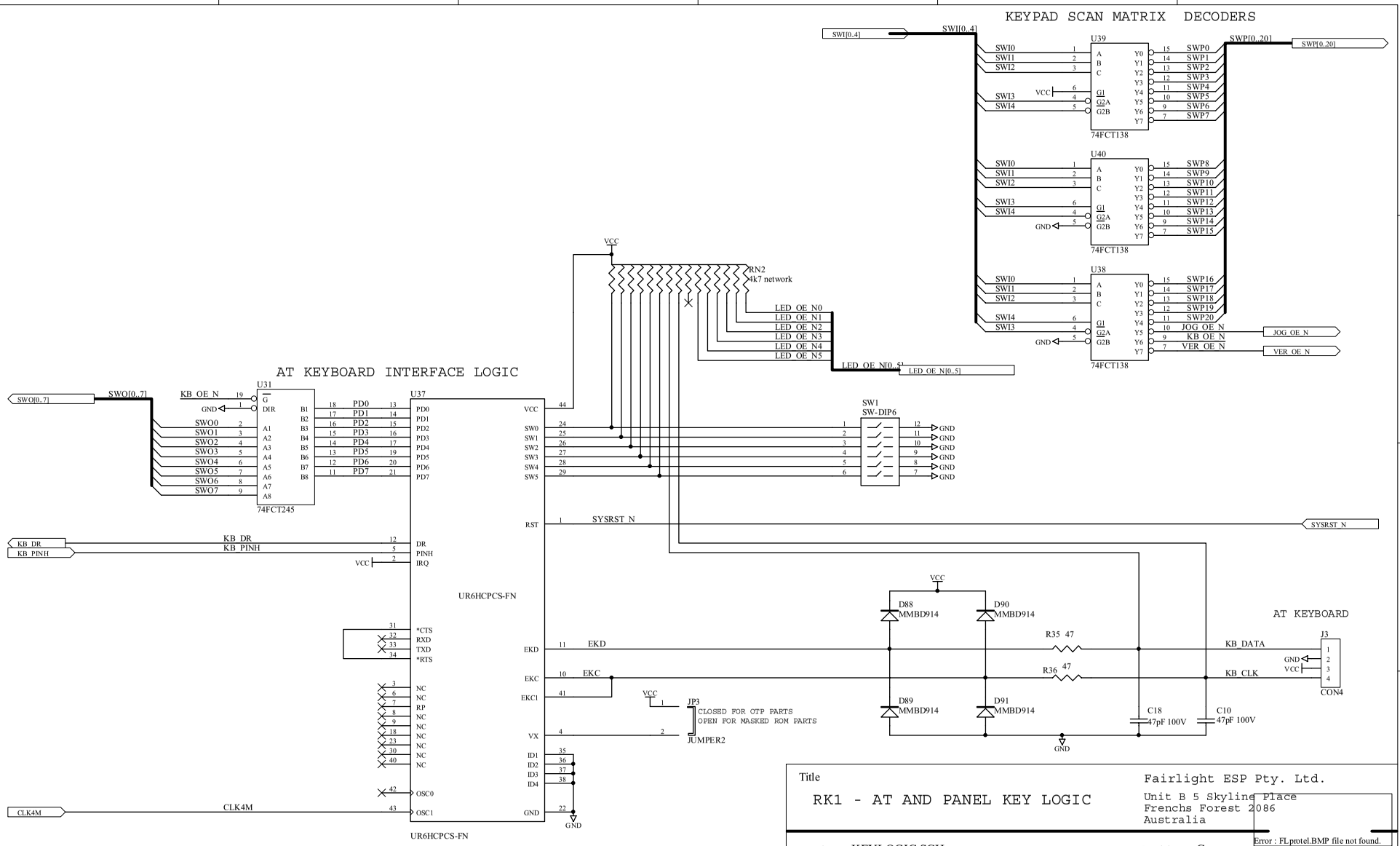
DRAFT


Title
RK1 - PANEL KEYS 1 TO 32
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Number: KEYS_A.SCH
Revision: C
Design: TONY ARNOLD
Date: 2-Sep-2000
Sheet 6 of 13
Error: FI.guess[1].BMP file not found.


KEYPAD SCAN MATRIX DECODERS
SWI[0..4]
U39
U40
U38
74FCT138
SWP[0..20]
SWP0
SWP1
SWP2
SWP3
SWP4
SWP5
SWP6
SWP7
SWP8
SWP9
SWP10
SWP11
SWP12
SWP13
SWP14
SWP15
SWP16
SWP17
SWP18
SWP19
SWP20
JOG_OE_N
KB_OE_N
VER_OE_N
RN2
4k7 network
LED_OE_N0
LED_OE_N1
LED_OE_N2
LED_OE_N3
LED_OE_N4
LED_OE_N5
LED_OE_N[0..5]
AT KEYBOARD INTERFACE LOGIC
SWO[0..7]
U31
74FCT245
U37
UR6HCPCS-FN
SW1
SW-DIP6
SYSRST_N
KB_DR
KB_PINH
JP3
CLOSED FOR OTP PARTS
OPEN FOR MASKED ROM PARTS
JUMPER2
CLK4M
EKD
EKC
D88
D89
D90
D91
MMBD914
R35 47
R36 47
C18
47pF 100V
C10
47pF 100V
AT KEYBOARD
KB_DATA
KB_CLK
CON4
Title
RK1 - AT AND PANEL KEY LOGIC
Fairlight ESP Pty. Ltd.
Unit B 5 Skyline Place
Frenchs Forest 2086
Australia
Error : FLprotel.BMP file not found.
Number: KEYLOGIC.SCH
Revision: C
Design: TONY ARNOLD
Date: 2-Sep-2000
Sheet 4 of 13

BOM Part Number requests

1FM2-M3UG
FAME 2 Upgrade Kit

Application

Provides everything required to upgrade an existing FAME 1 to a FAME 2.

Contents

QTY	Description	Fairlight Part Number
1	M4 Rack fitted with 3 x QDCs, 24 x Digital IO and 24 x Analogue IO	
1	M4 to MFK console cable adapter	AMW4112-A
1	Set M4 compatible ROMs for MFK console	SRD9552FM2
1	FAME V3.1 or later Mix and Automation Manual	DFM2101-A
1	FAME V16.2 or later Editing and Recording Manual	DFM2102-A
1	FAME 2 Installation manual	DFM2100-A
1	FAME V3.1 or later software update disk set	7FM1111

1MW4-M3ADAPT
FAME 2 Upgrade Engine connector adapter Kit

Application

Provides cable adapters to connect an existing FAME 1 wiring installation to a FAME 2 engine.

Contents

QTY	Description	Fairlight Part Number
3	M4 50-pin D to MFX 3 15 pin D analogue Input adapter cables	AMW4110-A
3	M4 50-pin D to MFX 3 15 pin D analogue Output adapter cables	AMW4110-A
3	M4 50-pin D to MFX 3 37 pin Digital IO adapter cables	AMW4111-A
2	9-pin adapter connectors (9-pin female-female gender changer)	AMW4116-A

1	AES IO adapter cable	AMW4117-A
1	MIDI IO adaptor cable	AMW4114-A
1	GPIO adaptor cable	AMW4115-A
1	LTC IO adapter Cable	AMW4113-A

1MW4-8CHUG
FAME 2 IO Expansion Kit (8 IO)

Application

Offers an upgrade from the standard 24 IO to a 32 IO configuration FAME 2.

Contents

QTY	Description	Fairlight Part Number
1	M4 AES card	9MW4061
1	M4 Analogue Input card	9MW4081
1	M4 Analogue Output card	9MW4091

9MW4-SPARES
M4 Engine complete Spares Kit

Application

Provides a complete set of spare parts for an M4 engine.

Contents

QTY	Description	Fairlight Part Number
1	QDC Spares kit	9MW4041S
1	PXY spares Kit	9MW4011S
1	PSU	9PS1611
1	PXY daughter board kit	9MW4051S

9MW4041S

QDC Spares Kit

Application

Provides a basic set of QDC spare parts for an M4 engine.

Contents

QTY	Description	Fairlight Part Number
1	QDC	9MW4041
1	Analogue Output Card	9MW4091
1	Analogue Input Card	9MW4081
1	AES IO card	9MW4061

9MW4011S
PXY Spares Kit

Application

Provides a spare PXY for an M4 engine. It's a built PXY without daughter boards.

Contents

QTY	Description	Fairlight Part Number
1	PXY	9MW4011
1	IOC	9MW4032
1	PXY Metalwork (assembled to PXY/IOC)	MMW4025

9MW4051S
PXY daughter board Kit

Application

Provides a set of PXY daughter boards.

Contents

QTY	Description	Fairlight Part Number
1	SIO1	9MW4101
1	SIO2	9MW4102
1	CG5	9MW4051
1	Network card	PASYPWBPNE